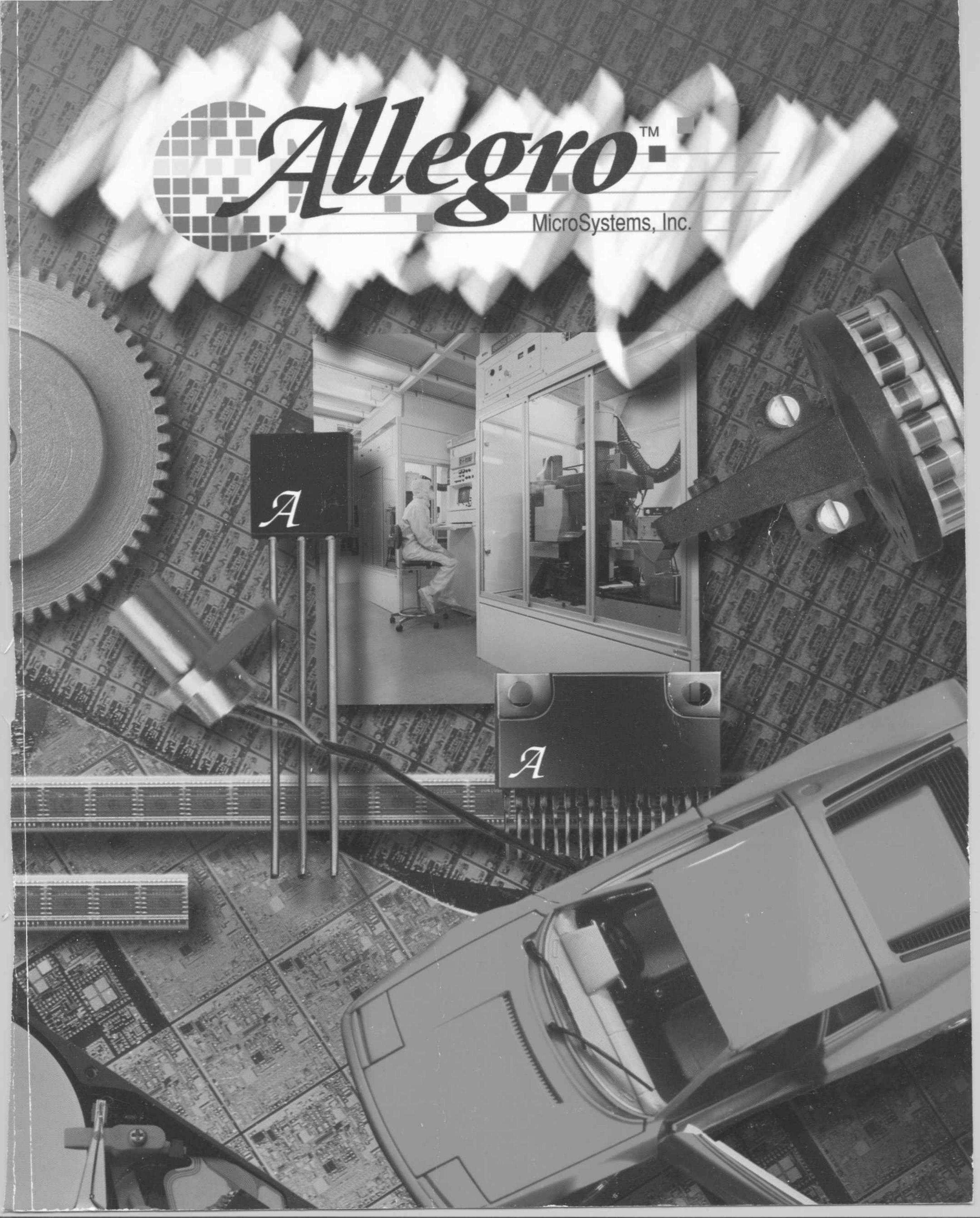
Allegro™
MicroSystems, Inc.

INTEGRATED AND DISCRETE

SEMICONDUCTORS

Applications for

- EDP Peripherals
- Industrial Control
- Motor & Power Drive
- Office Automation
- Mass Storage
- Automotive
- Consumer
- Displays
- Power Management

Allegro MicroSystems, Inc.

Formerly Sprague Semiconductor Group

115 Northeast Cutoff, Box 15036
Worcester, MA 01615
(508) 853-5000

Data Book AMS-502

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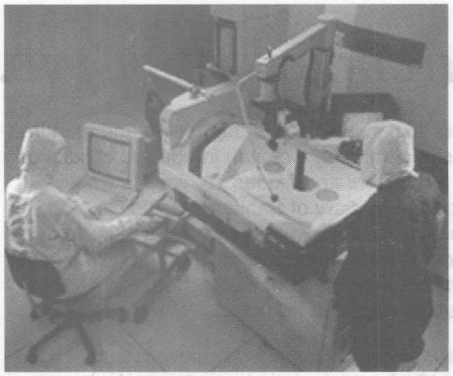
GENERAL INFORMATION

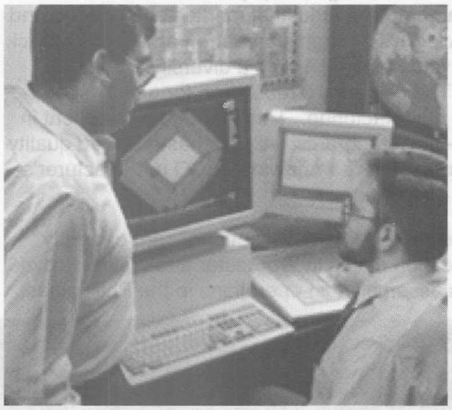
ALLEGRO MICROSYSTEMS, INC.

Allegro MicroSystems, Inc. specializes in the design and manufacture of advanced mixed-signal (analog + digital) integrated circuits as well as a line of discrete transistors and diodes. Allegro, a wholly-owned, American-managed subsidiary of Sanken Electric Co., Ltd., combines 30 years of semiconductor experience, over a decade of extensive merged-technologies experience, and worldwide resources in design and applications engineering, process technology, packaging, quality control, manufacturing, and testing.

Allegro is a leading supplier of mixed-signal solutions and emphasizes system-level ICs for original equipment manufacturers that primarily serve the automotive, industrial markets, consumer, and computer peripherals. Allegro's strengths center on an excellent track record in product quality and innovation, and a diversified base of major OEM customers. The company's reputation for quality spans both product design and manufacturing. This reputation is evident in preferred vendor/ship-to-stock programs. Allegro has received quality awards from leading manufacturers worldwide, IECQ manufacturer's approval, and ISO 9001 registration.

Headquartered in Worcester, Massachusetts, Allegro currently operates two wafer-fabrication plants in Worcester and Willow Grove, Pennsylvania, as well as assembly/test operations in the Philippines.





Allegro also jointly develops and markets leading-edge products with Sanken in the areas of power management and motion control. This enables both organizations to fully utilize the company's world-wide strengths and resources for the benefit of our customers.

Allegro's product expertise in power ICs, signal processing ICs, and Hall-Effect sensor ICs—believed to be unique in the industry—is supported by strong capabilities in bipolar, CMOS, and DMOS process technologies. Allegro can and does combine any two or all three of its product disciplines (and/or process technologies) in a single monolithic chip to deliver powerful system-level solutions.

Within the worldwide semiconductor market, Allegro has strategically positioned itself in the analog segment. Allegro primarily serves the analog IC industry through the development, manufacture, and marketing of a wide variety of complex products. The company emphasizes application-specific, market-driven products with high technology content. These include bipolar, CMOS, and DMOS technologies, as well as merged technologies such as BiCMOS (bipolar + CMOS), BCD (bipolar + CMOS + DMOS), and DABIC (digital + analog + BiCMOS).

Analog ICs can generally be separated into three classifications: sensor, signal processing, and power ICs. Sensors are analog ICs that respond to physical phenomena and provide inputs to an electronic system. Signal processing ICs represent a broad category of analog ICs that accept, generate, or process an analog signal. Power ICs are those products which act as the interface from an electronic system back to the physical world. These products typically operate at voltages and currents well in excess of those applied to other parts of the electronic system due to their requirement to drive motors, displays, solenoids, relays, lamps, and other devices.

At Allegro, original designs are emphasized, rather than second source products. Many of these original designs have ultimately become industry standard products, such as the company's popular Hall-effect switches and power drivers.

Customers expect suppliers to add tangible value at a system level because they need to maximize performance and speed time to market. Applications, design, and technology consultation provided by IC suppliers, therefore, become crucial, as does the working synergy between the two design partners. Customers also need to feel confident in their IC supplier's ability to control the manufacturing and testing processes, thereby ensuring quality, reliability, and consistent delivery.

Allegro is exceptionally positioned to serve each customer's system requirements with either application-specific custom products or a broad spectrum of standard products. The measure of our success is your total satisfaction.

SECTION 1. GENERAL INFORMATION & PRODUCT INDEX

INTEGRATED CIRCUITS AND TRANSISTOR ARRAYS

*ICs and TRANSISTOR ARRAYS PRODUCT INDEX in NUMERICAL ORDER**

(See Section 8 for Index to Discrete Devices)

* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

ICs AND TRANSISTOR ARRAYS
PRODUCT INDEX IN NUMERICAL ORDER

* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

ICs AND TRANSISTOR ARRAYS
PRODUCT INDEX IN NUMERICAL ORDER

* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

* Complete part number includes additional characters to indicate operating temperature range and package style. See detailed specification.

GENERAL INFORMATION

DEFINITION OF TERMS

ABSOLUTE MAXIMUM RATINGS are limiting values of operation and should not be exceeded under the worst conditions. These values are chosen to provide acceptable serviceability of the device. The equipment manufacturer should design so that initially, and throughout life, no absolute maximum value is exceeded. If exceeded, even if the device continues to operate, its life may be considerably shortened.

The absolute maximum output current ratings are the maximum allowable under any condition. In application, output current will be limited by number of outputs conducting, duty cycle and timing, ambient temperature, heat sinking and/or forced cooling, and other heat sources.

Under any set of conditions, the specified maximum junction temperature (usually +150°C) should not be exceeded. In those devices which include an internal thermal shutdown, fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

TYPICAL CHARACTERISTICS are given for circuit design information only and, unless otherwise stated, are usually given at the nominal operating voltage and an ambient temperature of +25°C. Although these values are indicative of the peak distribution for a large number of production lots, these values should not be construed as guaranteed for any particular device or production lot.

CHARACTERISTICS LIMITS are those values that are guaranteed under the test conditions shown.

The absolute magnitude convention is used for **Electrical Characteristics Limits** where the limits are defined as:

> maximum [minimum] limit: the greater [smaller] magnitude limit of a range of like-signed values; if the range includes both positive and negative values, both limiting values are maximums [the minimum is implicitly zero].

The algebraic convention is used for **Magnetic Characteristics Limits** where negative flux densities are defined as less than zero. The minimum value is therefore the most negative value, the maximum value is the most positive value, and zero has no special significance.

RECOMMENDED OPERATING CONDITIONS are given for optimum device performance. Operation outside these conditions is permitted (within the Absolute Maximum Ratings) without any implied guarantee of level of performance.

DEFINITION OF TERMS

IMPORTANT NOTICE

Allegro MicroSystems, Inc., reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Changes and improvements made after the publication of this catalog will be reflected in updated data sheets or other literature as soon as possible. Components made under military approvals will be in accordance with the approval requirements.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

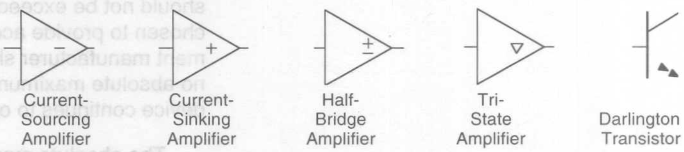
Allegro MicroSystems, Inc. reserves the right to discontinue any device without notice.

Before placing an order, Allegro advises its customers to obtain the latest version of the relevant information to verify that the information being relied upon is current.

Allegro products are not intended for use in life support appliances, devices, or systems. Use of an Allegro product in such applications without the written consent of Allegro MicroSystems, Inc. is prohibited.

It is recommended that equipment manufacturers consult their local sales office whenever device applications involve unusual electrical, mechanical, or environmental operating conditions.

SPECIAL SYMBOLS are sometimes used to simplify circuit drawings.



Dwg. No. OA-001

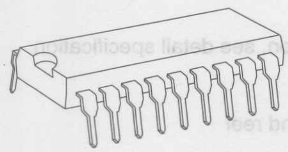
PRODUCT PREVIEW is used to advise customers of proposed additions to the product line. The specifications given are target or goal specifications and may, therefore, change without notice. Allegro MicroSystems, Inc. reserves the right to not manufacture proposed devices that have been announced as “product preview”; samples may not be available yet. It is imperative that you contact your local sales office for details of current status and latest specifications prior to making any circuit design commitments.

ADVANCE INFORMATION (engineering prototypes) or **PRELIMINARY INFORMATION** (preproduction or first production) are used to advise customers of additions to the product line that, nevertheless, still have “preproduction” status. Details may, therefore, change without notice although it is expected that preliminary performance data is representative of “full production” status. Contact your local sales office for details of current status and latest specifications.

INTERIM DATA is used to describe a publication that is incomplete. The status of the products described may be advance, preliminary, or production. It is intended that a more complete description will follow.

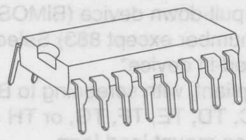
PACKAGE DESIGNATORS

A (DIP)
14 to 40 pins



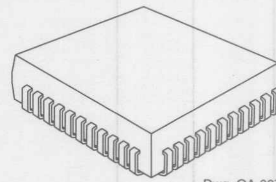
Dwg. OA-004-18

B (Semi-Tab DIP)
8 to 24 pins



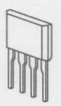
Dwg. OA-004-17

EA (One-Semi-Tab PLCC) 28 leads
EB (Semi-Tab PLCC) 28 or 44 leads
EP (Sq. PLCC) 20, 28, or 44 leads
EQ (Rect. PLCC) 32 (7 x 9) leads



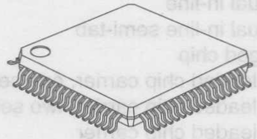
Dwg. OA-007-44

K (SIP) 4 pins
KA (SIP) 5 pins



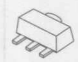
Dwg. OA-013-4

JT (Low-Profile Quad Flatpack)
64 leads



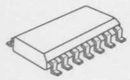
Dwg. OA-014-64

LL, LR, or LT (SOT)



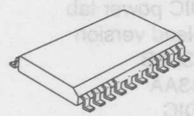
Dwg. OA-008-3

L (SOIC)
8, 14, or 16 leads

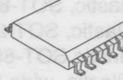


Dwg. OA-005-14

LB (Semi-Tab SOIC) 16 to 24 leads
LW (Wide-Body SOIC) 16 to 28 leads

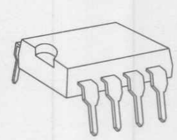


Dwg. OA-005-21



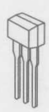
Dwg. OA-005-17

M (DIP) 8 pins



Dwg. OA-004-8

U

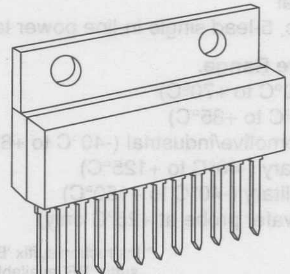


Dwg. OA-015-3

UA

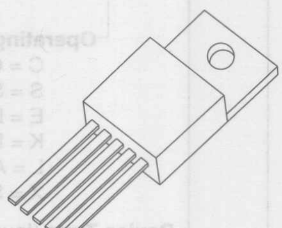
Dwg. OA-015-4

W (Power-Tab SIP) 12 leads



Dwg. OA-006-12

Z (Power-Tab SIP) 5 leads



Dwg. OA-006-5

DEVICE PART-NUMBERING

ALLEGRO MICROSYSTEMS NEW PART NUMBERS

A 8958 S EA F-1

Instructions (optional; in the order listed).

A = Revision, see detail specification
F = Active pull-down device (BiMOS only)
-1 = (Any number except 883) Selected version, see detail specification
BU = Burned-in device*
BS = Compliant, with screening to BS9493*
TA, TB, TC, TD, TE, TF, TG, or TH = Tape and reel
TL = Surface-mount lead form
TM or TP = Ammo pack taped
TR = Tape and reel (surface-mount devices only)

Package Designation.

A = Plastic, dual in-line
B = Plastic, dual in-line semi-tab
C = Unpackaged chip
EA = Plastic, leaded chip carrier, one semi-tab
EB = Plastic, leaded chip carrier, two semi-tabs
EP = Plastic, leaded chip carrier
EQ = Plastic, leaded chip carrier, rectangular
JT = Plastic, low-profile quad flatpack
K = Plastic, 4-lead mini-SIP
KA = Plastic, 5-lead mini-SIP
L = Plastic, SOIC
LB = Plastic, wide-body SOIC power tab
LL = Plastic, SOT-89, long-lead version
LR = Plastic, SOT-23/TO-236AB
LT = Plastic SOT-89/TO-243AA
LW = Plastic, wide-body SOIC
M = Plastic, 8-pin mini-DIP
U = Plastic, 3-lead thin mini-SIP
UA = Plastic, short 3-lead thin mini-SIP
W = Plastic, 12-lead single in-line power tab
X = Special
Z = Plastic, 5-lead single in-line power tab (TO-220)

Operating Temperature Range.

C = Commercial (0°C to +70°C)
S = Standard (-20°C to +85°C)
E = Extended automotive/industrial (-40°C to +85°C)
K = Industrial/military (-40°C to +125°C)
L = Automotive/military (-40°C to +150°C)
X = Special (i.e., wafer probe at +25°C only)

Device Type (four digits).

Allegro MicroSystems Identifier.

* Instruction suffix 'BU' available only with temperature codes 'S', 'E', 'K, or 'L'; suffix 'BS' available only through European sales office.

All possible combinations of device type, operating temperature range, and package style are not necessarily available. Consult individual device specification or sales office for complete information.

ORIGINAL SPRAGUE SEMICONDUCTOR GROUP PART NUMBERS

UC N 5810 A F-1

Instructions
Same as Allegro New Part Number System*

Package Designation.
Same as Allegro New Part Number System*

Device Type (four digits).

Operating Temperature Range.
K = Extended automotive/industrial (-40°C to +125°C)
L = Extended auomotive/industrial (-40°C to +150°C)
N = Commercial/industrial (-20°C to +85°C)
Q = Extended automotive/industrial (-40°C to +85°C)
S = Military

Family (UC, UD, UG, or UL).

* Instruction suffix 'BU' available only with temperature codes 'L', 'N', or 'Q'; suffix 'BS' available only through European sales office.

TMPT 3904 FM

Shipping Style
FM = Wafer sawn on frame
TA, TB, TC, TD, TE, TF, TG, or TH = Tape and reel
TS = Tray pack
WA = Whole wafer

Device Type (three or four digits).

Family.
BA– = Pro-Electron registered diode
BZ– = Pro-Electron registered Zener diode
TH* = Unpackaged discrete device chip
TMP* = SOT-23/TO-236AB packaged discrete device
TND = Diode array
TP = Bipolar transistor in TO-92/TO-226AA/AB
TPQ= Quad transistor array
1N = JEDEC registered diode
2N = JEDEC registered transistor

* D = diode
T = transistor
Z = Zener

All possible combinations of device type, operating temperature range, and package style are not necessarily available. Consult individual device specification or sales office for complete information.

GENERAL INFORMATION

ORDERING INFORMATION

To place an order, obtain price and delivery information, or to request technical literature, contact your local Allegro sales office or sales representative.

From United States and Canada	Allegro MicroSystems, Inc. 115 Northeast Cutoff Box 15036 Worcester, MA 01615 Tel: (508) 853-5000 Fax: (508) 853-7861
From Europe and Mideast	Allegro MicroSystems Europe Ltd. Balfour House, Churchfield Road Walton-on-Thames, Surrey KT12 2TD UNITED KINGDOM Tel: (44-1932) 253-355 Fax: (44-1932) 246-622
From Asia	Allegro MicroSystems Philippines, Inc. Sampaguita Street, Marimar Village Parangue, Metro Manila 1700 PHILIPPINES Tel: (63-2) 828-9026 Fax: (63-2) 828-4045

TECHNICAL ASSISTANCE

Requests for additional technical information or applications assistance should be referred to your local Allegro sales office, sales representative or

For Integrated Circuits	Allegro MicroSystems, Inc. 115 Northeast Cutoff Box 15036 Worcester, MA 01615 Tel: (508) 853-5000 Fax: (508) 853-7861
For Sensors and Discrete Devices	Allegro MicroSystems, Inc. 53 Regional Drive Concord, NH 03301 Tel: (603) 228-5533 Fax: (603) 224-2466
or call	**(508) Allegro** (508) 255-3476

RELIABILITY

BACKGROUND INFORMATION

CMOS, bipolar, and BiMOS integrated circuits exhibit the same reliability characteristics as other electronic devices in that the failure rate has three distinct phases:

1) Within a relatively short time after manufacture, certain failure mechanisms appear under moderate levels of stress. The faiure during this period is termed “infant mortality.”

2) After the period of infant mortality, failure rate falls dramatically and, for a long period, only infrequent random failures occur.

3) Finally, device packages can actually wear out and the failure rate will increase again.

When the failure rate for electronic components is plotted as a function of time, the result is a characteristic bathtub curve. While the bathtub shape is universal throughout the industry, actual values for a single component type can vary greatly from one manufacturer to another. Through many years of experience in the manufacture of integrated circuits, design rules and processing techniques have been developed to:

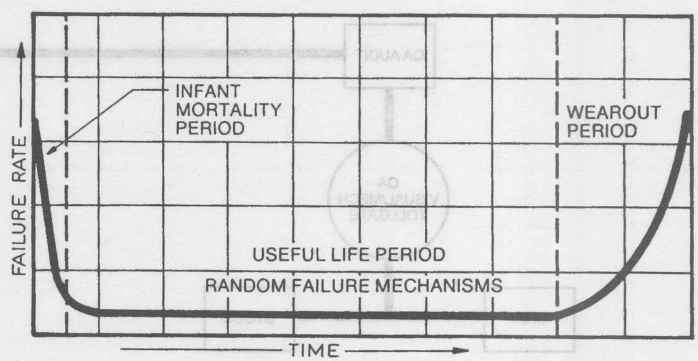
1) Minimize the infant mortality failure mechanisms.

2) Detect potential failures before they reach the customer.

3) Control wear-out so that operating life far exceeds the lifetime required by the customer.

RELIABILITY LIFE CYCLE

TYPICAL CURVE



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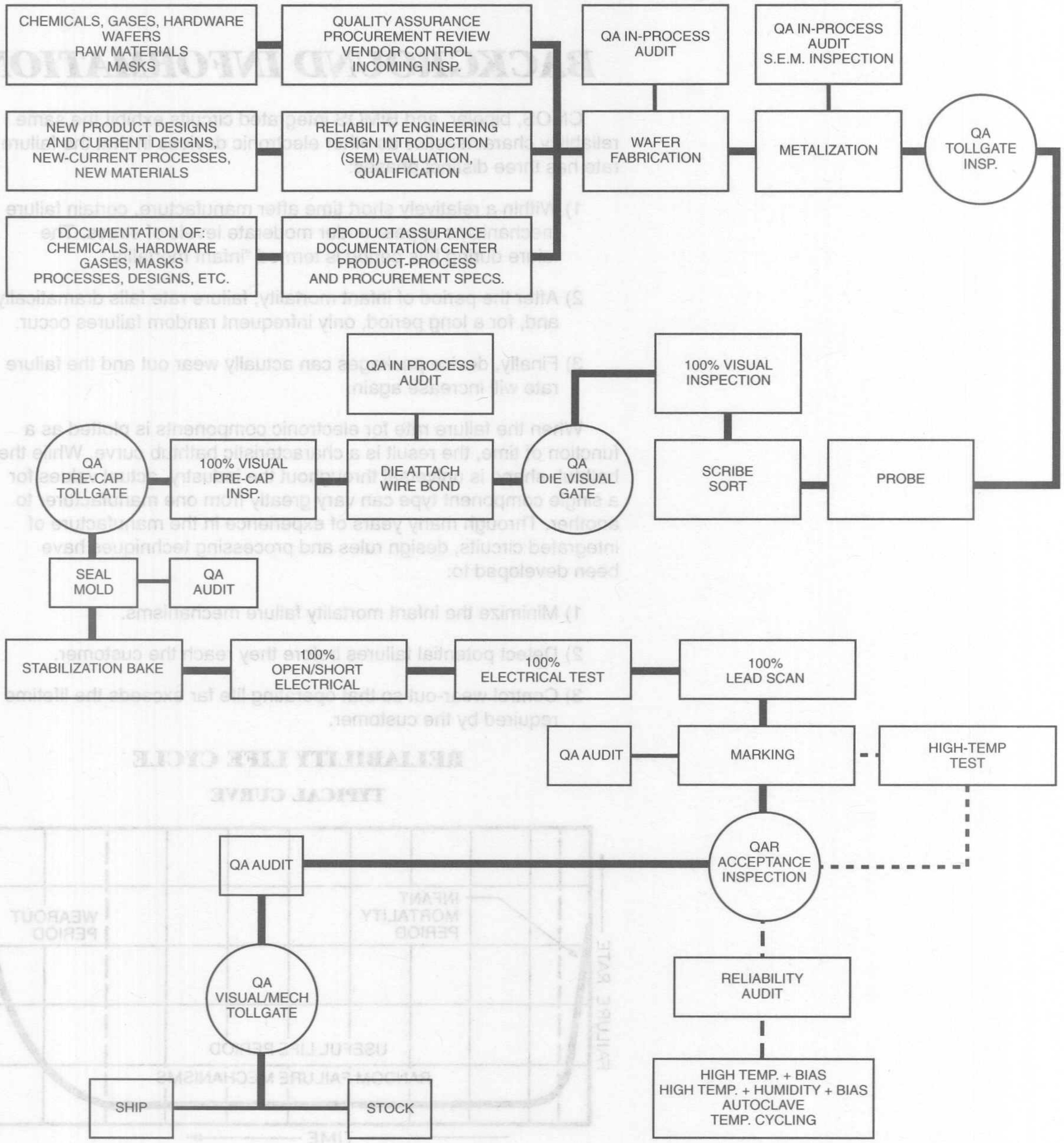
QUALITY ASSURANCE FLOW CHART



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PACE PRIMER

METHODOLOGY AND APPROACH FOR DEVELOPMENT

New products inherently require several functional groups working closely, and in parallel, to accomplish all the tasks necessary to complete a product development effort successfully and on schedule. These programs are typically small in number, high in impact, and require a detailed level of attention and focus in order to ensure their success. The methodologies and approaches for developing new products are referred to at Allegro as the PACE (Product And Cycle-time Excellence) Process.

Major product development efforts are undertaken by cross-functional teams of key individuals who have full responsibility for the product's success. With increasing levels of product complexity, many disciplines are required to contribute to a given development effort in order for it to succeed. Communication and coordination of these efforts can be as difficult as the execution of any of the many tasks involved.

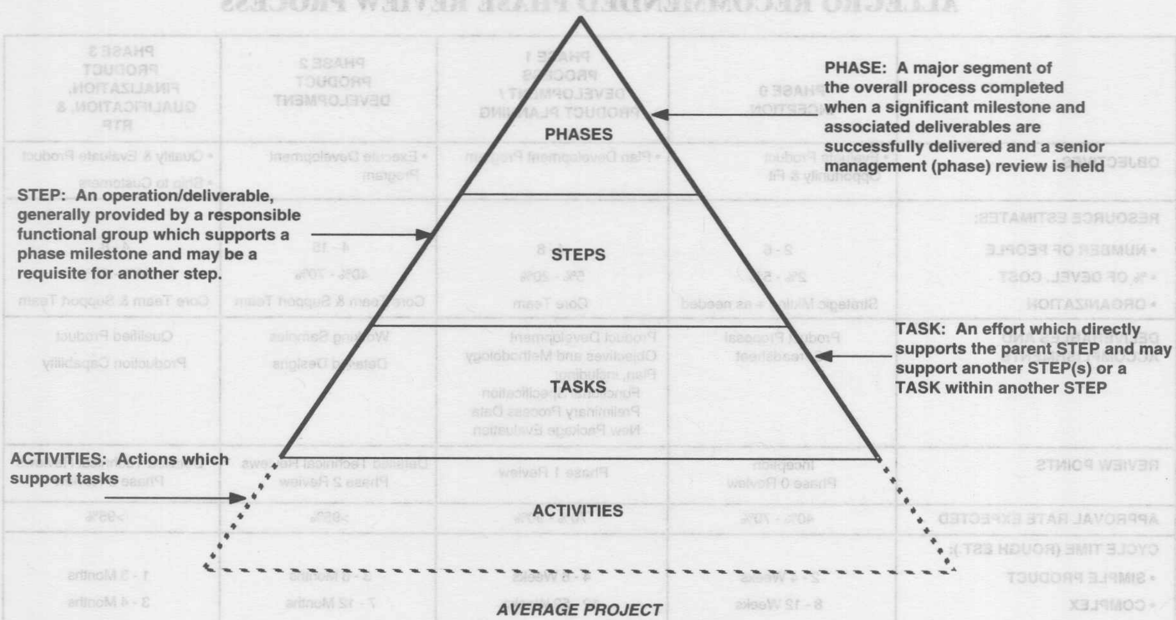
The PACE process is based upon seven key concepts:

1. The structured development process
2. The phase review process
3. The Product/Project Approval Committee (PAC)
4. The development organization
5. The planning process
6. The technical requirements
7. The documentation requirements

EXHIBIT 1

PRODUCT DEVELOPMENT PROCESS REVIEW

Phases, Steps, and Tasks



Dwg. OA-009

THE STRUCTURED DEVELOPMENT PROCESS

Structuring the development process establishes a framework for continuity and comparison between programs. This structure establishes specific phases, steps, tasks, and expectations for each product or process development program. This structure assures that each program proceeds through similar checkpoints, and that at each checkpoint, specific tasks have been completed.

THE PHASE REVIEW PROCESS

The structure of the Allegro phase review process contains four phases and their associated steps. This phase review process is the most important element of the development process. The four phases for a product development program are:

Phase 0	Product Inception
Phase 1	Product Development Planning
Phase 2	Product Development
Phase 3	Product Finalization, Qualification, and Release to Production

There are three types of programs within Allegro's development process:

PACE	These programs adhere rigidly to the phase review process
Mini-PACE	These programs adhere to all of the PACE requirements but are not obligated to hold reviews with the PAC beyond the Phase 1 approval
Action Plan	These programs utilize the PACE guidelines and process but do not require phase reviews with the PAC

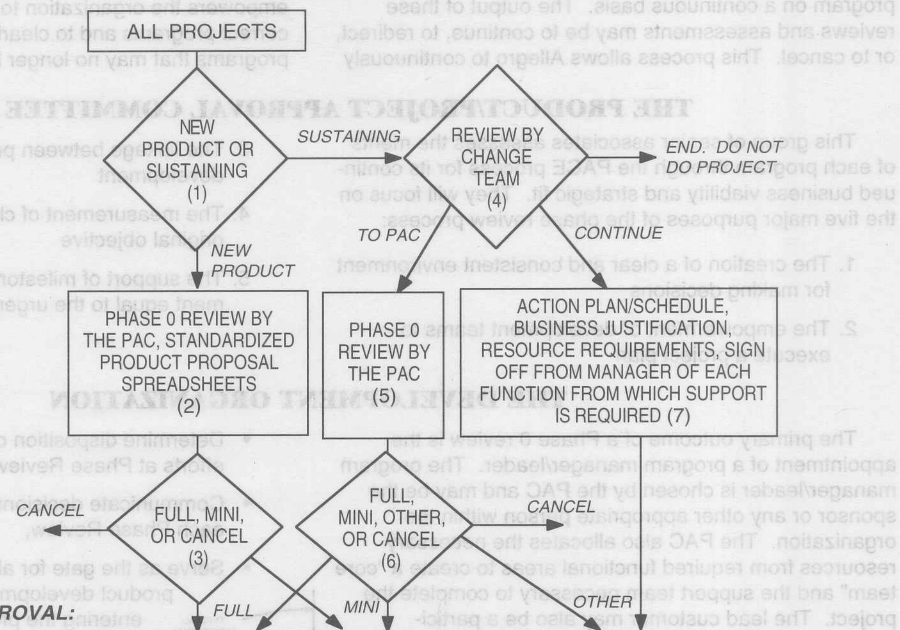
EXHIBIT 2
ALLEGRO RECOMMENDED PHASE REVIEW PROCESS

	PHASE 0 INCEPTION	PHASE 1 PROCESS DEVELOPMENT / PRODUCT PLANNING	PHASE 2 PRODUCT DEVELOPMENT	PHASE 3 PRODUCT FINALIZATION, QUALIFICATION, & RTP
OBJECTIVES	• Evaluate Product Opportunity & Fit	• Plan Development Program	• Execute Development Program	• Qualify & Evaluate Product • Ship to Customers
RESOURCE ESTIMATES:				
• NUMBER OF PEOPLE	2 - 6	4 - 8	4 - 15	4 - 8
• % OF DEVEL. COST	2% - 5%	5% - 20%	40% - 70%	10% - 20%
• ORGANIZATION	Strategic Mkting + as needed	Core Team	Core Team & Support Team	Core Team & Support Team
DELIVERABLES AND ACCOMPLISHMENTS	Product Proposal Spreadsheet	Product Development Objectives and Methodology Plan, including: Functional Specification Preliminary Process Data New Package Evaluation	Working Samples Detailed Designs	Qualified Product Production Capability
REVIEW POINTS	Inception Phase 0 Review	Phase 1 Review	Detailed Technical Reviews Phase 2 Review	Detailed Technical Reviews Phase 3 Review
APPROVAL RATE EXPECTED	40% - 70%	70% - 90%	>95%	>95%
CYCLE TIME (ROUGH EST.):				
• SIMPLE PRODUCT	2 - 4 Weeks	4 - 6 Weeks	3 - 6 Months	1 - 3 Months
• COMPLEX	8 - 12 Weeks	12 - 52 Weeks	7 - 12 Months	3 - 4 Months

Dwg. OA-010

EXHIBIT 3

PACE, Mini-PACE, AND ACTION PLAN BASED PROJECTS



	PACE PROGRAM (8)	MINI-PACE PROGRAM (9)	ACTION PLAN BASED PROGRAM (10)
PROJECT LEADER	PROGRAM MANAGER	PROGRAM LEADER	TEAM LEADER
PHASE 1 REQUIREMENTS	PRODUCT DEVELOPMENT OBJECTIVES AND METHODOLOGY (PHASE 1 DELIVERABLE)	SCHEDULE, SPEC AND TRACKING SHEET AT ABRIDGED PHASE 1	ACTION PLAN
TEAM REQUIREMENTS	FULL CORE TEAM	CORE TEAM	PROJECT TEAM
PROGRESS REVIEWS	REVIEWS BY PAC	PHASE 0, ABRIDGED PHASE 1 BY PAC, ALL COMMENSURATE REVIEWS BY FUNCTIONAL MANAGERS. RETURNS TO PAC IF TRACKING SHEET TOLERANCES ARE VIOLATED	FUNCTIONAL MANAGERS MONTHLY REPORTS
SCHEDULING	TEMPLATE-BASED SCHEDULE; ACTUAL vs. PLANNED REPORTING	TEMPLATE-BASED SCHEDULE; ACTUAL vs. PLANNED REPORTING	TEMPLATE-BASED SCHEDULE; ACTUAL vs. PLANNED REPORTING

Dwg. OA-011

The key point of the phase review process is that it allows the team, the PAC, and any other pertinent members of the organization to assess the merits of each program on a continuous basis. The output of these reviews and assessments may be to continue, to redirect, or to cancel. This process allows Allegro to continuously refine its development process and assure that its priorities and resource allocations are consistent with Allegro's strategic mission and vision. The phase review process empowers the organization to focus intensely on the correct programs and to clearly discontinue those programs that may no longer be appropriate.

THE PRODUCT/PROJECT APPROVAL COMMITTEE (PAC)

This group of senior associates assesses the merits of each program through the PACE process for its continued business viability and strategic fit. They will focus on the five major purposes of the phase review process:

1. The creation of a clear and consistent environment for making decisions
2. The empowerment of development teams to execute a project plan
3. The linkage between product strategy and product development
4. The measurement of clear checkpoints towards the original objective
5. The support of milestones that emphasize commitment equal to the urgency

THE DEVELOPMENT ORGANIZATION

The primary outcome of a Phase 0 review is the appointment of a program manager/leader. The program manager/leader is chosen by the PAC and may be the sponsor or any other appropriate person within the organization. The PAC also allocates the necessary resources from required functional areas to create a "core team" and the support team necessary to complete the project. The lead customer may also be a participant on a development team as a member of the support team. See Exhibit 4.

The roles and responsibilities of the Product Approval Committee are to:

- Provide a clear and consistent process for making major decisions on new products and enhancements,
- Empower Core Teams to execute product development efforts,
- Link product development efforts with overall corporate strategy and communicate linkage to organization,
- Determine disposition of product development efforts at Phase Reviews,
- Communicate decisions within one work day of each Phase Review,
- Serve as the gate for all new product development efforts entering the product development pipeline,
- Make resource allocation decisions,
- Establish priorities among new product development efforts,
- Contribute to the continuous improvement of the Allegro PACE Process,
- Ensure that the organization adheres to the policies and procedures set forth by the Allegro PACE Process, and
- Support customer requirements.

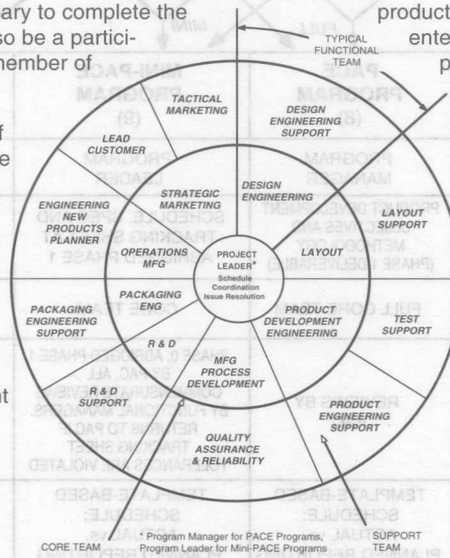


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EXHIBIT 4

EXAMPLE OF A DEVELOPMENT TEAM

The PAC is the senior group of managers who set and monitor the overall strategic direction of the company. The PAC members attend all Phase Reviews, and are responsible for ensuring that products allowed into the product development pipeline are consistent with the overall strategic direction of the company. In addition, the PAC must allocate the appropriate resources to each product development effort, and make changes to these resources as appropriate. The PAC also has the responsibility of providing advice, guidance, and support to the Core Teams when asked.

All team members are equally responsible for assuring the success of the program. Their roles and responsibilities are as follows:

The responsibilities of the Program Manager or Program Leader are to:

- Act as product champion,
- Act as team leader, builder, and motivator,
- Be responsible for monitoring overall cost and schedule of the program,
- Be responsible for assuring that overall product quality and technical performance goals are achieved,
- Negotiate with functional management for initial resources on the Core Team and any necessary changes to the Core Team membership,
- Coordinate and authorize project activities and information,
- Provide status to all levels of management, the customer, Core Team, and Support Team on a regular basis,
- Review all deliverables,
- Chair the regularly scheduled Core Team meetings and ensures timely distribution of the meeting minutes,
- Coordinate scheduling of and preparation for Phase Reviews,
- Be responsible for encouraging information exchange within the Core Team,
- Be responsible for problem resolution within the Core Team,
- Be responsible for coordinating any scenario analyses required by the PAC,
- Maintain project history (Product Development Notebook), and
- Support customer requirements.

The role of the Program Manager/Leader is to lead, manage, and drive the entire development project. He or she is the leader of the Development Team, which is responsible for the overall success of the product development effort, and must do everything possible to ensure this success. In this leadership role, the Program Manager/Leader must work with other members of the organization (including Core Team members) to ensure that appropriate resources are applied to the project in a timely fashion.

The responsibilities of the Core Team Members are to:

- Act as product champions,
- Work with Development Team members,
- Prepare and manage functional area schedule and contribute to overall schedule,
- Actively participate in Core Team meetings,
- Represent the Core Team to functional group,
- Work with other Core Team members to ensure that members' functional objectives are integrated into overall project design,
- Prepare and present appropriate sections of Phase Review presentations (this is done at the Program Manager/Leader's request),
- Report problem areas and potential schedule slips to the Core Team and/or Program Manager/Leader **before** they become critical,
- Ensure that all functional area rules and guidelines are adhered to (such as design rules, testing standards, customer commitment policies, etc.),
- Ensure overall product quality and performance,
- Support Program Manager/Leader in maintaining project history for Product Development Notebook,
- Support customer requirements, and
- Complete assigned tasks.

Core Team members are responsible for the inputs and activities required by the development effort. This includes communicating the progress and requirements of the project to their functional areas, as well as directly managing Development Team members from their area. Because each Core Team member is a member of the Development Team (see Exhibit 4), he/she is responsible for the success of the product development effort.

The responsibilities of the Support Team Members are to:

- Work with the Core Team members on requirements of the product development effort,
- Attend Core Team meetings at the request of the Core Team member from their functional area or from the Program Manager/Leader,
- Contribute to the overall flow of communication regarding the product development effort,
- Participate in Technical Reviews where appropriate,
- Assist Core Team representative in developing the program schedule,
- Understand the tasks and activities that need to be accomplished in the functional area,
- Support Core Team members in maintaining project history for Product Development Notebook,
- Support customer requirements, and
- Complete assigned tasks.

The Support Team members are not generally active participants in Core Team meetings, but attend these meetings on an invited basis only. Working through Core Team members, these individuals are responsible for the many day-to-day activities required for the successful execution of a product development effort.

THE PLANNING PROCESS

A critical premise of PACE is an emphasis on the planning process during Phase 1. Dedicating time up front is essential to a program's success by assuring that all potential critical issues are considered and resolved and that any areas of uncertainty are understood. It is expected that no detailed development work occurs during this phase. The planning phase is the preparation for Phase 2 development.

THE TECHNICAL REQUiREMENTS

Phase 2, the product development or execution phase, contains a series of required technical reviews to assure clear understanding and consensus among all functional areas necessary to ensure success of the project. These reviews are typically design, layout, process, and silicon oriented. The results of these reviews form part of the program's development history and are intended to move the program toward first-pass success.

THE DOCUMENTATION REQUIREMENTS

Each program is fully documented by a project notebook containing the minutes of meetings, the schedule, the results of the technical reviews, and any other pertinent information and data.

Checklists are provided as part of the PACE methodology for each step in the product development process to ensure that each program follows a consistent set of guidelines. The deliverables outlined by these checklists must be completed before a program can continue.

GENERAL INFORMATION & PRODUCT INDEX 1

PRODUCT SELECTION GUIDES 2

TECHNICAL DATA & APPLICATION NOTES FOR PERIPHERAL POWER DRIVER ICs 3

TECHNICAL DATA & APPLICATION NOTES FOR HALL-EFFECT SENSOR ICs 4

TECHNICAL DATA FOR AUTOMOTIVE POWER & SIGNAL-PROCESSING ICs 5

TECHNICAL DATA FOR POWER CONVERSION / POWER MANAGEMENT ICs 6

TECHNICAL DATA FOR SAFETY & SECURITY ICs 7

TECHNICAL DATA FOR DISCRETE TRANSISTORS, DIODES, AND ARRAYS 8

PACKAGE INFORMATION 9

SECTION 2. PRODUCT SELECTION GUIDES

SELECTION GUIDE

PERIPHERAL POWER DRIVER ICs

(Section 3, unless otherwise indicated)

IN ORDER OF 1) OUTPUT CURRENT, 2) OUTPUT VOLTAGE, 3) NUMBER OF DRIVERS

Output Ratings *			Features					
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	Part Number †
SINK DRIVERS								
100	20	8	–	–	–	X	–	2595
	30	32	X	X	–	–	–	5833
	40	32	X	X	–	X	–	5832
250	150	7	–	–	X	–	–	7003
300	45	1	Hall Sensor/Driver		X	–	X	5140 ‡
	50	8	–	–	X	X	–	2596
	60	2	Hall Sensor/Driver		–	X	–	5275 ‡
	80	2	–	–	X	X	–	5713
	80	4	–	–	X	X	–	5703 and 5706 §
350	50	4	–	X	X	–	–	5800
	50	8	–	X	X	–	–	5801
	50	8	X	X	–	–	–	5821
	50	8	X	X	X	–	–	5841
	80	8	X	X	X	–	–	5842
450	30	28	Dual 4 to 14-Line Decoder/Driver			–	–	5817
600	60	4	–	–	X	X	X	2547 §
	60	4	–	–	X	X	X	2549 §
700	60	4	–	–	X	X	X	2543 §
750	50	8	–	–	X	X	–	2597
900	14	2	Hall Sensor/Driver		X	X	X	3625 ‡
	26	2	Hall Sensor/Driver		X	X	X	3626 ‡
1250	50	4	Stepper Motor Translator/Driver			–	X	5804
	50	4	–	–	X	–	–	2064 and 2068
1500	80	4	–	–	X	–	–	2065 and 2069
1600	50	9	X	X	–	–	X	5829
1800	50	4	–	–	X	–	–	2544
	50	4	–	–	X	–	–	2540
4000	50	4	–	–	X	–	–	2878
	80	4	–	–	X	–	–	2879

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall-Effect sensor; Section 4.

§ Automotive Power & Signal-Processing IC; Section 5.

Output Ratings *			Features					
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	Part Number †
SOURCE DRIVERS								
-25	60	8	–	X	–	–	–	5815
	60	10	X	X	Active Pull-Down	–	–	5810-F (also §)
	60	12	X	X	–	–	–	5811
	60	20	X	X	Active Pull-Down	–	–	5812-F (also §)
	60	32	X	X	Active Pull-Down	–	–	5818-F (also §)
	80	10	X	X	Active Pull-Down	–	–	5810-F-1
	85	8	–	–	–	–	–	6118
-120	-25	8	–	–	X	X	–	2585
	30	8	–	–	X	X	–	2985
	50	8	X	X	X	X	–	5895
-350	35	8	–	–	X	–	X	2987
	50	8	–	–	X	–	–	2981 and 2982
	50	8	X	X	X	–	–	5891
	-50	8	–	–	X	–	–	2580 and 2588
	-80	8	–	–	X	–	–	2588-1
	80	8	–	–	X	–	–	2983 and 2984
	80	8	X	X	X	–	–	5890
-4000	60	4	–	–	X	–	–	2944
SOURCE / SINK DRIVERS								
±350	7.0	2	Voice-Coil Motor Driver		–	NMOS	X	8980
±500	6.0	2	Voice-Coil Motor Driver		–	CMOS	X	8932-A
	30	4	Dual Full Bridge		X	–	–	2993
±750	45	4	Dual PWM Full Bridge		X	–	X	2916
	45	4	Dual PWM Full Bridge		X	–	X	2919
±800	30	4	Dual PWM Full Bridge		X	–	X	3962
	45	4	Dual PWM Full Bridge		X	–	X	3961
±900	14	3	3-Ø Back-EMF Controller/Driver			DMOS	X	8902-A
±1000	7.0	3	3-Ø Back-EMF Controller/Driver			NMOS	X	8980 and 8983
	24	1	Half Bridge		X	–	X	2943 §
±1300	50	2	PWM Full Bridge		X	–	X	3953
±1500	45	4	Dual PWM Full Bridge		X	–	X	2917
	45	4	Dual PWM Full Bridge		X	–	X	2918
±2000	45	3	3-Ø Brushless Controller/Driver			–	X	2936 and 2936-120
	50	4	Dual Full Bridge		X	–	X	2998
	50	4	PWM Full Bridge		X	–	X	3952
±3000	45	2	PWM Control		X	–	X	2962
±3400	45	1	PWM Control		X	–	X	2961
±4000	14	3	3-Ø Brushless Controller/Driver			DMOS	X	8925

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall-Effect sensor; Section 4.

§ Automotive Power & Signal-Processing IC; Section 5.

SELECTION GUIDE

HIGH-VOLTAGE PERIPHERAL POWER AND DISPLAY DRIVERS

(Section 3, unless otherwise indicated)

IN ORDER OF 1) OUTPUT VOLTAGE, 1) OUTPUT CURRENT, 3) NUMBER OF DRIVERS

Output Ratings*			Features					
V	mA	#	Serial Input	Latched Drivers	Diode Clamp	Saturated Outputs	Internal Protection	Part Number †
60	-25	8	–	X	–	–	–	5815
	-25	10	X	X	Active Pull-Down	–	–	5810-F (also §)
	-25	12	X	X	–	–	–	5811
	-25	20	X	X	Active Pull-Down	–	–	5812-F (also §)
	-25	32	X	X	Active Pull-Down	–	–	5818-F (also §)
	300	2	Hall Sensor/Driver		–	X	–	5275 ‡
	600	4	–	–	–	X	X	2547 §
	600	4	–	–	X	X	X	2549 §
	700	4	–	–	X	X	X	2543 §
	4000	4	–	–	X	–	–	2944
80	-25	10	X	X	Active Pull-Down	–	–	5810-F-1
	300	2	–	–	–	X	X	5713
	300	4	–	–	–	X	X	5703 and 5706§
	-350	8	–	–	X	–	–	2983 and 2984
	350	8	–	X	X	X	–	5842
	-350	8	X	X	X	–	–	5890
	1500	4	–	–	–	X	–	2065 and 2069
	4000	4	–	–	X	–	–	2879
-80	-350	8	–	–	X	–	–	2588-1
85	-25	8	–	–	–	–	–	6118
150	250	7	–	–	X	–	–	7003

* Current is maximum test condition; voltage is absolute maximum allowable.
Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Hall-Effect sensor; Section 4.

§ Automotive Power & Signal-Processing IC; Section 5.

BiMOS INTELLIGENT POWER INTERFACE DRIVERS

(Section 3, unless otherwise indicated)

	Output Ratings *		Part Number †
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	50 V‡	5841
8-Bit	-350 mA	50 V‡	5891
8-Bit	350 mA	80 V‡	5842
8-Bit	-350 mA	80 V‡	5890
9-Bit	1.6 A	50 V	5829
10-Bit (active pull-downs)	-25 mA	60 V	5810-F (also §)
10-Bit (active pull-downs)	-25 mA	80 V	5810-F-1
12-Bit	-25 mA	60 V	5811
20-Bit (active pull-downs)	-25 mA	60 V	5812-F (also §)
32-Bit (active pull-downs)	-25 mA	60 V	5818-F (also §)
32-Bit	100 mA	30 V	5833
32-Bit	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
Dual 8-Bit With Read Back	25 mA	20 V‡	5881
SPECIAL-PURPOSE FUNCTIONS			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 28-Line Decoder/Driver	450 mA	30 V	5817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

§ Automotive Power & Signal-Processing IC; Section 5.

SELECTION GUIDE

MOTOR DRIVERS

(Sections 3, 4, and 5)

Function	Output Ratings *		Part Number †	Detailed Info Section
INTEGRATED CIRCUITS FOR BRUSHLESS DC MOTORS				
3-Phase Controller/Drivers	±2.0 A	45 V	2936 and 2936-120	3
Hall-Effect Latched Sensors	10 mA	24 V	3175 and 3177	4
2-Phase Hall-Effect Sensor/Controller	20 mA	25 V	3235	4
Hall-Effect Complementary Output Sensor	20 mA	25 V	3275	4
2-Phase Hall-Effect Sensor/Driver	900 mA	14 V	3625	4
2-Phase Hall-Effect Sensor/Driver	900 mA	26 V	3626	4
Hall-Effect Comp. Output Sensor/Driver	300 mA	60 V	5275	4
3-Phase Back-EMF Controller/Driver	±900 mA	14 V	8902–A	3
3-Phase Controller/DMOS Driver	±4.0 A	14 V	8925	3
3-Phase Back-EMF Controller/Driver	±1.0 A	7 V	8980 and 8983	3
BRIDGE DRIVERS FOR DC AND BIPOLAR STEPPER MOTORS				
PWM Current Controlled Dual Full Bridge	±750 mA	45 V	2916	3
PWM Current Controlled Dual Full Bridge	±1.5 A	45 V	2917	3
PWM Current Controlled Dual Full Bridge	±1.5 A	45 V	2918	3
PWM Current Controlled Dual Full Bridge	±750 mA	45 V	2919	3
Half-Bridge Driver	±1.0 A	24 V	2943	5
Dual Full Bridge	±500 mA	30 V	2993	3
Dual Full Bridge	±2.0 A	50 V	2998	3
PWM Current Controlled Full Bridge	±2.0 A	50 V	3952	3
PWM Current Controlled Full Bridge	±1.3 A	50 V	3953	3
PWM Current Controlled Dual Full Bridge	±800 mA	45 V	3961	3
PWM Current Controlled Dual Full Bridge	±800 mA	30 V	3962	3
OTHER MOTOR DRIVERS				
Unipolar Stepper Motor Quad Driver	1.8 A	50 V	2544	3
Unipolar Stepper-Motor Translator/Driver	1.25 A	50 V	5804	3
Voice-Coil Motor Driver	±500 mA	6 V	8932-A	3
Voice-Coil Motor Driver	±800 mA	16 V	8958	3
Voice-Coil Motor Driver	±350 mA	7 V	8980 and 8983	3

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

SELECTION GUIDE

HALL-EFFECT SENSORS

(Section 4)

Partial Type Number	Avail. Op. Temp.	Operate Limits Over Temp. B_{OP}max	B_{RP}min	B_{hys}min	Function†	Notes
3046	E/L	+200	-200	15	Gear-Tooth Sensor	
3054	K/S	+300	+5	5.0	Unipolar Multiplex	1
3056	E/L	+225	-225	15	Gear-Tooth Sensor	
3058	E/L	+300	-300	150	Gear-Tooth Sensor	
3059	K/S	+100	-100	20	AC Gear-Tooth Sensor	
3121	E/L	+500	+80	60	Unipolar Switch	
3122	E/L	+430	+120	70	Unipolar Switch	
3123	E/L	+470	+160	70	Unipolar Switch	
3132	K/S	+95	-95	30	Bipolar Switch	
3133	K/S	+75	-75	30	Bipolar Switch	
3134	E/L	+50	-40	10	Bipolar Switch	
3141	E/L	+175	+10	20	Unipolar Switch	
3142	E/L	+245	+60	30	Unipolar Switch	
3143	E/L	+355	+150	30	Unipolar Switch	
3144	E/L	+450	+25	20	Unipolar Switch	
3175	S	+180	-180	80	Bipolar Latch	
3177	S	+150	-150	50	Bipolar Latch	
3185	E/L	+300	-300	280	Bipolar Latch	
3186	E/L	+350	-350	100	Bipolar Latch	
3187	E/L	+175	-175	100	Bipolar Latch	
3188	E/L	+200	-200	160	Bipolar Latch	
3189	E/L	+250	-250	100	Bipolar Latch	
3195	E/L	+200	-200	110	Bipolar Latch	2, 3
3197	E/L	+200	-200	80	Bipolar Latch	3
3235	S	+200	+15	15	Unipolar Switch	4
		-200	-15	15	Unipolar Switch	
3275	S	+250	-250	100	Bipolar Latch	5
3503	S	Typ. 1.3mV/G		–	Linear Sensor	
3506	L	Typ. 2.5mV/G		–	Linear Sensor	
3507	E/L	Typ. 2.5 mV/G		–	Linear Sensor	
3508	S	Typ. 2.5 mV/G		–	Linear Sensor	
3625	S	+150	-150	200*	900 mA Bipolar Latch	3, 5, 6
3626	S	+150	-150	200*	400 mA Bipolar Latch	3, 5, 6
5140	E	+240	+25	20	300 mA Unipolar Switch	3, 6
5275	S	+250	-250	100	300 mA Bipolar Latch	5, 6

Operating Temperature Ranges:
C = 0°C to +70°C, S = -20°C to +85°C, E = -40°C to +85°C, K = -40°C to +125°C, L = -40°C to +150°C

Notes 1. Multiplexed two-wire sensor; after proper address, power/signal bus current indicates magnetic field condition.
2. Active pull down.
3. Protected.
4. Output 1 switches on south pole, output 2 switches on north pole for 2-phase, bifilar-wound, unipolar-driven brushless dc motor control.
5. Complementary outputs for 2-phase bifilar-wound, unipolar-driven brushless dc motor control.
6. Power driver output.
* Typical.
† Latches will not switch on removal of magnetic field; bipolar switches may switch on removal of field but require field reversal for operation over operating temp. range.

AUTOMOTIVE POWER & SIGNAL-PROCESSING ICs

EXTENDED TEMPERATURE DEVICES SUITABLE FOR AUTOMOTIVE APPLICATIONS

Part Number *	Function	Detailed Info Section
2064, 2065, 2068, & 2069	1.5 A Darlington Switches	3
2429	Fluid (Low-Coolant) Detector	5
2436	Countdown Power Timer (Rear-Window Defogger)	5
2454 & 2455	Lamp Monitors	5
2460	Electronic Ignition Timing	5
2540	Quad Power Driver	3
2543	Protected Quad Power Driver	5
2544	Protected Quad Power Driver	3
2547, 2549, & 2559	Protected Quad Power Drivers	5
2595. 2596, & 2597	8-Channel Saturated Sink Drivers	3
2916, 2917, & 2918	Dual Full-Bridge PWM Motor Drivers	3
2936	3-Phase Brushless DC Motor Controller/Driver	3
2943	High-Current Half-Bridge Motor Driver	5
2982, 2984, & 2987	8-Channel Source Drivers	3
2993 & 2998	Dual H-Bridge Motor Drivers	3
3046, 3056, & 3058	Hall-Effect Gear-Tooth Sensors - Zero Speed	4
3054	Multiplexed Two-Wire Hall-Effect Sensor	4
3059 & 3060	Hall-Effect Gear-Tooth Sensors - AC Coupled	4
3121, 3122, & 3123	Hall-Effect Switches	4
3132 & 3133	Ultra-Sensitive Bipolar Hall-Effect Switches	4
3134	Bipolar Hall-Effect Switch	4
3141, 3142, 3143, & 3144	Sensitive Hall-Effect Switches	4
3185 thru 3189	Hall-Effect Latches	4
3195	Protected Hall-Effect Latch with Active Pull-Down	4
3197	Protected, Open-Collector Hall-Effect Latch	4
3506 thru 3508	Ratiometric, Linear Hall-Effect Sensors	4
3828	FM Stereo Decoder	5
3841	AM Signal Processor	5
3845 & 3846	AM Noise Blankers	5
3848	Dual-Conversion AM Receiver	5
3952 & 3953	Full-Bridge PWM Motor Driver	3
3961 & 3962	Dual Full-Bridge PWM Motor Drivers	3
5140	Protected PowerHall Sensor - Lamp/Solenoid Driver	4
5703 & 5706	Quad 2-Input Peripheral/Power Drivers	5
5800 & 5801	BiMOS II Latched Drivers	3
5810-F	BiMOS II 10-Bit Serial-Input, Latched Source Driver	5
5811	BiMOS II 12-Bit Serial-Input, Latched Source Driver	5
5812-F	BiMOS II 20-Bit Serial-Input, Latched Source Driver	5
5818-F	BiMOS II 32-Bit Serial-Input, Latched Source Driver	5
5821	BiMOS II 8-Bit Serial-Input, Latched Driver	3
5832	BiMOS II 32-Bit Serial-Input, Latched Driver	3
5841 & 5842	BiMOS II 8-Bit Serial-Input, Latched Drivers	3
6118	Fluorescent Display Driver	3

* Complete part number includes additional characters to indicate operating temperature range and package style.

LINEAR INTEGRATED CIRCUITS FOR RADIO APPLICATIONS (Detailed Information in Section 5)

Part Number *	Inputs	Function	Supply Voltage Range
3718	Audio	Low-Voltage Audio Power Amplifier	1.8-9 V
3828	Composite Audio	FM Stereo Decoder w/Noise-Actuated Blend	8.5-12 V
3841	to 30 MHz	AM Signal Processor	7-16 V
3845	to 30 MHz	AM Stereo Noise Blanker	7.5-12 V
3846	to 30 MHz	AM Noise Blanker	7.5-12 V
3848	to 30 MHz	Dual-Conversion AM Receiver	7.5-16 V

* Complete part number includes additional characters to indicate operating temperature range and package style.

SPECIALIZED DEVICES FOR CONSUMER APPLICATIONS

Part Number *	Function	Detailed Info Section
2429	Fluid Detector	5
2436	Countdown Power Timer	5
2454 & 2455	Quad Comparators	5
3056 thru 3061	Hall-Effect Gear-Tooth Sensor	4
5347 & 5348	Ionization-Type Smoke Detector	7
5349 & 5350	Ionization-Type Smoke Detector with Interconnect and Timer	7
5358	Photoelectric-Type Smoke Detector with Interconnect and Timer	7
8902–A	3-Phase Brushless DC Motor Controller/Driver w/Back-EMF Sensing	3
83145 & 84145	Latched, Universal Input-Voltage Switches	6

* Complete part number includes additional characters to indicate operating temperature range and package style.

OTHER ANALOG INTEGRATED CIRCUITS

Part Number *	Function	Detailed Info Section
3503 thru 3508	Ratiometric Linear Output Hall-Effect Sensors	4
3718	Low-Voltage Audio Power Amplifier	5
8131	Precision Supervisory Systems Monitor	6
8181	Low-Dropout, High-Efficiency, 5 V Regulator	6
8183 & 8184	Low-Dropout, High-Efficiency, 3 V Regulators	6
8186 & 8187	Low-Dropout, High-Efficiency, 3.3 V Regulators	6
8932-A	16 V, 250 mA Voice-Coil Motor Driver	3
8958	16 V, 800 mA Voice-Coil Motor Driver	3

* Complete part number includes additional characters to indicate operating temperature range and package style.

SELECTION GUIDE

DEVICES FOR MASS STORAGE APPLICATIONS

(Section 3)

Part Number*	Description
8902–A	5 V and 12 V 3-Phase Brushless DC Motor Controller/Driver with Back-EMF Sensing
8920	Dual Schottky Diode
8925	3-Phase Motor Controller/Driver with Linear Current Control and Power DMOS Outputs
8932–A	6 V, 600 mA Voice Coil Motor Driver
8958	16 V, 800 mA Voice Coil Motor Driver
8980	Spindle & Voice-Coil Actuation Manager/Driver
8983	Spindle & Voice-Coil Actuation Manaager/Driver

* Complete part number includes additional characters to indicate operating temperature range and package style.

DEVICES FOR PRINTER APPLICATIONS

(Section 3)

Part Number*	Description
2916	Dual 45 V, 750 mA Full-Bridge PWM Stepper Motor Driver
2917	Dual 45 V, 1.5 A Full-Bridge PWM Stepper Motor Driver
2918	Dual 45 V, 1.5 A Full-Bridge PWM Stepper Motor Driver
2919	Dual 45 V, 750 mA Full-Bridge PWM Stepper Motor Driver
2961	45 V, 3.4 A Solenoid Printhead Driver
2962	Dual 45 V, 3 A Solenoid Printhead Driver
3952	50 V, 2 A Full-Bridge PWM Stepper Motor Driver
3953	50V, 1.3 A Full-Bridge PWM Motor Driver
3961	Dual 45 V, 800 mA Full-Bridge PWM Stepper Motor Driver
3962	Dual 30 V, 800 mA Full-Bridge PWM Stepper Motor Driver
5817	Addressable 30 V, 450 mA 28-Line Ink-Jet Printer Decoder/Driver
5829	Serial-In 50 V, 1.6 A 9-Wire Solenoid Printhead Driver

* Complete part number includes additional characters to indicate operating temperature range and package style.

SELECTION GUIDE

POWER CONVERSION/POWER MANAGEMENT

LINEAR REGULATOR ICs

Part Number*	V_O	Max DC In	Max Dropout	Max I_O	Package
8181	5.0 V	10 V	300 mV @ 500 mA	1.0 A	16-lead SOIC
8183	3.0 V	10 V	300 mV @ 125 mA	250 mA	6-lead SOT-89
8184	3.0 V	10 V	300 mV @ 125 mA	250 mA	SOT-89
8186	3.3 V	10 V	300 mV @ 125 mA	250 mA	6-lead SOT-89
8187	3.3 V	10 V	300 mV @ 125 mA	250 mA	SOT-89

* Complete part number includes additional characters to indicate operating temperature range and package style.

CROSS REFERENCE

IN ALPHA-NUMERICAL ORDER

The suggested Allegro replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is not guaranteed and the user should compare the specifications of the competitive and recommended Allegro replacement. Special caution must be exercised in attempting to do a reverse cross. In some instances, the competitive device is obsolete; in many instances, the suggested Allegro device features improved performance or specifications.

Mfg Codes:

A	Allegro MicroSystems
AMI	American Microsystems
APX	Apex Microtechnology Corp.
ASAHI	Asahi
BELL	Bell
CS	Cherry Semiconductor
CSI	Concord Sensors, Inc
DI	Dionics, Inc.
EXR	Exar Integrated Systems
FER	Ferranti Limited
FSC	Fairchild Semiconductor
FUJ	Fujitsu
GE	General Electric*
HIT	Hitachi Ltd.
IP	Integrated Power
IR	International Rectifier*
ITT	ITT Semiconductors
LT	Linear Technology
MAL	P. R. Mallory*
MAT	Matsushita
MCRL	Micrel
MICR	Microswitch
MIT	Mitsubishi Electric Corp.
MOT	Motorola Semiconductor
MT	Mietec
NEC	Nippon Electric Co.
NS	National Semiconductor
OKI	Oki Semiconductor
OM	Omnirel
PE	Pro-Electron #
PLS	Plessey Semiconductor
RAY	Raytheon Co.*
RCA	RCA (Harris)
RFA	Rifa
SAM	Samsung Semiconductor
SANY	Sanyo
SG	Silicon General Inc.
SIEM	Siemens Corp.
SIG	Signetics Corp.
SIL	Siliconix
SGS	SGS-Thomson
SUPER	Supertex
SPC	Sprague Products Co.*
SPR	Sprague Electric Co.
SYL	Sylvania
THM	Thomson-CSF
TI	Texas Instruments
TLF	AEG-Telefunken
TOKO	RCL Toko
TOS	Toshiba Corp.
TRW	TRW
UNI	Unitrode

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Competitive Part Number				Suggested Allegro	
Prefix	Base Number	Suffix	Mfg Code(s)	Replacement	Notes
CA	3169		RCA	UDN2943Z	≈
CA	3219	AE	RCA	UDN2543B	
CA	3219	E	RCA	UDQ2543B	
CA	3242	E	RCA	UDN2543B	
CA	3262	AE	RCA	UDK2549B	
CA	3262	AQ	RCA	UDK2549EB	
CA	3262	E	RCA	UDN2543B	
CA	3262	Q	RCA	UDN2543EB	
CA	3272	AQ	RCA	UDK2547EB	
CA	3272	Q	RCA	UDK2547EB	
CS	166		CS	ULN2429A	
DI	514		DI	UDN6118A	≈
DN	6835		NS/MAT	UGN3503U	≈
DN	6836		NS/MAT	UGN3503U	≈
DN	6837		NS/MAT	A3121EU	
DN	6838		NS/MAT	UGN3132U	
DN	6839		NS/MAT	A3121EU	
DN	6851		MAT	UGN3132–	≈
ECG	2021		SYL	ULN6118A	
EW	500		ASAHI	UGN3175U	
EW	550		ASAHI	A3141E–	
EW	550		ASAHI	A3142E–	
FPQ	2222		FSC	TPQ2222A	
FPQ	2907		FSC	TPQ2907A	
FSA	2619	P	FSC	TND908	
FSA	2719	P	FSC	TND903	
HA	13007		HIT	UDN2540B	
HA	13415		HIT	UDN2543B	
HA	13421	A	HIT	UDN2993B	≈
HA	16617	P	HIT	UDN6118A	
HA	16617	PJ	HIT	UDQ6118A	
HV	6810	WG	SUPER	UCQ5810LWF-1	≈
IP	293	D	IP	ULN2993B	≈
IP	2064	N	IP	ULN2064B	
IP	2065	N	IP	ULN2065B	
IP	2068	N	IP	ULN2068B	
IP	2069	N	IP	ULN2069B	

Competitive Part Number				Suggested Allegro	
Prefix	Base Number	Suffix	Mfg Code(s)	Replacement	Notes
KA	2580	A	SAM	UDN2580A	
KA	2588	A	SAM	UDN2588A	
L	293	D	SGS/UNI	UDN2993B	≈
L	293		SGS	UDN2993B	≈
L	293	DNE	TI	UDN2993B	≈
L	295		SGS/UNI	UDN2962W	≈
L	298	D	SGS	UDN2998W	≈
L	298		SGS/UNI	UDN2998W	≈
L	6218		SGS	UDN2916B	≈
L	6219		SGS	UDN2916B	
L	6220		SGS	UDN2544B	
L	6221		SGS	UDN2540B	
L	6451		SGS	A5817SEP	
M	2064	P	MIT	ULN2064B	≈
M	2065	P	MIT	ULN2065B	
M	2580	P	MIT	UDN2580A	
M	2981	P	MIT	UDN2981A	
M	2982	P	MIT	UDN2982A	
M	2983	P	MIT	UDN2983A	
M	2984	P	MIT	UDN2984A	
M	54532	P	MIT	ULN2064B	≈
M	54562	P	MIT	UDN2982A	
M	54563	P	MIT	UDN2981A	
MC	1417	P	MOT	UDN2580A	
MC	1473	PI	MOT	UDN5713M	
MC	3479	P	MOT	UCN5804B	≈
MIC	5801	CN	MCRL	UCN5801A	
MIC	5821	CN	MCRL	UCN5821A	
MPQ	2222		MOT	TPQ2222A	
MPQ	2907		MOT	TPQ2907A	
MPQ	3904		MOT	TPQ3904	
MPQ	3906		MOT	TPQ3906	
MPQ	6502		MOT	TPQ6502	
MSL	912	R	OKI	UDN6118A	
MTC	6020		MT	UCN5801A	
NE	594	N	SIG	UDN6118A	
OH	360		TRW	A3121E–	

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Competitive Part Number				Suggested	
Prefix	Base Number	Suffix	Mfg Code(s)	Allegro Replacement	Notes
OHN	3013	U	TRW	A3121EU	
OHN	3019	U	TRW	A3121EU	
OHN	3020	U	TRW	A3121EU	
OHN	3030	U	TRW	UGN3132U	
OHN	3040	U	TRW	A3141EU	
OHN	3040	U	TRW	A3142EU	
OHS	3019	U	TRW	A3121LU	
OHS	3020	U	TRW	A3121LU	
OHS	3030	U	TRW	UGS3132U	
OHS	3040	U	TRW	A3141LU	
OHS	3040	U	TRW	A3142LU	
PBD	3517		RFA	UCN5804B	≈
PBL	3717		RFA	UDN2953B	≈
PBL	3770		RFA	UDN2953B	≈
Q2T	2222		TI	TPQ2222A	
S	4534		AMI	UCN5810AF	
SA	594	N	SIG	UDQ6118A	
SAA	1027		SIG/PE	UCN5804B	≈
SAA	1042		MOT/PE	UCN5804B	≈
SAS	251	S4	SIEM	UGN3275–	
SAS	251	S5	SIEM	A3121E–	
SG	298	D	SG	UDN2998W	≈
SG	2064	W	SG	ULN2064B	
SG	2065	W	SG	ULN2065B	
SG	2068	W	SG	ULN2068B	
SG	2069	W	SG	ULN2069B	
SG	3643	S	SG	UDN2962W	≈
SG	6118	N	SG	UDN6118A	
SN	65518	FN	TI	UCQ5818EPF	
SN	65518	N	TI	UCQ5818AF	
SN	75064	NE	TI	ULN2064B	
SN	75065	NE	TI	ULN2065B	
SN	75068	NE	TI	ULN2068B	
SN	75069	NE	TI	ULN2069B	
SN	75437	ANE	TI	UDN2543B	
SN	75478	P	TI	UDN5713M	–
SN	75512	BN	TI	UCN5811A	
SN	75518	FN	TI	UCN5818EPF	
SN	75518	N	TI	UCN5818AF	
SN	754410		TI	UDN2993B	≈
SN	754411		TI	UDN2993B	≈
SS	31	EA	MICR	UGS3132U	≈
SS	41		MICR	UGS3132UA	≈
SS	44	A	MICR	A3141L–	≈
SS	44	A	MICR	A3142L–	≈
SS	44	B	MICR	A3144LUA	≈
SS	46		MICR	A3185LUA	≈
SS	81	EA	MICR	UGN3132U	≈
SS	89	A1	MICR	UGN3503U	≈
TD	62064	AP	TOS	ULN2064B	
TD	62064	BP	TOS	ULN2065B	
TD	62064	F	TOS	ULN2064LB	
TD	62064	P	TOS	ULN2064B	
TD	62478	P	TOS	UDN5713M	
TD	62781	AP	TOS	UDN6118A	
TD	62783	AP	TOS	UDN2982A	
TDA	3717		PE	UDN2953B	≈
TEA	3717		PE	UDN2953B	≈
TID	121		TI	TND933	
TID	122		TI	TND940	
TL	170		TI	UGN3132U	≈
TL	172	C	TI	A3121EU	≈
TL	173	C	TI	UGN3503U	≈
TL	173	I	TI	UGN3503U	≈
TL	175	C	TI	UGN3176U	
TL	3013		TI	A3121EUA	
TL	3019		TI	A3121EUA	
TL	3020		TI	A3144EUA	
TL	4810	ADW	TI	UCN5810LWF	≈
TL	4810	AIDW	TI	UCQ5810LWF	≈
TL	4810	AIN	TI	UCQ5810AF	
TL	4810	AN	TI	UCN5810AF	
TL	4810	BDW	TI	UCN5810LWF	≈
TL	4810	BIDW	TI	UCQ5810LWF	≈

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CROSS REFERENCE
TL-UGS

Competitive Part Number				Suggested	
Prefix	Base Number	Suffix	Mfg Code(s)	Allegro Replacement	Notes
TL	4810	BIN	TI	UCQ5810AF	
TL	4810	BN	TI	UCN5810AF	
TL	5812	FN	TI	UCN5812EPF	
TL	5812	IFN	TI	UCQ5812EPF	
TL	5812	IN	TI	UCQ5812AF	
TL	5812	N	TI	UCN5812AF	
TLE	4945	F	SIEM	UGN3132U	
TLE	4945	L	SIEM	UGN3132UA	
TPQ	2222		A/SPR	TPQ2222A	
TPQ	2907		A/SPR	TPQ2907A	
TYA	298		MOT/PE	ULQ2436M	
UC	3175		UNI	A8958CEA	
UC	3517		UNI	UCN5804B	≈
UC	3620		UNI	UDN2936W	≈
UC	3717	A	UNI	UDN2953B	≈
UC	3770		UNI	UDN2954W	≈
UCN	4202	A	SPR	UCN5804B	≈
UCN	4203	A	SPR	UCN5804B	≈
UCN	4204	B	SPR	UCN5804B	
UCN	4205	B-2	SPR	UCN5804B	
UCN	4401	A	SPR	UCN5800A	
UCN	4801	A	SPR	UCN5801A	
UCN	4801	ADP	THM	UCN5801A	
UCN	4810	A	SPR	UCN5810AF	
UCN	4810	N	TI	UCN5810AF	
UCN	4815	A	SPR	UCN5815A	
UCN	4821	A	SPR	UCN5821A	
UCN	5812	A	SPR	UCN5812AF	
UCN	5812	EP	SPR	UCN5812EPF	
UDN	2541	B	SPR	UDN2543B	≈
UDN	2542	B	SPR	UDN2543B	≈
UDN	2952	B	SPR	UDN2953B	≈
UDN	2952	W	SPR	UDN2954W	≈
UDN	2956	A	SPR	UDN2957A	≈
UDN	2975	W	SPR	UDN2962W	≈
UDN	5713	N	TI	UDN5713M	
UGN	3013	–	SPR	A3121E–	

Competitive Part Number				Suggested	
Prefix	Base Number	Suffix	Mfg Code(s)	Allegro Replacement	Notes
UGN	3019	–	SPR	A3121E–	
UGN	3020	–	SPR	A3121E–	
UGN	3030	–	SPR	UGN3132–	
UGN	3040	–	SPR	A3141E–	
UGN	3040	–	SPR	A3142E–	
UGN	3055	U	A/SPR	A3054SU	
UGN	3075	–	SPR	UGN3175–	
UGN	3076	–	SPR	UGN3177–	
UGN	3077	–	SPR	UGN3177–	
UGN	3113	–	A/SPR	A3121E–	
UGN	3119	–	A/SPR	A3121E–	
UGN	3120	–	A/SPR	A3144E–	
UGN	3130	–	A/SPR	UGN3132–	
UGN	3131	–	A/SPR	UGN3132–	
UGN	3140	–	A/SPR	A3141E–	
UGN	3140	–	A/SPR	A3142E–	
UGS	3140	–	A/SPR	A3141L–	
UGS	3140	–	A/SPR	A3142L–	
UGN	3176	–	SPR	UGN3177–	
UGN	3501	M	SPR	UGN.	≈
UGS	3019	–	SPR	A3121L–	
UGS	3020	–	SPR	A3144L–	
UGS	3030	–	SPR	UGS3132–	
UGS	3040	–	SPR	A3141L–	
UGS	3040	–	SPR	A3142L–	
UGS	3119	–	A/SPR	A3121L–	
UGS	3120	–	A/SPR	A3144L–	
UGS	3130	–	A/SPR	UGS3132–	
UGS	3131	–	A/SPR	UGS3132–	
UGS	3140	–	A/SPR	A3141L–	
UGS	3140	–	A/SPR	A3142L–	
UHP	402	-1	SPR	UDN5703A	≈
UHP	402		SPR	UDN5703A	≈
UHP	403	-1	SPR	UDN5703A	≈
UHP	403		SPR	UDN5703A	≈
ULN	2064	B	MOT/SGS	ULN2064B	
ULN	2064	N	IP	ULN2064B	

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CROSS REFERENCE
UHP-XR

Competitive Part Number				Suggested Allegro	
Prefix	Base Number	Suffix	Mfg Code(s)	Replacement	Notes
ULN	2064	NE	MOT/TI	ULN2064B	
ULN	2065	B	MOT/SGS	ULN2065B	
ULN	2065	N	IP	ULN2065B	
ULN	2065	NE	MOT/TI	ULN2065B	
ULN	2068	B	MOT/SGS	ULN2068B	
ULN	2068	N	IP	ULN2068B	
ULN	2068	NE	TI	ULN2068B	
ULN	2069	B	MOT/SGS	ULN2069B	
ULN	2069	N	IP	ULN2069B	
ULN	2069	NE	TI	ULN2069B	
ULN	2401	A	SPR	ULN2455A	≈
ULN	3006	T	SPR	A3121EU	
ULN	3008	T	SPR	UGN3503U	≈
ULN	3827	A	SPR	A3828EA	
ULN	3847	EP	SPR	A3844EEP	
ULS	3006	T	SPR	A3121LU	
XR	6118	P	EXR	UDN6118A	
XR	6118	P-2	EXR	UDN6118A	
	6	SS	MICR	UGN3503–	≈
	8	SS1E1	MICR	UGN3132U	≈
	8	SS3E1	MICR	UGN3121EU	≈
	8	SS5E1	MICR	UGN3132U	≈
	8	SS7E1	MICR	A3144EU	≈
	55	SS16	MICR	A3144EU	≈
	65	SS2	MICR	A3121EU	≈
	65	SS4	MICR	A3121EU	≈
	91	SS12-2	MICR	UGN3503U	≈
	92	SS12-2	MICR	UGN3503U	≈
	103	SR	MICR	UGN3503–	≈
	103	SR13A-1	MICR	A3121L–	≈
	103	SR17A-1	MICR	UGS3130–	≈
	103	SR5A-1	MICR	A3121E–	≈

Competitive Part Number				Suggested Allegro	
Prefix	Base Number	Suffix	Mfg Code(s)	Replacement	Notes
	513	SS16	MICR	A3141LU	≈
	513	SS16	MICR	A3142LU	≈
	517	SS16	MICR	UGS3132U	≈
	518	SS16	MICR	UGS3132U	≈
	613	SS2	MICR	A3121E–	≈
	613	SS2	MICR	A3121LU	≈
	613	SS4	MICR	A3144LU	≈
	617	SS2	MICR	UGS3132–	≈
	617	SS2	MICR	UGS3132U	≈
	617	SS4	MICR	UGS3132U	≈

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Cherry Semiconductor:

CS 123 D

Package. D = Small Outline
DW = Wide-Body Small Outline
FN = Plastic Leaded Chip Carrier
J = Ceramic DIP
N = Plastic DIP
V = Power Tab SIP
VH = Power Tab SIP with Lead Form

Exar:

XR 2001 C N

Package. D = Small Outline
N = CerDIP
P = Plastic DIP

Grade. C = Commercial (0°C to +70°C)
M = Military (-55°C to +125°C)
Blank = Improved Commercial

Fairchild:

µA 705 P C

Temperature. C = Commercial (0°C to +70 or +75°C)
L = -55°C to +85°C
M = Military (-55°C to +125°C)

Package. D = Ceramic DIP
J = Flange Mount (TO-66)
K = Flange Mount (TO-3)
P = Plastic DIP
R = Ceramic Mini-DIP
T = Plastic Mini-DIP
U = Power Tab (TO-220)

Fujitsu:

MB 3759 E C

Package. C = Ceramic
P = Plastic DIP
Z = CerDIP

Hitachi:

HA 1199 P

Package. C = Ceramic DIP
CG = Ceramic Leadless Chip Carrier
CP = Plastic Leaded Chip Carrier
F = Small Outline
G = CerDIP
P = Plastic DIP
T- = Power-Tab SIP

COMPETITIVE IC PART NUMBERING

Integrated Power:

IP 3 P 45 T

- T — **Package.** D = Ceramic
  - J = CerDIP
  - K = Flange Mount (TO-3)
  - N = Plastic DIP
  - T = Power Tab (TO-220)
- 3 — **Temperature.** 1 = -55°C to +125°C
  - 2 = -25°C to +85°C
  - 3 = 0°C to +70°C

Micrel:

MIC 5800 B N

- N — **Package.** J = CerDIP
  - JB = CerDIP with Burnin
  - M = Small Outline
  - N = Plastic DIP
  - T = Power Tab SIP
  - V = Plastic Leaded Chip Carrier
  - WM = Wide-Body Small Outline
- B — **Temperature.** A = -55°C to +125°C
  - B = -40°C to +85°C
  - C = 0°C to +70°C

Mitsubishi:

M 5 4523 P

- P — **Package.** K = CerDIP
  - P = Plastic DIP
  - S = Ceramic DIP
- 5 — **Temperature.** 5 = Commercial/Industrial
  - 9 = Military

Motorola:

MC 1311 P

- P — **Package.** D = Small Outline
  - K = Metal Flange Mount (TO-3)
  - L = Ceramic DIP
  - P = Plastic DIP
  - PQ = Plastic Quad In-Line
  - R = Metal Flange Mount (TO-66)
  - T = Power Tab (TO-220)
  - U = Ceramic DIP

National Semiconductor:
LM 380 N

N — **Package.**
- D = Ceramic DIP
- E = Ceramic Leadless Chip Carrier
- J = CerDIP
- M= Small Outline
- N = Plastic DIP
- T = Power Tab (TO-220)
- V = Plastic Leaded Chip Carrier
- WM = Wide-Body Small Outline

Pro-Electron:
TD A 1060 P P

P — **Material.**
- C = Metal-Ceramic
- G = Glass-Ceramic (CerDIP)
- M= Metal
- P = Plastic

P — **Package.**
- D = Dual In Line
- G = Flat Quad
- K = Diamond

A — **Temperature.**
- A = See Detail Specification
- B = 0°C to +70°C
- C = -55°C to +125°C
- D = -25°C to +70°C
- E = -25°C to +85°C
- F = -40°C to +85°C
- G = -55°C to +85°C

RCA (Harris):
CA 758 E

E — **Package.**
- D = Ceramic DIP
- E = Plastic DIP
- F = CerDIP
- M = Small Outline
- Q = Plastic Leaded Chip Carrier
- W = Staggered Quad In-Line Plastic
- Blank = See Detail Specification

SGS-Thomson:
L 292 C V

V — **Package.**
- M = Mini-DIP
- N = DIP
- T = Flange Mount
- V = Power Tab SIP (TO-220)
- VH = Power Tab SIP with Lead Form

C — **Special.**
- C = Commercial Temperature
- D = Internal Diodes

Signetics:

NE 564 N

- **Package.** A = Plastic Leaded Chip Carrier
  - D = Small Outline
  - F = CerDIP
  - FE = Mini-CerDIP
  - G = Leadless Chip Carrier
  - I = Ceramic DIP
  - N = Plastic DIP
  - U = Plastic SIP
- **Temperature.** N or NE = 0°C to +70°C
  - SA = -40°C to +85°C
  - S or SE = -55°C to +125°C
  - SU = -25°C to +85°C

Silicon General:

SG 1524 F

- **Package.** D = Small Outline
  - DM = 8-Lead Small Outline
  - DW = Wide-Body Small Outline
  - G = Power Tab (TO-220)
  - H = Ceramic DIP
  - J = CerDIP
  - L = Leadless Ceramic Chip Carrier
  - M = Plastic Mini-DIP
  - N = Plastic DIP
  - P = Power Tab (TO-220)
  - W = Plastic DIP Semi-Tab
  - Y = Ceramic Mini-DIP

Supertex:

HV 6810 P

- **Package.** D = Ceramic DIP
  - NG = Plastic Narrow-Body Small Outline
  - P = Plastic DIP
  - PJ = Plastic Chip Carrier
  - WG = Plastic Wide-Body Small Outline

Texas Instruments:

SN 75 064 NE

Package. D = Small Outline
DW = Wide-Body Small Outline
FG = Ceramic Rectangular Leadless Chip Carrier
FH = Ceramic Square Leadless Chip Carrier
FK = Ceramic Square Leadless Chip Carrier
FM = Plastic Rectangular Leaded Chip Carrier
FN = Plastic Square Leaded Chip Carrier
J = CerDIP
JD = Ceramic DIP
K = Power Tab (TO-220)
N = Plastic DIP
ND = Plastic DIP Semi-Tab
NE = Plastic DIP Semi-Tab
P = Plastic Mini-DIP

Temperature. 55 = -55°C to +125°C
75 = 0°C to +70°C

TL 494 C J

Package. As shown above.

Temperature. C = Commercial (0°C to +70°C)
E = Extended (-40°C to +85°C)
I = Industrial (-25°C to +85°C)
M = Military (-55°C to +125°C)
Q = Extended Industrial (-40°C to +125°C)

Toshiba:

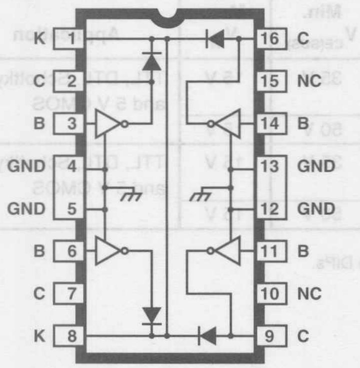
TA 7272 P

Package. C = Ceramic
D = CerDIP
F = Plastic Small Outline
J = Plastic SOJ
P = Plastic DIP
T = PLCC

SECTION 3. TECHNICAL DATA & APPLICATION NOTES FOR PERIPHERAL POWER DRIVER ICs

29305E

ULN2064/65B



Dwg. No. A-9765A

1.5 A DARLINGTON SWITCHES

High-voltage, high-current Darlington arrays ULN2064B/LB through ULN2069B are designed for interface between low-level logic and a variety of peripheral loads such as relays, solenoids, dc and stepper motors, magnetic print hammers, multiplexed LED and incandescent displays, heaters, and similar loads. Output OFF voltage ratings of 50 V and 80 V are available. In the DIP, the quad drivers can drive resistive loads to 480 watts (1.5 A x 80 V, 26% duty cycle). For inductive loads, sustaining voltages of 35 V and 50 V at 100 mA are specified.

Quad drivers ULN2064B/LB, ULN2065B, ULN2068B/LB, and ULN2069B are intended for use with TTL, low-speed TTL, and 5 V MOS logic. The ULN2065B and ULN2069B are selected for the 80 V minimum output breakdown specification. The ULN2068B/LB and ULN2069B have pre-driver stages and are recommended for applications requiring high gain (low input-current loading). Quad-driver arrays are supplied with heat-sink contact tabs in 16-pin plastic DIPs (suffix B) and 20-lead surface-mountable wide-body SOICs (suffix LB).

FEATURES

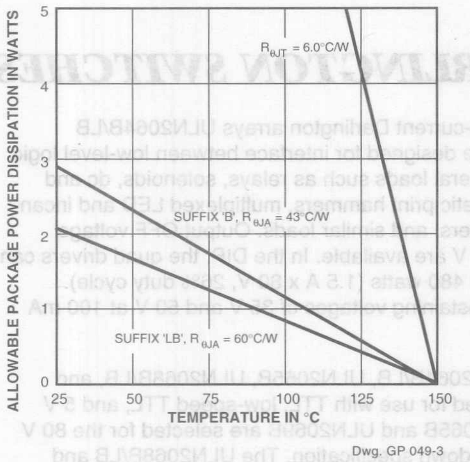
- TTL, DTL, MOS, CMOS Compatible Inputs
- Transient-Protected Outputs
- Loads to 480 Watts
- Heat-Sink Contact Tabs on Quad Arrays
- Automotive Capable

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for Any One Driver (unless otherwise noted)

Output Voltage, V_{CEX} .... See Guide
Output Sustaining Voltage,
$V_{CE(SUS)}$ .... See Guide
Output Current, I_{OUT} (Note 1) .... 1.75 A
Input Voltage, V_{IN} .... See Guide
Input Current, I_B (Note 2) .... 25 mA
Supply Voltage,
V_S (ULN2068B/LB & 2069B) .... 10 V
Total Package Power Dissipation,
P_D .... See Graph
Operating Temperature Range,
T_A .... -20°C to +85°C
Storage Temperature Range,
T_S .... -55°C to -150°C

1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input current may be limited by maximum allowable input voltage.

Always order by complete part number, e.g., ULN2064B . See matrix on next page. Note that all devices are not available in all package types.



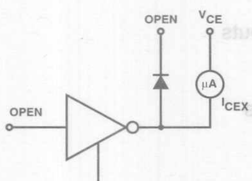
Dwg. GP 049-3

SELECTION GUIDE

Part Number*	Max. V_{CEX}	Min. $V_{CE(SUS)}$	Max. V_{IN}	Application
ULN2064B ULN2064LB	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2065B	80 V	50 V	15 V	
ULN2068B ULN2068LB	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULN2069B	80 V	50 V	15 V	

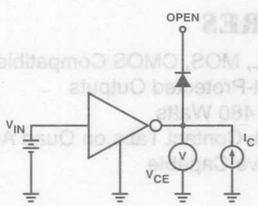
* Suffixes 'LB' are SOICs, 'B' are DIPs.

TEST FIGURES



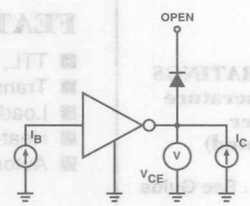
Dwg. No. A-9729A

FIGURE 1



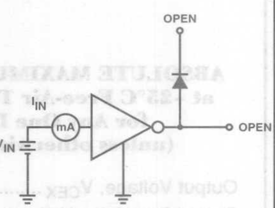
Dwg. No. A-10,350

FIGURE 2



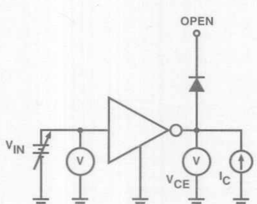
Dwg. No. A-10,349

FIGURE 3



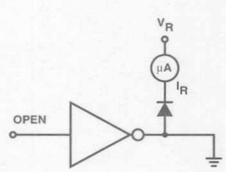
Dwg. No. A-9732

FIGURE 4



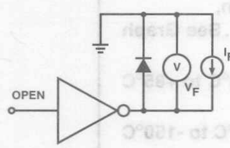
Dwg. No. A-9734A

FIGURE 5



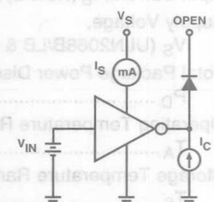
Dwg. No. A-9735A

FIGURE 6



Dwg. No. A-9736

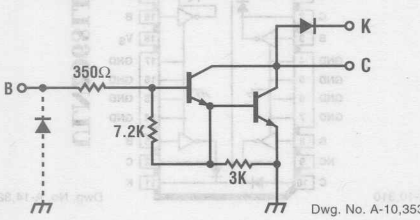
FIGURE 7



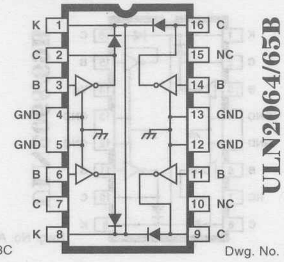
Dwg. No. A-10,351

FIGURE 8

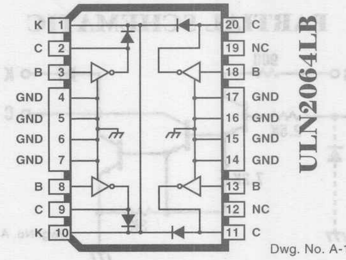
PARTIAL SCHEMATIC



Dwg. No. A-10,353C



Dwg. No. A-9765A



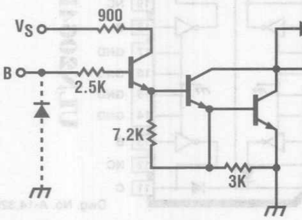
Dwg. No. A-14,326

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

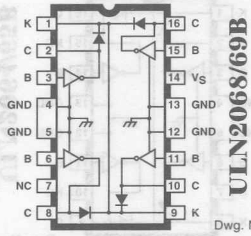
Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2064*	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN2065B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2064*	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN2065B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN2065B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN2064*	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.5	V
			ULN2065B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
Turn-On Delay	t_{PLH}		Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}		Both	0.5 E_{in} to 0.5 E_{out}	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN2064*	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN2065B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

* Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

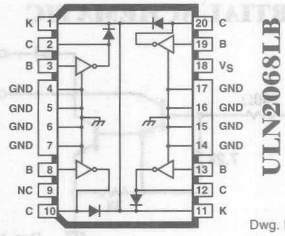
PARTIAL SCHEMATIC



Dwg. No. A-10,354C



Dwg. No. A-10,310



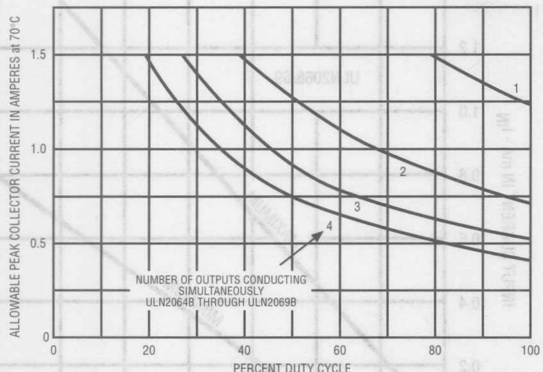
Dwg. No. A-14,327

ELECTRICAL CHARACTERISTICS at +25°C, V_S = 5.0 V (unless otherwise noted).

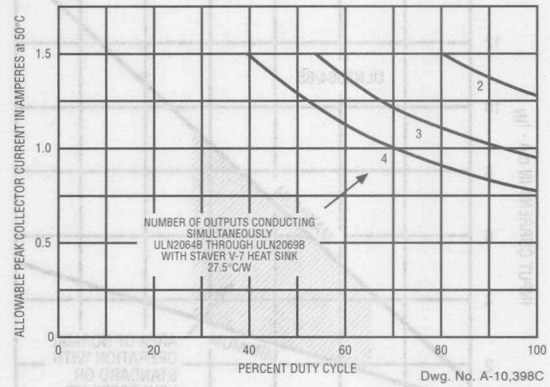
Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN2068*	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN2069B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN2068*	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN2069B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, V_{IN} = 2.75 V	—	1.1	V
				I_C = 750 mA, V_{IN} = 2.75 V	—	1.2	V
				I_C = 1.0 A, V_{IN} = 2.75 V	—	1.3	V
				I_C = 1.25 A, V_{IN} = 2.75 V	—	1.4	V
			ULN2069B	I_C = 1.5 A, V_{IN} = 2.75 V	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	5	ULN2068*	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.75	V
			ULN2069B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.75	V
Supply Current	I_S	8	Both	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 E_{out}, I_C = 1.25 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN2068*	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN2069B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

*Complete part number includes suffix to identify package style: B = DIP with heat sink tabs, LB = SOIC with heat sink tabs.

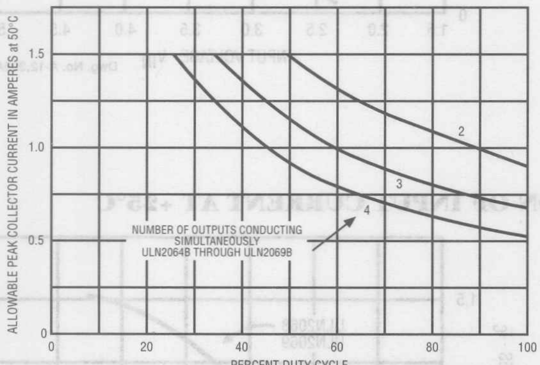
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
(DUAL IN-LINE PACKAGED DEVICES)



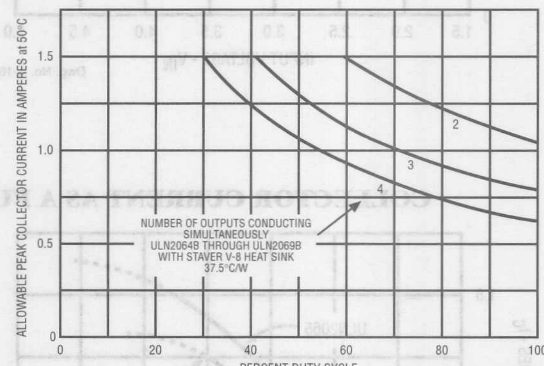
Dwg. No. A-10,360B



Dwg. No. A-10,398C

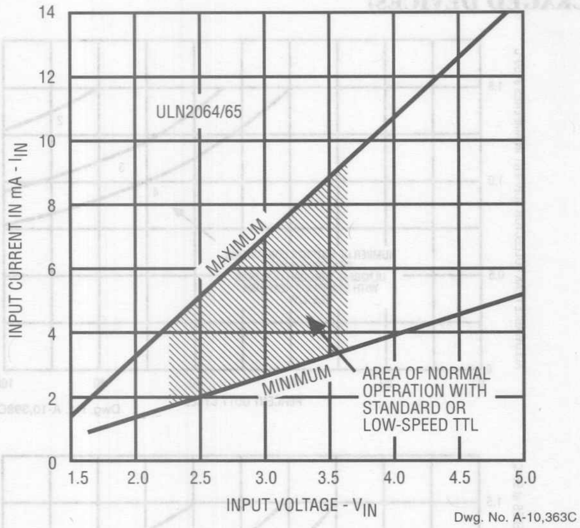


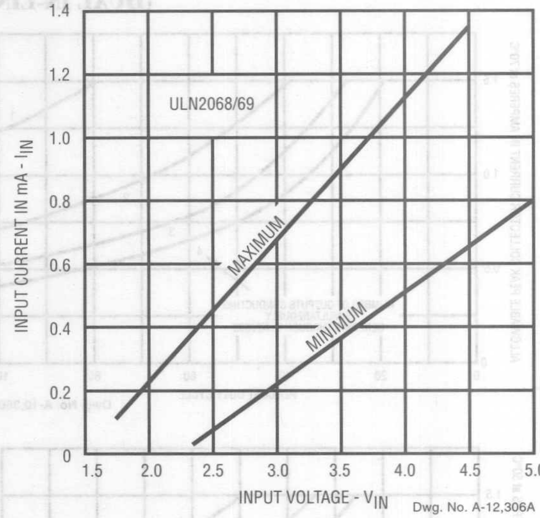
Dwg. No. A-10,361B



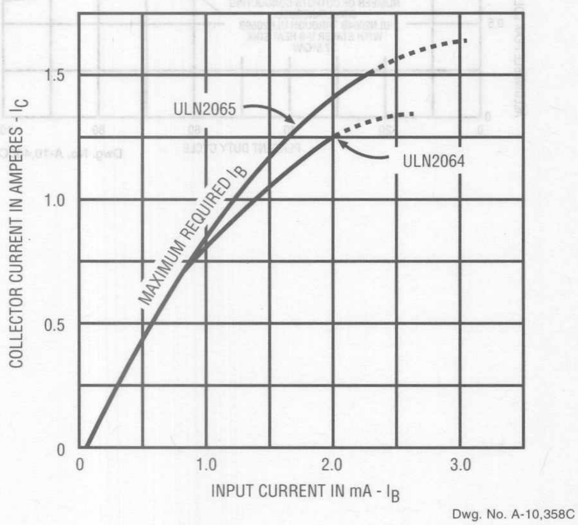
Dwg. No. A-10,400C

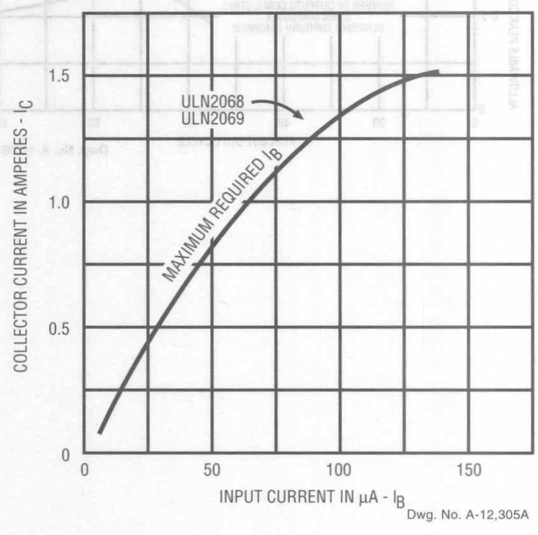
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE AT +25°C



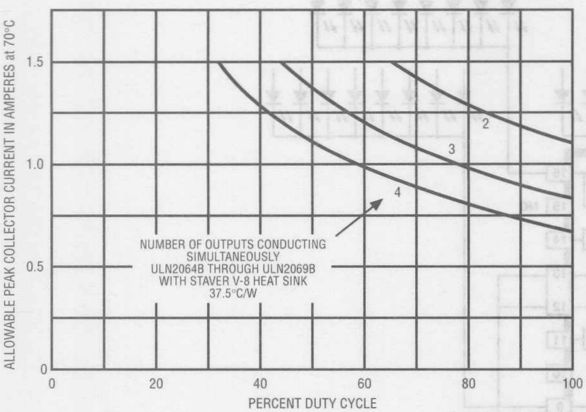


COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT AT +25°C

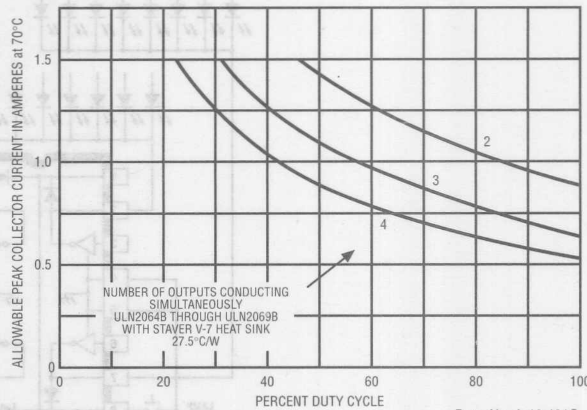




PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
(DUAL IN-LINE PACKAGED DEVICES, cont'd)

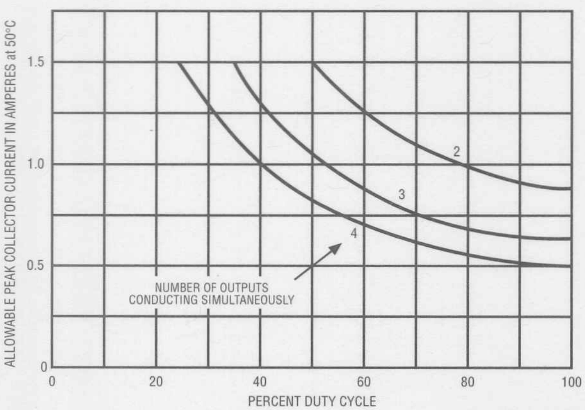


Dwg. No. A-10,399C

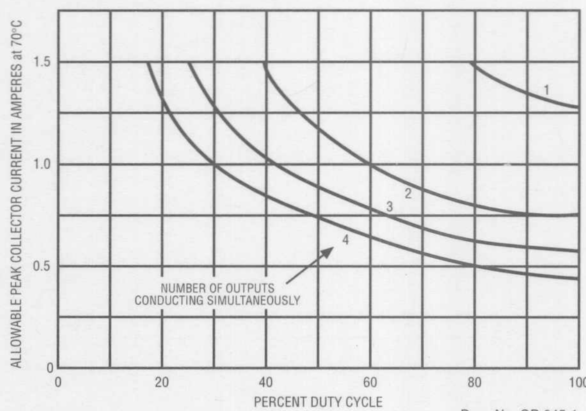


Dwg. No. A-10,401C

(ULN2064LB and ULN2068LB only)

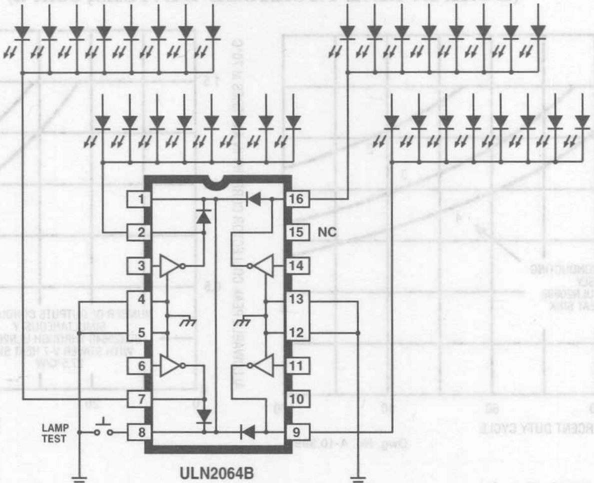


Dwg. No. GP-045



Dwg. No. GP-045-1

TYPICAL APPLICATION



Dwg. No. B-1365

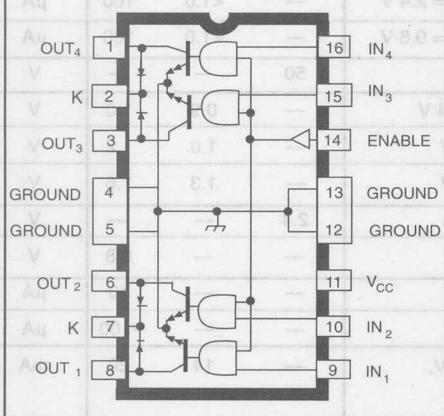
COMMON-CATHODE LED DRIVERS

(Type ULN2068B/LB is also applicable)

2540

29317B

QUAD DARLINGTON POWER DRIVER



Dwg. No. A-11,561A

Combining AND logic gates and inverting high-current bipolar outputs, the UDN2540B quad Darlington power driver provides interface between low-level signal-processing circuits and power loads totaling 360 W. Each of the four independent outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive leads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

Typical applications include print heads, relays, solenoids, and dc stepping motors. The UDN2540B can also be used to drive high-current incandescent lamps, LEDS, and heaters. A similar device, specifically intended for driving a unipolar stepper motor in the two-phase drive format, is the UDN2544B.

The UDN2540B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

FEATURES

- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- TTL and 5 V CMOS Compatible Inputs
- Efficient Input/Output Pinning
- Integral Transient-Suppression Diodes
- Replaces L6221A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

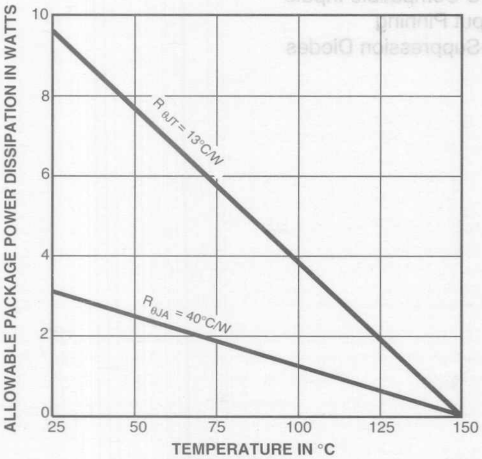
Output Voltage, V_{OUT} .... **50 V**
Output Current, I_{OUT} (peak) .... **2.5 A**
(continuous) .... **1.8 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} .... **7.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Always order by complete part number: **UDN2540B**.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $T_J \leq 150°C$, $V_{CC} = 4.75$ V to 5.25 V.

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 50$ V, $V_{IN} = 0.8$ V, $V_{EN} = 2.4$ V	—	<1.0	100	µA
		$V_{OUT} = 50$ V, $V_{IN} = 2.4$ V, $V_{EN} = 0.8$ V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = 1.8$ A, L = 3.0 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 600$ mA, $V_{IN} = V_{EN} = 2.4$ V	—	0.9	1.0	V
		$I_{OUT} = 1.0$ A, $V_{IN} = V_{EN} = 2.4$ V	—	1.0	1.2	V
		$I_{OUT} = 1.8$ A, $V_{IN} = V_{EN} = 2.4$ V	—	1.3	1.6	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.4	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)} = 2.4$ V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)} = 0.8$ V	—	—	-100	µA
Total Supply Current	I_{CC}	$V_{IN}^* = V_{EN} = 2.4$ V, $V_{CC} = 5.0$ V, Outputs Open	—	14	20	mA
		$V_{IN}^* = V_{EN} = 0.8$ V, $V_{CC} = 5.0$ V	—	0.4	2.0	mA
Clamp Diode Forward Voltage	V_F	$I_F = 1.0$ A	—	1.3	1.6	V
		$I_F = 1.8$ A	—	1.6	2.0	V
Clamp Diode Leakage Current	I_R	$V_R = 50$ V	—	<1.0	100	µA

Typical Data is for design information only.
*All inputs simultaneously, all other tests are performed with each input tested separately.



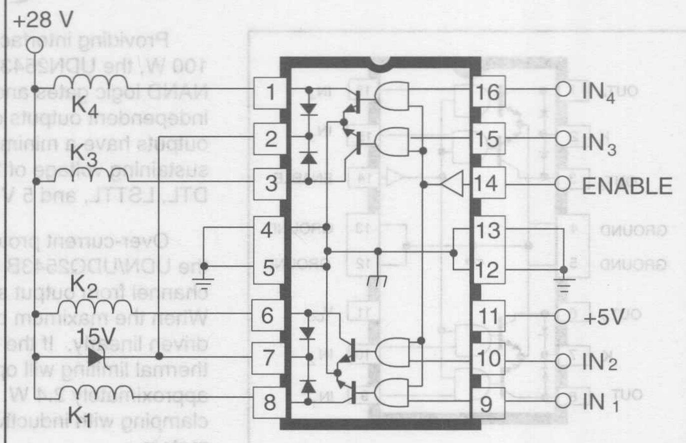
Dwg. GP-004-1

TRUTH TABLE

ENABLE	IN_N	OUT_N
H	H	ON
	L	OFF
L	X	OFF

X = Don't care.

TYPICAL APPLICATION
(QUAD RELAY DRIVER WITH ZENER FLYBACK)



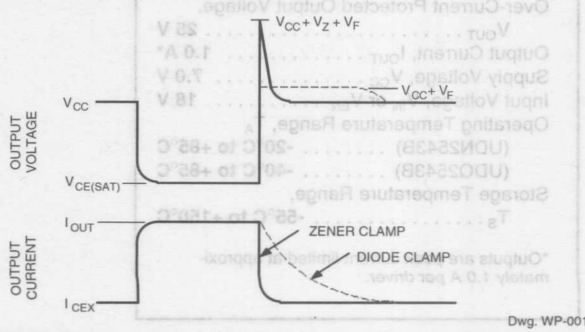
Dwg. EP-016

APPLICATIONS INFORMATION

A typical application is shown for driving four high-current relays, solenoids, or print heads. A Zener diode is used to increase the flyback voltage, providing a much faster inductive load turn-OFF current decay, resulting in faster dropout (reduced relay contact arcing), and improved performance. The maximum Zener voltage, plus the load supply voltage, plus the flyback diode forward voltage must not exceed the device's rated sustaining voltage.

With external control circuitry, the ENABLE input can be used for chopper (PWM) applications. If the ENABLE input is not used, it should be tied high.

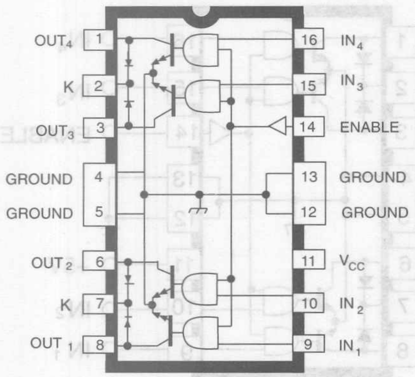
All inputs will float high if open circuited.



Dwg. WP-001

2543

PROTECTED QUAD POWER DRIVERS



Dwg. No. A-11,561A

Providing interface between low-level logic and power loads to 100 W, the UDN2543B and UDQ2543B quad power drivers combine NAND logic gates and high-current bipolar outputs. Each of the four independent outputs can sink up to 700 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 35 V. The inputs are compatible with most TTL, DTL, LSTTL, and 5 V CMOS and PMOS logic systems.

Over-current protection has been designed into each channel of the UDN/UDQ2543B and typically occurs at 1 A. It protects any one channel from output short circuits with supply voltages up to 25 V. When the maximum output current is reached, that output stage is driven linearly. If the over-current condition continues, that output's thermal limiting will operate, limiting that output's power dissipation to approximately 2.4 W. The outputs also include diodes for voltage clamping with inductive loads such as relays, solenoids, or dc stepper motors.

Complete, detailed technical information on the UDN2543B and UDQ2543B is shown in Section 5.

FEATURES

- 700 mA Output Current per Channel
- Low Output-Saturation Voltage
- Integral Output Transient-Suppression Diodes
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Independent Over-Current Protection for Each Output

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

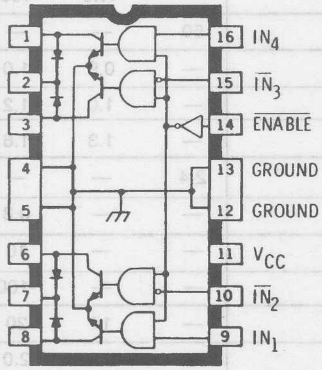
Output Voltage, V_{OUT} . . . . **60 V**
Over-Current Protected Output Voltage,
V_{OUT} . . . . **25 V**
Output Current, I_{OUT} . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . **18 V**
Operating Temperature Range, T_A
(UDN2543B) . . . . **-20°C to +85°C**
(UDQ2543B) . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver.

2544

29317.6*

QUAD DARLINGTON POWER DRIVER



Dwg. No. PP-017

Combining logic gates and high-current bipolar outputs, the UDN2544B quad Darlington power driver provides an interface between low-level logic circuitry and high-power loads. Each of the four outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive loads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

This device is particularly well-suited for unipolar stepper motor drive applications. With complementary control inputs and an active-low ENABLE, the UDN2544B makes it easy to implement full stepping of a stepper motor with only two microcontroller/microprocessor control lines. Other typical applications include relay or solenoid driving and incandescent or LED lamp driving.

The UDN2544B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} .... **50 V**
Output Current, I_{OUT}
(Peak) .... **2.5 A**
(Continuous) .... **1.8 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} .... **7.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

FEATURES

- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- Inputs Configured for Unipolar Stepper Motors
- Active-Low Output Enable
- TTL and 5 V CMOS Compatible Inputs
- Integral Transient-Suppression Diodes

Always order by complete part number: **UDN2544B**.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_J ≤ 150°C, V_{CC} = 4.75 V to 5.25 V.

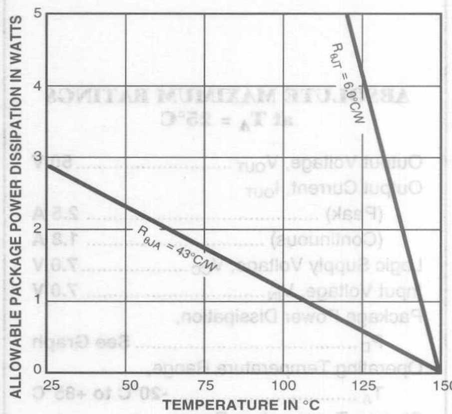
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 1.8 A, L = 3.0 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 600 mA	—	0.9	1.0	V
		I_{OUT} = 1.0 A	—	1.0	1.2	V
		I_{OUT} = 1.8 A	—	1.3	1.6	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.4	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.4 V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-100	µA
Total Supply Current	I_{CC}	All Outputs ON, Outputs Open	—	14	20	mA
		All Outputs OFF	—	0.4	2.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.3	1.6	V
		I_F = 1.8 A	—	1.6	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	< 1.0	100	µA

Typical Data is for design information only

TRUTH TABLE

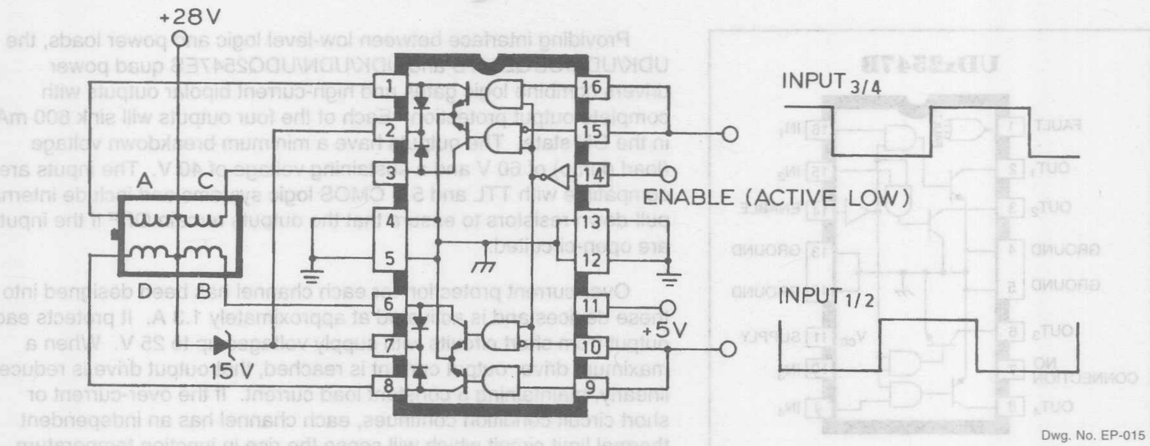
ENABLE	IN_1	OUT_1	IN_2	OUT_2	IN_3	OUT_3	IN_4	OUT_4
L	H	ON	H	OFF	H	OFF	H	ON
	L	OFF	L	ON	L	ON	L	OFF
H	X	OFF	X	OFF	X	OFF	X	OFF

X = Don't care



Dwg. GP-010B

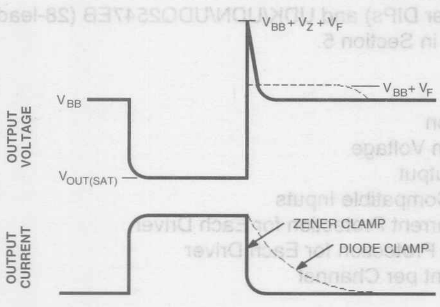
TYPICAL APPLICATION
(UNIPOLAR STEPPER MOTOR WITH ZENER FLYBACK)



Dwg. No. EP-015

TRUTH TABLE

INPUTS		WINDINGS			
1/2	3/4	A	B	C	D
L	H	ON	ON	OFF	OFF
L	L	OFF	ON	ON	OFF
H	L	OFF	OFF	ON	ON
H	H	ON	OFF	OFF	ON



Dwg. No. WP-001

APPLICATIONS INFORMATION

A typical application is shown driving a four-phase unipolar stepper motor. Note that with the complimentary control inputs, only two logic signals are needed to drive the motor in the two-phase format. The two phase drive format illustrated, energizes two adjacent phases in each detent position (AB, BC, CD, DA) to provide an improved torque-speed product and greater detent torque.

A Zener diode can be used to increase the flyback voltage. The increased flyback voltage gives a much faster inductive load turn-OFF current decay resulting in improved motor performance. The maximum Zener voltage, plus the load supply voltage, plus the flyback diode forward voltage must not exceed the device's rated sustaining voltage.

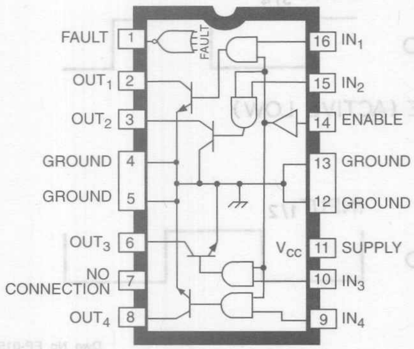
With external control circuitry, the ENABLE input (active low) can be used for chopper (PWM) applications. If the ENABLE input is not used, it should be tied low.

All inputs will float high if open circuited.

2547

PROTECTED QUAD POWER DRIVERS

UDx2547B



Dwg. PP-018

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} ....60 V
Over-Current Protected Output Voltage,
V_{OUT} ....25 V
Output Current, I_{OUT} .... 1.3 A*
FAULT Output Voltage, V_F .... 40 V
Supply Voltage, V_{CC} .... 7.0 V
Input Voltage, V_{IN} or V_{EN} ....7.0 V
Package Power Dissipation,
P_D .... See Graph
Operating Temperature Range, T_A
Prefix 'UDK' .... -40°C to +125°C
Prefix 'UDN' .... -20°C to +85°C
Prefix 'UDQ' .... -40°C to +85°C
Storage Temperature Range,
T_S .... -55°C to +150°C

*Outputs are current limited at approximately 1.3 A per driver and junction temperature limited if current in excess of 1.3 A is attempted.

Providing interface between low-level logic and power loads, the UDK/UDN/UDQ2547B and UDK/UDN/UDQ2547EB quad power drivers combine logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems and include internal pull-down resistors to ensure that the outputs remain OFF if the inputs are open-circuited.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1.3 A. It protects each output from short circuits with supply voltages up to 25 V. When a maximum driver output current is reached, that output drive is reduced linearly, maintaining a constant load current. If the over-current or short circuit condition continues, each channel has an independent thermal limit circuit which will sense the rise in junction temperature and turn OFF the individual channel that is at fault. Foldback circuitry decreases the output current if excessive voltage is present across the output and assists in keeping the device within its SOA (safe operating area).

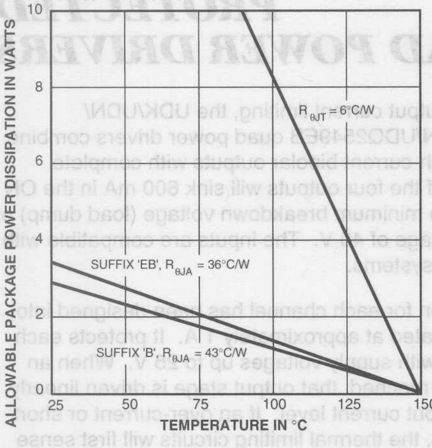
Each output also includes diagnostics for increased device protection. If any output is shorted or opened, the diagnostics can signal the controlling circuitry through a common FAULT pin.

These devices can be used to drive various resistive loads including incandescent lamps (without warming or limiting resistors). With the addition of external output clamp diodes, they can be used to drive inductive loads such as relays, solenoids, or dc stepping motors.

Complete, detailed technical information on the UDK/UDN/UDQ2547B (16-pin power DIPs) and UDK/UDN/UDQ2547EB (28-lead power PLCCs) is shown in Section 5.

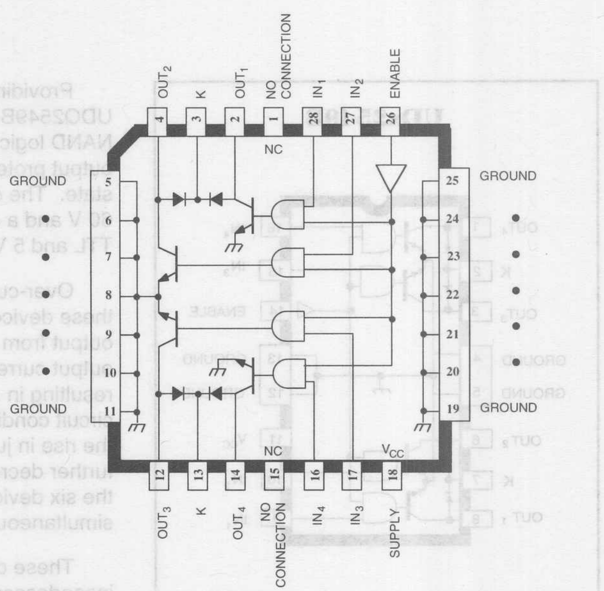
FEATURES

- Output SOA Protection
- Low Output-Saturation Voltage
- Diagnostic FAULT Output
- TTL and 5 V CMOS Compatible Inputs
- Independent Over-Current Protection for Each Driver
- Independent Thermal Protection for Each Driver
- 600 mA Output Current per Channel



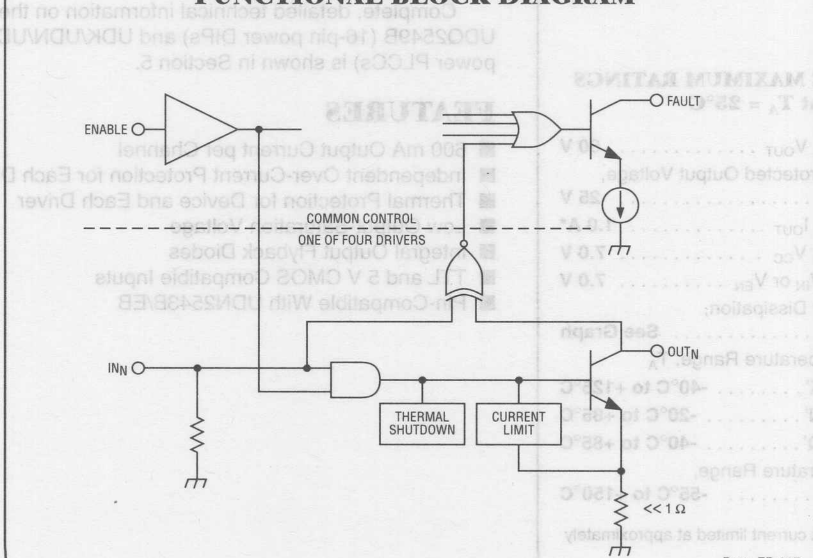
Dwg. GP-004-1A

UDx2547EB



Dwg. PP-019

FUNCTIONAL BLOCK DIAGRAM

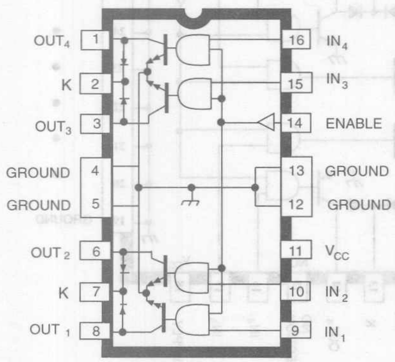


Dwg. FP-007

2549

PROTECTED QUAD POWER DRIVERS

UDx2549B



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . **60 V**
Over-Current Protected Output Voltage,
V_{OUT} . . . . **25 V**
Output Current, I_{OUT} . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . **7.0 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range, T_A
Prefix 'UDK' . . . . **-40°C to +125°C**
Prefix 'UDN' . . . . **-20°C to +85°C**
Prefix 'UDQ' . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver.

Providing improved output current limiting, the UDK/UDN/UDQ2549B and UDK/UDN/UDQ2549EB quad power drivers combine NAND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short circuit condition continues, the thermal limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, the six devices in this family will tolerate short-circuits on all outputs, simultaneously.

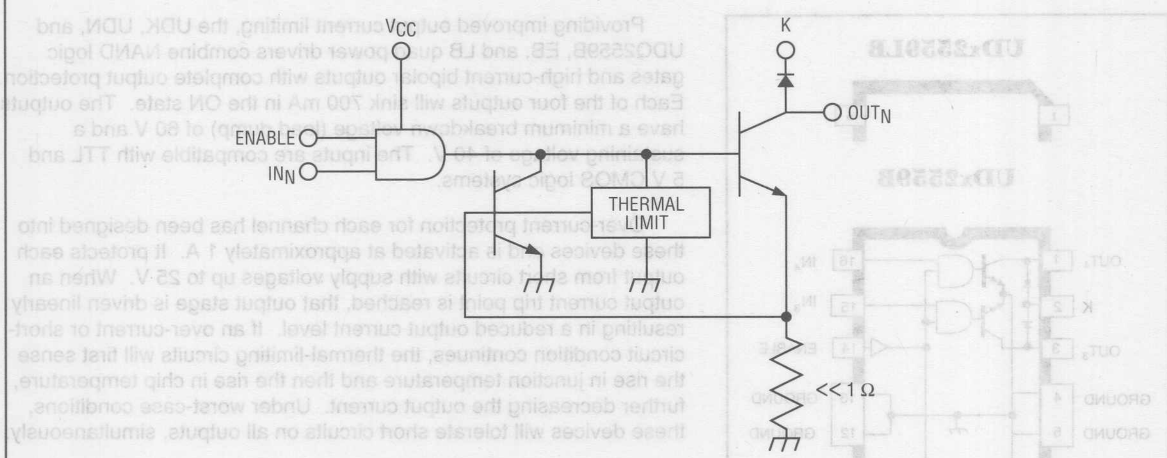
These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

Complete, detailed technical information on the UDK/UDN/UDQ2549B (16-pin power DIPs) and UDK/UDN/UDQ2549EB (28-lead power PLCCs) is shown in Section 5.

FEATURES

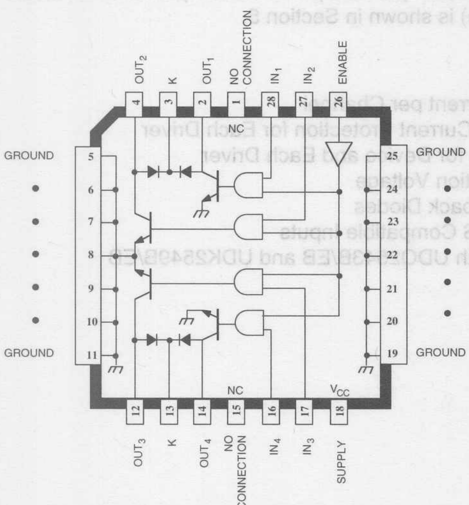
- 600 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDN2543B/EB

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)

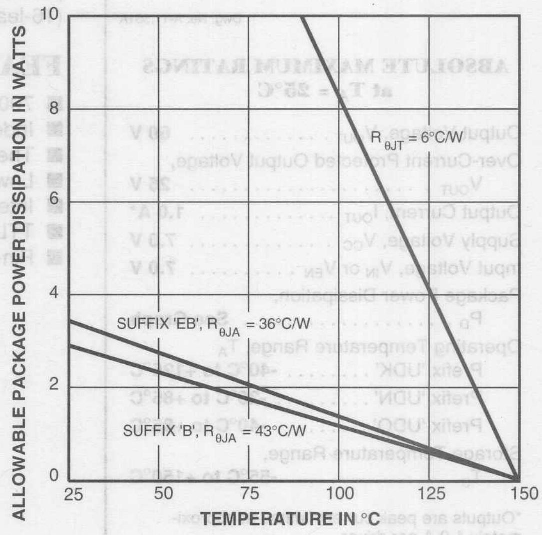


Dwg. No. D-1005

UDx2549EB



Dwg. No. PP-019-1



Dwg. No. GP-004-1A

PROTECTED QUAD POWER DRIVERS

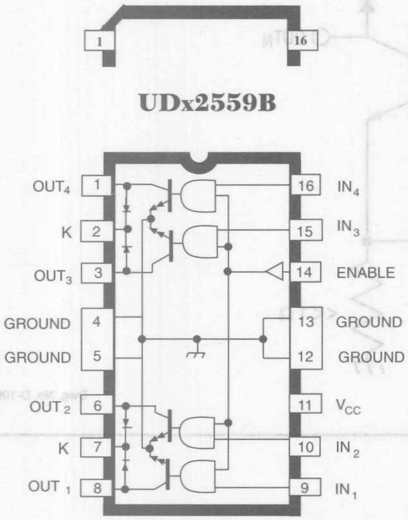
Providing improved output current limiting, the UDK, UDN, and UDQ2559B, EB, and LB quad power drivers combine NAND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 700 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short-circuit condition continues, the thermal-limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, these devices will tolerate short circuits on all outputs, simultaneously.

These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

Complete, detailed technical information on the UDx2559B (16-pin power DIPSs), UDx2559EB (28-lead power PLCCs), and UDx2559LB (16-lead power SOICs) is shown in Section 5.

UDx2559LB



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . **60 V**
Over-Current Protected Output Voltage, V_{OUT} . . . . **25 V**
Output Current, I_{OUT} . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . **7.0 V**
Package Power Dissipation, P_D . . . . **See Graph**
Operating Temperature Range, T_A
Prefix 'UDK' . . . . **-40°C to +125°C**
Prefix 'UDN' . . . . **-20°C to +85°C**
Prefix 'UDQ' . . . . **-40°C to +85°C**
Storage Temperature Range, T_S . . . . **-55°C to +150°C**

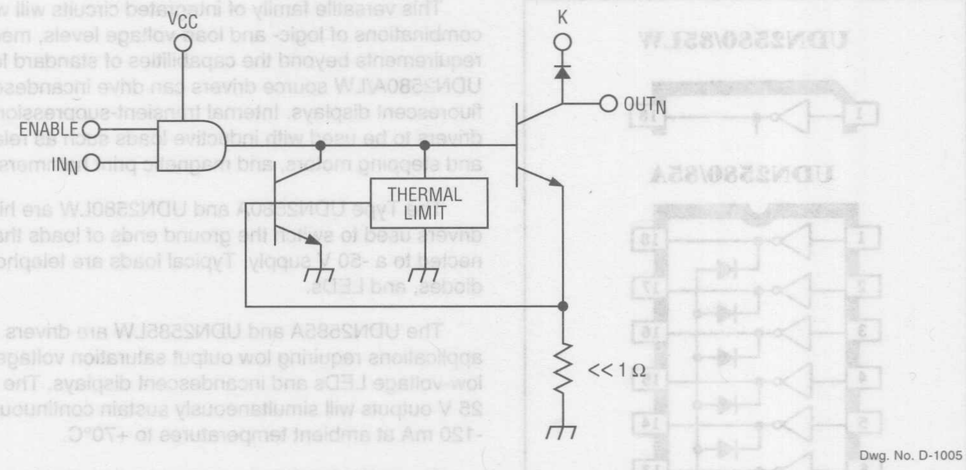
*Outputs are peak current limited at approximately 1.0 A per driver.

FEATURES

- 700 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDQ2543B/EB and UDK2549B/EB

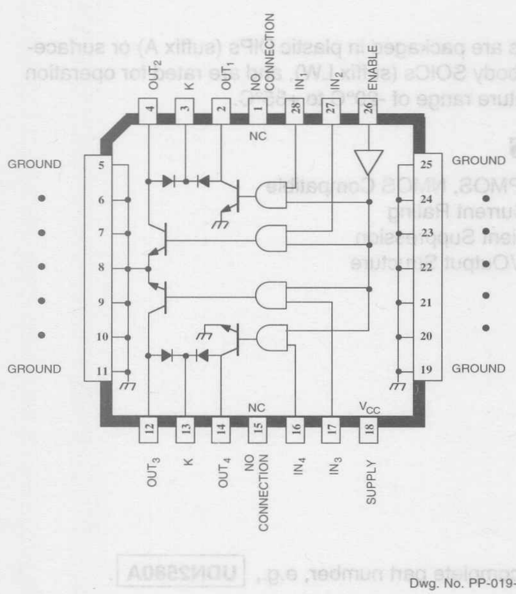
FUNCTIONAL BLOCK DIAGRAM

(1 of 4 Channels)

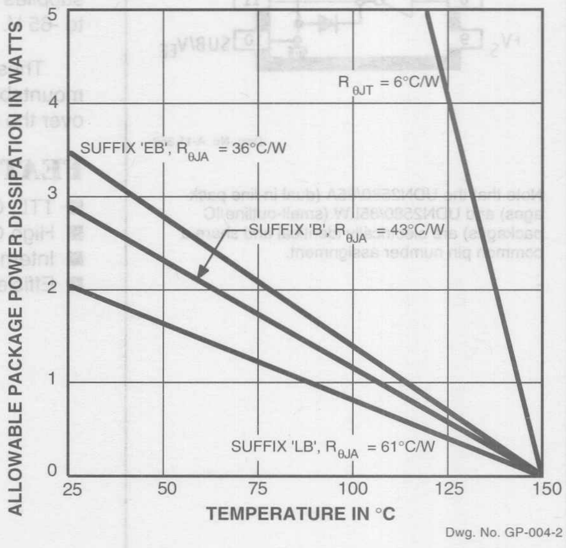


Dwg. No. D-1005

UDx2559EB



Dwg. No. PP-019-1

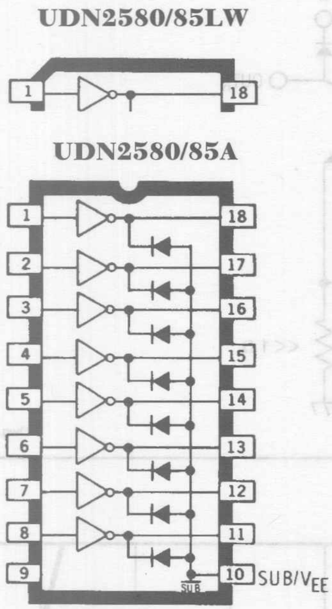


Dwg. No. GP-004-2

$$P_D = (V_{OUT1} \times I_{OUT1} \times dc) + \ldots + (V_{OUTn} \times I_{OUTn} \times dc) + (V_{CC} \times I_{CC})$$
$$= (T_J - T_A)/R_{\theta JA}$$

29316A

8-CHANNEL SOURCE DRIVERS



Dwg. No. A-11,359

Note that the UDN2580/85A (dual in-line packages) and UDN2580/85LW (small-outline IC packages) are electrically identical and share a common pin number assignment.

This versatile family of integrated circuits will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers. Series UDN2580A/LW source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads such as relays, solenoids, dc and stepping motors, and magnetic print hammers.

The Type UDN2580A and UDN2580LW are high-current source drivers used to switch the ground ends of loads that are directly connected to a -50 V supply. Typical loads are telephone relays, PIN diodes, and LEDs.

The UDN2585A and UDN2585LW are drivers designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington, 25 V outputs will simultaneously sustain continuous load currents of -120 mA at ambient temperatures to +70°C.

The UDN2588A has separate logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies to -45 V. Selected devices (UDN2588A-1) may be operated to -65 V.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -20°C to +85°C.

FEATURES

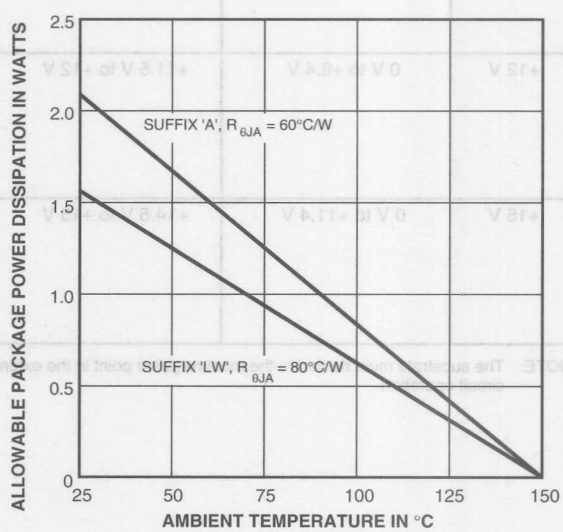
- TTL, CMOS, PMOS, NMOS Compatible
- High Output Current Rating
- Internal Transient Suppression
- Efficient Input/Output Structure

Always order by complete part number, e.g., UDN2580A.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature for any one driver (unless otherwise noted).

	UDN2580A/LW	UDN2585A/LW	UDN2588A	UDN2588A-1
Output Voltage, V_{CE}	50 V	25 V	50 V	80 V
Supply Voltage, V_S (ref. sub.)	50 V	25 V	50 V	80 V
Supply Voltage, V_{CC} (ref. sub.)	—	—	50 V	80 V
Input Voltage, V_{IN} (ref. V_S)	-30 V	-20 V	-30 V	-30 V
Total Output Current, ($I_C + I_S$)	-500 mA	-250 mA	-500 mA	-500 mA
Substrate Current I_{SUB}	3.0 A	2.0 A	3.0 A	3.0 A

Package Power Dissipation, P_D (single output) . . . . 1.0 W
(total package) . . . . See Graph
Operating Temperature Range, T_A . . . . -20°C to +85°C
Storage Temperature Range, T_S . . . . -55°C to +150°C



Dwg. No. GP-018B

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply (V_S), load supply (V_{EE}), and collector supply (V_{CC}). Typical use of the UDN2580A/LW is with negative referenced logic. The more common application of the UDN2585A/LW, UDN2588A, and UDN2588A-1 is with positive referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

TYPICAL OPERATING VOLTAGES

V_S	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
0 V	-15 V to -3.6 V	-0.5 V to 0 V	NA	-25 V	UDN2585A/LW
				-50 V	UDN2580A/LW
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	-20 V	UDN2585A/LW
				-45 V	UDN2580A/LW
			≤ 5 V	-45 V	UDN2588A
				-75 V	UDN2588A-1
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	-13 V	UDN2585A/LW
				-38 V	UDN2580A/LW
			≤12 V	-38 V	UDN2588A
				-68 V	UDN2588A-1
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	-10V	UDN2585A/LW
				-35 V	UDN2580A/LW
			≤15 V	-35 V	UDN2588A
				-65 V	UDN2588A-1

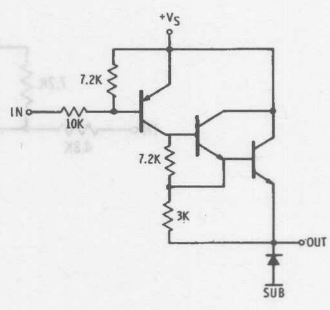
NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

UDN2580A and UDN2580LW
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = -45 V (unless otherwise noted).

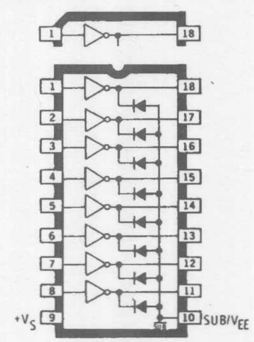
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = -0.5 V, V_{OUT} = V_{EE} = -50 V	—	50	µA
		V_{IN} = -0.4 V, V_{OUT} = V_{EE} = -50 V, T_A = 70°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{IN} = -0.4 V, I_{OUT} = -25 mA, Note 1	35	—	V
Output Saturation	$V_{CE(SAT)}$	V_{IN} = -2.4 V, I_{OUT} = -100 mA	—	1.8	V
		V_{IN} = -3.0 V, I_{OUT} = -225 mA	—	1.9	V
		V_{IN} = -3.6 V, I_{OUT} = -350 mA	—	2.0	V
Input Current	$I_{IN(ON)}$	V_{IN} = -3.6 V, I_{OUT} = -350 mA	—	-500	µA
		V_{IN} = -15 V, I_{OUT} = -350 mA	—	-2.1	mA
	$I_{IN(OFF)}$	I_{OUT} = -500 µA, T_A = 70°C, Note 3	-50	—	µA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = -100 mA, $V_{CE} \le 1.8$ V, Note 4	—	-2.4	V
		I_{OUT} = -225 mA, $V_{CE} \le 1.9$ V, Note 4	—	-3.0	V
		I_{OUT} = -350 mA, $V_{CE} \le 2.0$ V, Note 4	—	-3.6	V
	$V_{IN(OFF)}$	I_{OUT} = -500 µA, T_A = 70°C	-0.2		V
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = 70°C	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}		5.0	µs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES:
1. Pulsed test, $t_p \le 300$ µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



Dwg. No. A-11,358



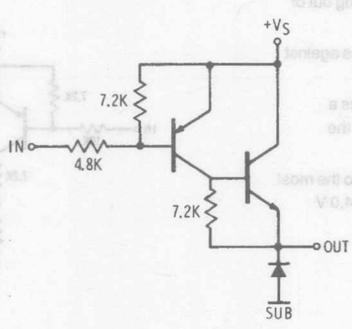
Dwg. No. A-11,359

UDN2585A AND UDN2585LW
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = -20 V (unless otherwise noted).

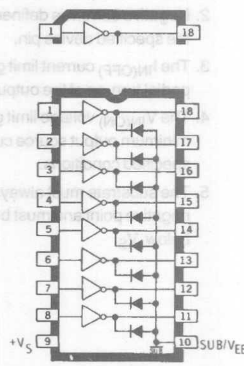
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = -0.5 V, V_{OUT} = V_{EE} = -25 V	—	50	µA
		V_{IN} = -0.4 V, V_{OUT} = V_{EE} = -25 V, T_A = 70°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{IN} = -0.4 V, I_{OUT} = -25 mA, Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = -4.6 V, I_{OUT} = -60 mA	—	1.1	V
		V_{IN} = -4.6 V, I_{OUT} = -120 mA	—	1.2	V
Input Current	$I_{IN(ON)}$	V_{IN} = -4.6 V, I_{OUT} = -120 mA	—	-1.6	mA
		V_{IN} = -14.6 V, I_{OUT} = -120 mA	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = -120 mA, V_{CE} ≤ 1.2 V, Note 3	—	-4.6	V
	$V_{IN(OFF)}$	I_{OUT} = -100 µA, T_A = 70°C	-0.4	—	V
Clamp Diode Leakage Current	I_R	V_R = 25 V, T_A = 70°C	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V
Input Capacitance	C_{IN}		—	25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES: 1. Pulsed test, t_p ≤ 300 µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
4. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



Dwg. No. A-11,360



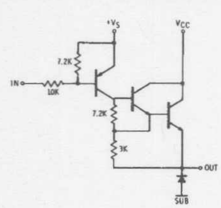
Dwg. No. A-11,359

UDN2588A AND UDN2588A-1
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V, V_{CC} = 5.0 V, V_{EE} = -40 V (unless otherwise noted).

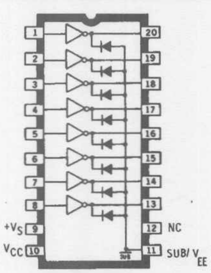
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN2588A	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE}$ = -45 V	—	50	µA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE}$ = -45 V, T_A = 70°C	—	100	µA
		UDN2588A-1	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE}$ = -75 V	—	50	µA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE}$ = -75 V, T_A = 70°C	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN2588A	$V_{IN} \geq 4.6$ V, I_{OUT} = -25 mA, Note 1	35	—	V
		UDN2588A-1	$V_{IN} \geq 4.6$ V, V_{EE} = -70 V, I_{OUT} = -25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	V_{IN} = 2.6 V, I_{OUT} = -100 mA, Ref. V_{CC}	—	1.8	V
			V_{IN} = 2.0 V, I_{OUT} = -225 mA, Ref. V_{CC}	—	1.9	V
			V_{IN} = 1.4 V, I_{OUT} = -350 mA, Ref. V_{CC}	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	V_{IN} = 1.4 V, I_{OUT} = -350 mA	—	-500	µA
			V_S = 15 V, V_{EE} = -30 V, V_{IN} = 0 V, I_{OUT} = -350 mA	—	-2.1	mA
	$I_{IN(OFF)}$	Both	I_{OUT} = -500 µA, T_A = 70°C, Note 3	-50	—	µA
Input Voltage	$V_{IN(ON)}$	Both	I_{OUT} = -100 mA, $V_{CE} \leq 1.8$ V, Note 4	—	2.6	V
			I_{OUT} = -225 mA, $V_{CE} \leq 1.9$ V, Note 4	—	2.0	V
			I_{OUT} = -350 mA, $V_{CE} \leq 2.0$ V, Note 4	—	1.4	V
	$V_{IN(OFF)}$	Both	I_{OUT} = -500 µA, T_A = 70°C	4.8	—	V
Clamp Diode Leakage Current	I_R	UDN2588A	V_R = 50 V, T_A = 70°C	—	50	µA
		UDN2588A-1	V_R = 80 V, T_A = 70°C	—	50	µA
Clamp Diode Forward Voltage	V_F	Both	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	µs

NOTES:
1. Pulsed test, $t_p \leq 300$ µs, duty cycle ≤ 2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.
6. V_{CC} must be equal to or less positive than V_S.

PARTIAL SCHEMATIC

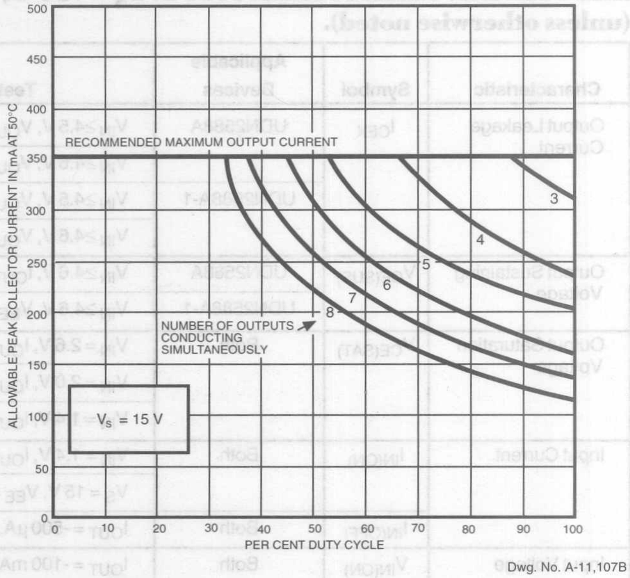


Dwg. No. A-11,361



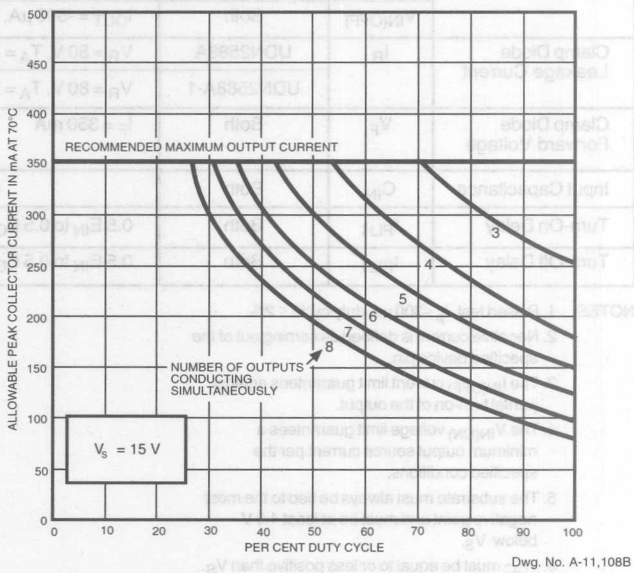
Dwg. No. A-11,357

ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



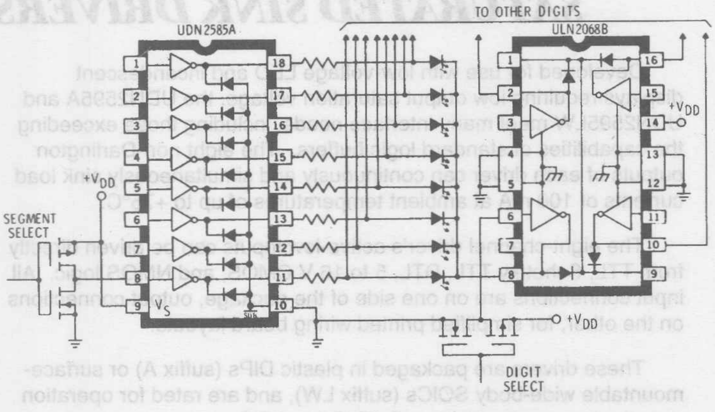
Dwg. No. A-11,107B

ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE



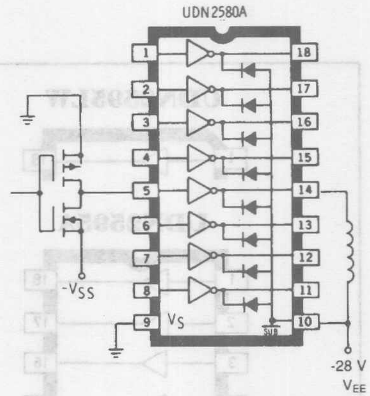
Dwg. No. A-11,108B

TYPICAL APPLICATIONS



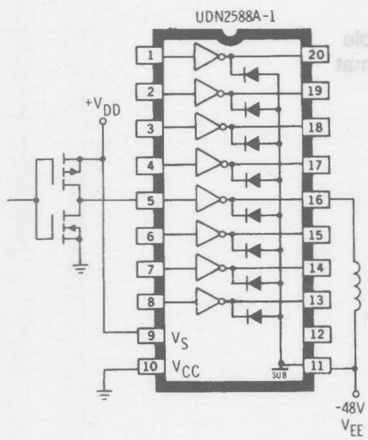
Dwg. No. B-1458A

COMMON-CATHODE LED DRIVER



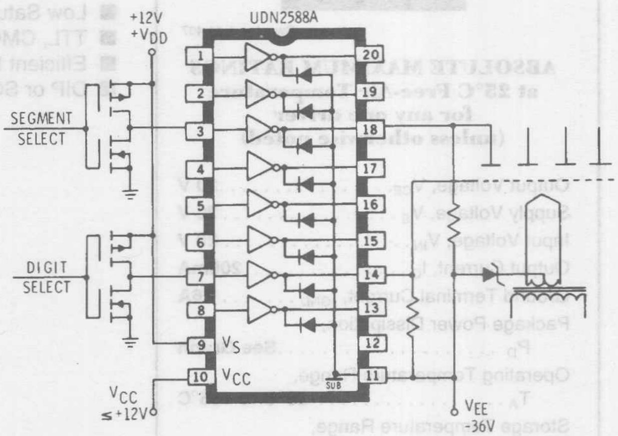
Dwg. No. A-11,356

TELECOMMUNICATIONS RELAY DRIVER
(Negative Logic)



Dwg. No. A-11,362

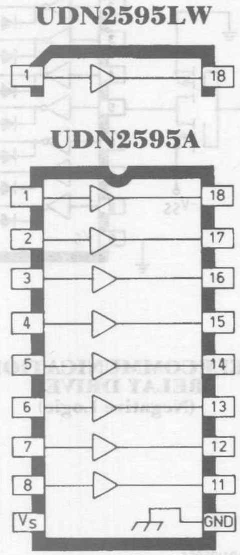
TELECOMMUNICATIONS RELAY DRIVER
(Positive Logic)



Dwg. No. A-11,363

VACUUM-FLUORESCENT DISPLAY DRIVER
(Split Supply)

8-CHANNEL SATURATED SINK DRIVERS



Dwg. No. A-11,407

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one driver (unless otherwise noted)

Output Voltage, V_{CE} . . . . **20 V**
Supply Voltage, V_S . . . . **20 V**
Input Voltage, V_{IN} . . . . **20 V**
Output Current, I_C **200mA**
Ground Terminal Current, I_{GND} **1.6A**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Note that the UDN2595A (dual in-line package) and UDN2595LW (small-outline IC package) are electrically identical and share a common pin number assignment.

Developed for use with low-voltage LED and incandescent displays requiring low output saturation voltage, the UDN2595A and UDN2595LW meet many interface needs, including those exceeding the capabilities of standard logic buffers. The eight non-Darlington outputs of each driver can continuously and simultaneously sink load currents of 100 mA at ambient temperatures of up to +75°C.

The eight-channel driver's active-low inputs can be driven directly from TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified printed wiring board layouts.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -20°C to +85°C.

FEATURES

- Non-Inverting Function
- (Input Low = Output ON)
- 200 mA Current Rating
- 100 mA Continuous and Simultaneous
- (All outputs) to +85°C
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- DIP or SOIC Packaging

Always order by complete part number:

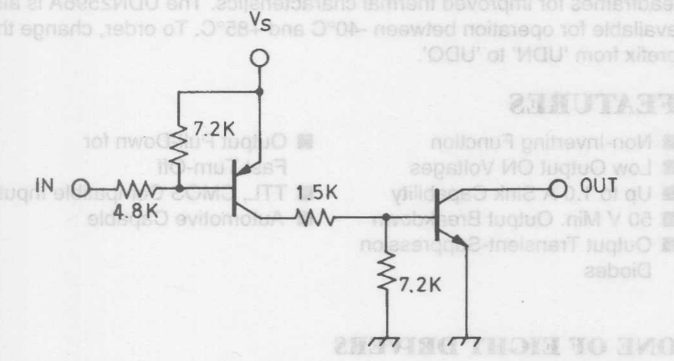
Part Number	Package
UDN2595A	**18-Pin DIP**
UDN2595LW	**18-Lead Wide-Body SOIC**

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V (unless otherwise noted).

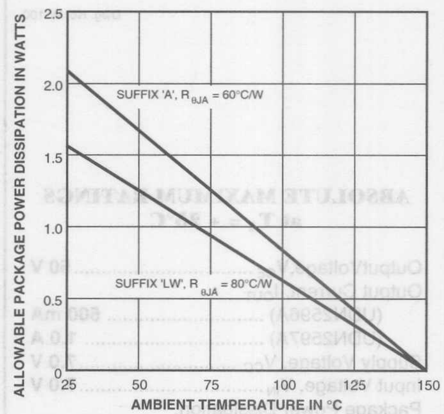
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5$ V, V_{OUT} = 20 V, T_A = 25°C	—	50	µA
		$V_{IN} \geq 4.6$ V, V_{OUT} = 20 V, T_A = 70°C	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 0.4 V, I_{OUT} = 50 mA	—	0.5	V
		V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	0.6	V
Input Current	$I_{IN(ON)}$	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	-1.6	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = 100 mA, $V_{OUT} \leq 0.6$ V	—	0.4	V
	$V_{IN(OFF)}$	I_{OUT} = 100 µA, T_A = 70°C	4.6	—	V
Input Capacitance	C_{IN}		—	25	pF
Supply Current	I_S	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	6.0	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	20	mA

NOTES: 1. Negative current is defined as coming out of the specified device pin.
2. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified conditions.
3. I_S is measured with any one of eight drivers turned ON.

ONE OF EIGHT DRIVERS



Dwg. No. A-11,408

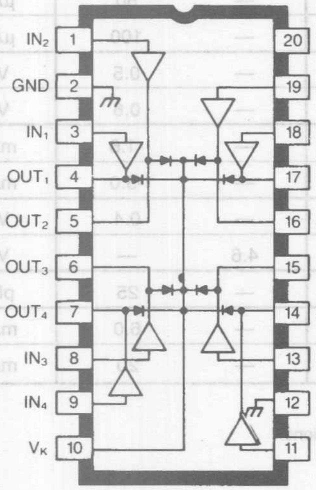


Dwg. No. GP-018B

2596 AND 2597

29320.2A

8-CHANNEL SATURATED SINK DRIVERS



Dwg. No. W-100

Low output saturation voltages at high load currents are provided by UDN2596A and UDN2597A sink driver ICs. These devices can be used as interface buffers between standard low-power digital logic (particularly MOS) and high-power loads such as relays, solenoids, stepping motors, and LED or incandescent displays. The eight saturated sink drivers in each device feature high-voltage, high-current open-collector outputs. Transient suppression clamp diodes and a minimum 35 V output sustaining voltage allow their use with many inductive loads.

The saturated (non-Darlington) NPN outputs provide low collector-emitter voltage drops as well as improved turn-off times due to an active pull-down function within the output predrive section. The UDN2596A is for use with output loads to 500 mA while the UDN2597A is for use with loads to 1 A. Adjacent outputs may be paralleled for higher load currents.

Inputs require very low input current and are activated by a low logic level consistent with the much greater sinking capability associated with NMOS, CMOS, and TTL logic. The UDN2596A and UDN2597A are rated for use with 5 V logic levels.

Both devices are furnished in 20-pin DIP packages with copper leadframes for improved thermal characteristics. The UDN2596A is also available for operation between -40°C and +85°C. To order, change the prefix from 'UDN' to 'UDQ'.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

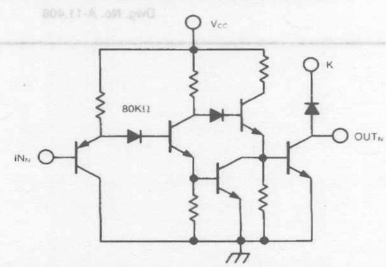
Output Voltage, V_{CE} .... **50 V**
Output Current, I_{OUT}
(UDN2596A) .... **500 mA**
(UDN2597A) .... **1.0 A**
Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} .... **7.0 V**
Package Power Dissipation,
P_D .... **2.27 W***
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

*Derate at the rate of 18.2 mW/°C above T_A= 25°C

FEATURES

- Non-Inverting Function
- Low Output ON Voltages
- Up to 1.0 A Sink Capability
- 50 V Min. Output Breakdown
- Output Transient-Suppression Diodes
- Output Pull-Down for Fast Turn-Off
- TTL, CMOS Compatible Inputs
- Automotive Capable

ONE OF EIGHT DRIVERS

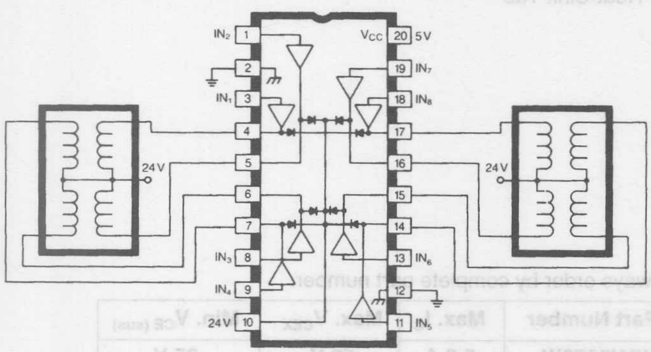


Dwg. No. W-101

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{CC} = 5.0 V

Characteristics	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	Both	V_{OUT} = 50 V, V_{IN} = 2.4 V	—	10	µA
Output Sustaining Voltage	$V_{CE(sus)}$	UDN2596A	I_{OUT} = 300 mA, L = 2 mH	35	—	V
		UDN2597A	I_{OUT} = 750 mA, L = 2 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	UDN2596A	I_{OUT} = 300 mA	—	0.5	V
		UDN2597A	I_{OUT} = 750 mA	—	1.0	V
Clamp Diode Leakage Current	I_R	Both	V_R = 50 V	—	10	µA
Clamp Diode Forward Voltage	V_F	UDN2596A	I_F = 300 mA	—	1.8	V
		UDN2597A	I_F = 750 mA	—	1.8	V
Logic Input Current	$I_{IN(0)}$	Both	V_{IN} = 0.8 V	—	-15	µA
	$I_{IN(1)}$	Both	V_{IN} = 2.4 V	—	10	µA
Supply Current (per driver)	$I_{CC(ON)}$	UDN2596A	V_{IN} = 0.8 V	—	6.0	mA
		UDN2597A	V_{IN} = 0.8 V	—	22	mA
	$I_{CC(OFF)}$	Both	V_{IN} = 2.4 V	—	1.3	mA
Turn-On Delay	t_{pd0}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	3.0	µs
Turn-Off Delay	t_{pd1}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	2.0	µs

TYPICAL APPLICATION
DUAL STEPPER MOTOR DRIVE



Dwg. No. W-102A

RECOMMENDED OPERATING CONDITIONS

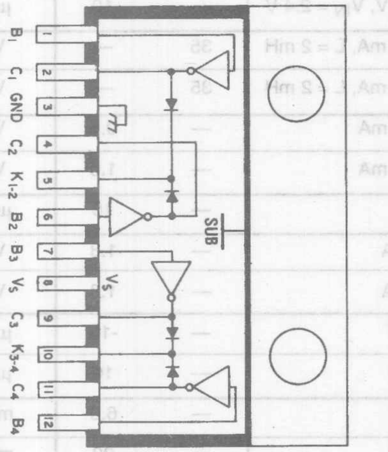
Type Number	Logic	I_{OUT}
UDN2596A	5.0 V	300 mA
UDN2597A	5.0 V	750 mA

Note: Pins 2 and 12 must both be connected to power ground.

2878 AND 2879

29305.10A

QUAD HIGH-CURRENT DARLINGTON SWITCHES



Dwg. No. A-11,974

These quad Darlington arrays are designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 320 W per channel. Both integrated circuits include transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LSTTL, and 5 V CMOS logic.

Type UDN2878W and UDN2879W 4 A arrays are identical except for output-voltage ratings. The former is rated for operation to 50 V (35 V sustaining), while the latter has a minimum output breakdown rating of 80 V (50 V sustaining). The lower-cost UDN2878W-2 is recommended for applications requiring load currents of 3 A or less. These less expensive devices are identical to the basic parts except for the maximum allowable load-current rating.

For maximum power-handling capability, all drivers are supplied in a 12-pin single in-line power-tab package. The tab needs no insulation. External heat sinks are usually required for proper operation of these devices.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any driver (unless otherwise noted)

Output Voltage, V_{CEX}
- (UDN2878W & UDN2878W-2) . . . . **50 V**
- (UDN2879W) . . . . **80 V**

Output Current, I_C
- (UDN2878W & UDN2879W) . . . . **5.0 A**
- (UDN2878W-2) . . . . **4.0 A**

Input Voltage, V_{IN} . . . . **15 V**

Input Current, I_{IN} . . . . **25 mA**

Supply Voltage, V_S . . . . **10 V**

Total Package Power Dissipation, P_D . . . . **See Graph**

Operating Ambient Temperature Range, T_A . . . . **-20°C to +85°C**

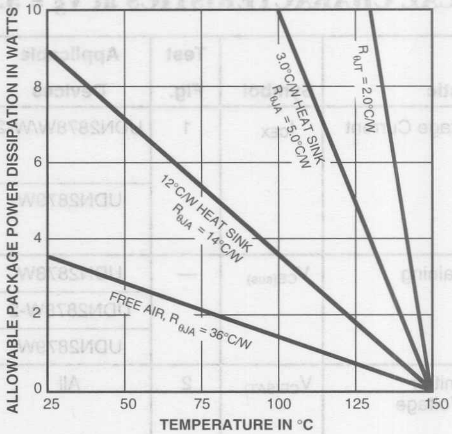
Storage Temperature Range, T_S . . . . **-55°C to +150°C**

FEATURES

- Output Currents to 4 A
- Output Voltages to 80 V
- Loads to 1280 W
- TTL, DTL, or CMOS Compatible Inputs
- Internal Clamp Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab

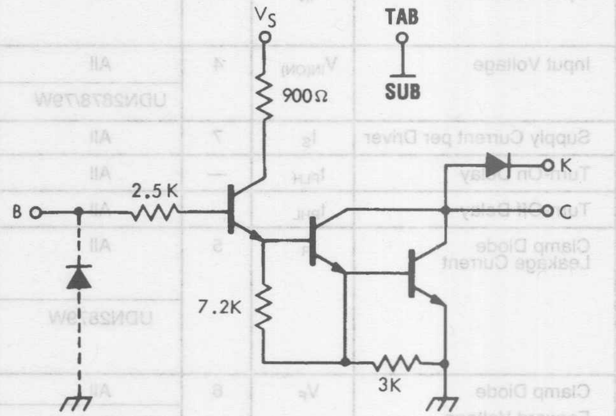
Always order by complete part number:

Part Number	Max. I_C	Max. V_{CEX}	Min. $V_{CE(sus)}$
UDN2878W	5.0 A	50 V	35 V
UDN2878W-2	4.0 A	50 V	35 V
UDN2879W	5.0 A	80 V	50 V



Dwg. GP-012A

PARTIAL SCHEMATIC
One of 4 Drivers



Dwg. No. A-12,037

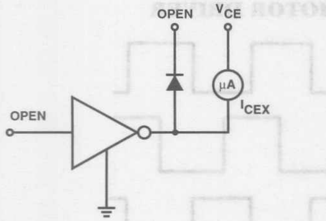
NOTE: Pin 3 must be connected to ground for proper operation.

ELECTRICAL CHARACTERISTICS at V_S = 5.0 V, T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits		Units
					Min.	Max.	
Output Leakage Current	I_{CEX}	1	UDN2878W/W-2	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = +70°C	—	500	µA
			UDN2879W	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = +70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(sus)}$	—	UDN2878W	I_C = 4 A, L = 10 mH	35	—	V
			UDN2878W-2	I_C = 3 A, L = 10 mH	35	—	V
			UDN2879W	I_C = 4 A, L = 10 mH	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 500 mA, V_{IN} = 2.75 V	—	1.1	V
				I_C = 1.0 A, V_{IN} = 2.75 V	—	1.3	V
				I_C = 2.0 A, V_{IN} = 2.75 V	—	1.5	V
				I_C = 3.0 A, V_{IN} = 2.75 V	—	1.9	V
			UDN2878/79W	I_C = 4.0 A, V_{IN} = 3.0 V	—	2.4	V
Input Current	I_{IN}	3	All	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	4	All	V_{CE} = 2.2 V, I_C = 3.0 A	—	2.75	V
			UDN2878/79W	V_{CE} = 2.2 V, I_C = 4.0 A	—	2.75	V
Supply Current per Driver	I_S	7	All	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}, I_C = 3.0 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	5	All	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = +70°C	—	100	µA
			UDN2879W	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = +70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	6	All	I_F = 3.0 A	—	2.5	V
			UDN2878/79W	I_F = 4.0 A	—	3.0	V

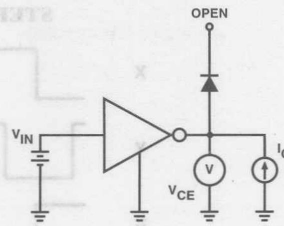
Caution: High-current tests are pulse tests or require heat sinking.

TEST FIGURES



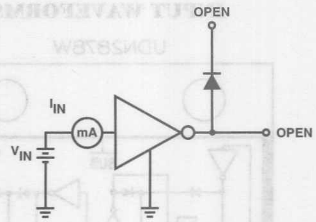
Dwg. No. A-9729A

FIGURE 1



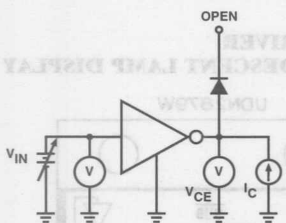
Dwg. No. A-10,350

FIGURE 2



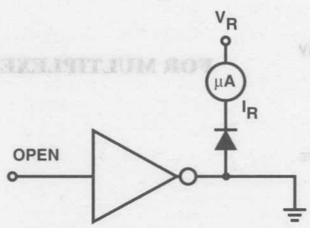
Dwg. No. A-9732

FIGURE 3



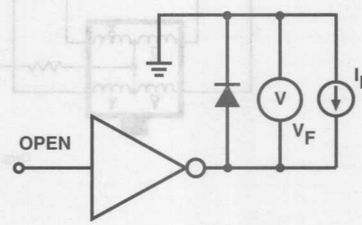
Dwg. No. A-9734A

FIGURE 4



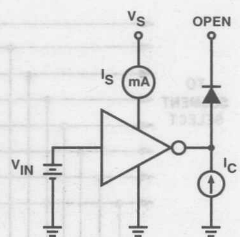
Dwg. No. A-9735A

FIGURE 5



Dwg. No. A-9736

FIGURE 6

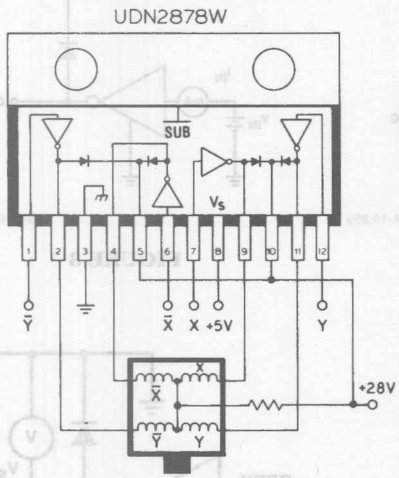


Dwg. No. A-10,351

FIGURE 7

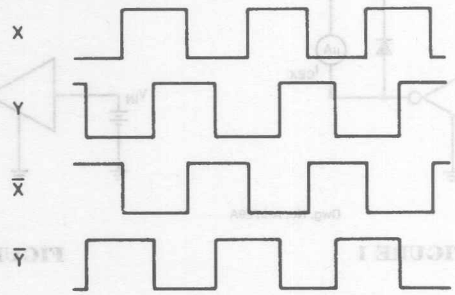
TYPICAL APPLICATIONS

INPUT WAVEFORMS



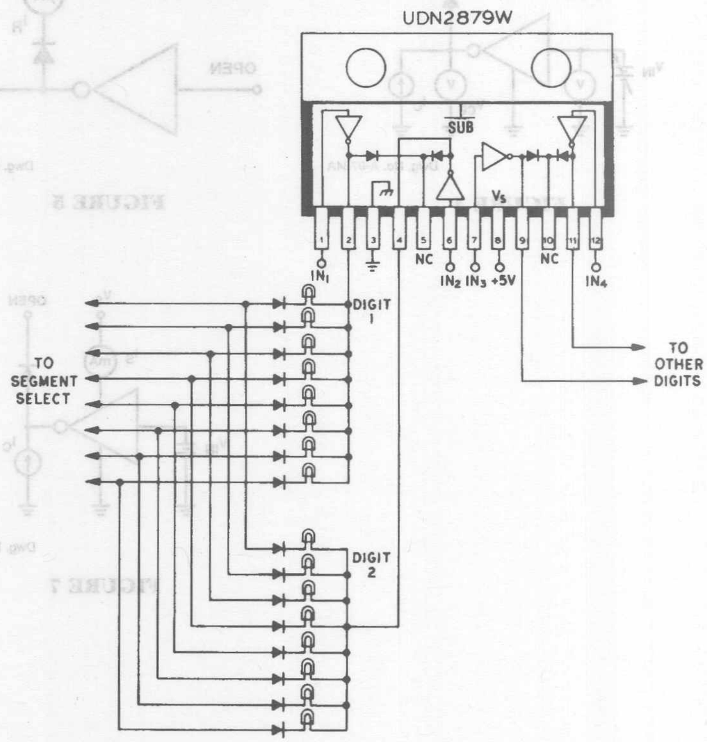
Dwg. No. A-11,975

STEPPER-MOTOR DRIVER



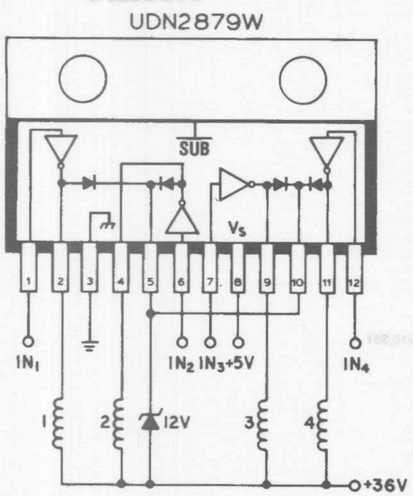
Dwg. No. A-11,795

DIGIT DRIVER FOR MULTIPLEXED INCANDESCENT LAMP DISPLAY



Dwg. No. B-1512

PRINT-HAMMER DRIVER

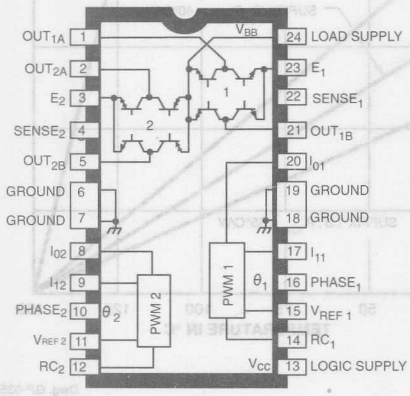


Dwg. No. A-11,976

2916

DUAL FULL-BRIDGE PWM MOTOR DRIVER

UDN2916B



Dwg. No. PP-005

ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Motor Supply Voltage, V_{BB} .... **45 V**
Output Current, I_{OUT}
(Peak) .... **+1.0 A**
(Continuous) .... **+750 mA**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E .... **1.5 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The UDN2916B, UDN2916EB, and UDN2916LB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33, 67, or 100% of the maximum level. A PHASE input to each bridge determines load current direction.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent crossover currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The UDN2916B is supplied in a 24-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. The UDN2916EB is supplied in a 44-lead power PLCC for surface mount applications. The UDN2916LB is supplied in a 24-lead surface-mountable SOIC. Their batwing construction provides for maximum package power dissipation in the smallest possible construction. The UDN2916B/EB/LB are also available for operation from -40°C to +85°C. To order, change the prefix from 'UDN' to 'UDQ'.

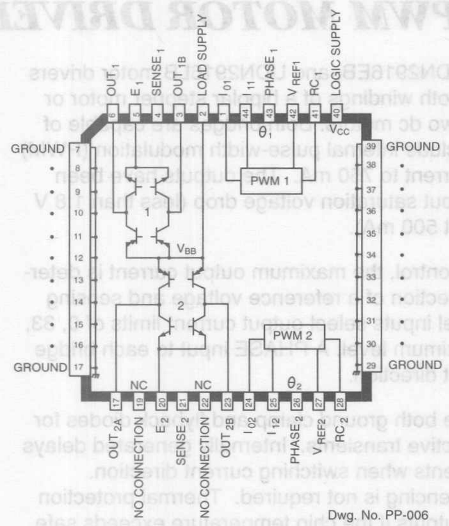
FEATURES

- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3717, UC3770

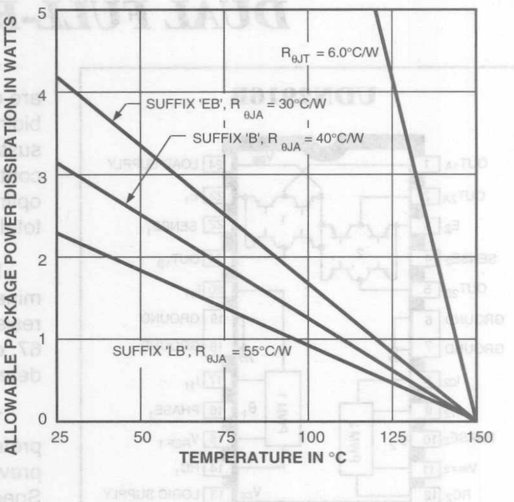
Always order by complete part number:

Part Number	Package
UDN2916B	24-Pin DIP
UDN2916EB	44-Lead PLCC
UDN2916LB	24-Lead SOIC

UDN2916EB

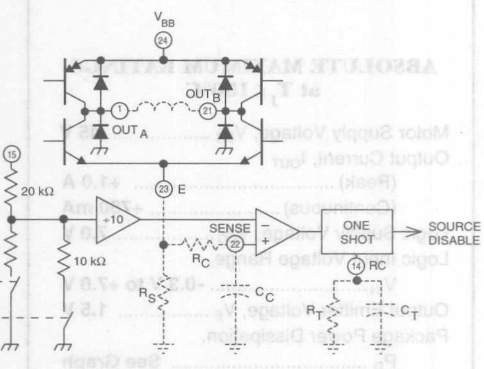


Dwg. No. PP-006



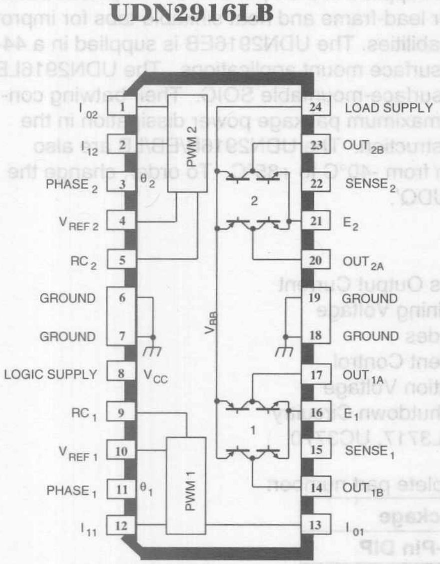
Dwg. GP-035A

PWM CURRENT-CONTROL CIRCUITRY



Dwg. No. EP-007B

UDN2916LB



Dwg. PP-047

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_J \leq 150°C$, $V_{BB} = 45$ V, $V_{CC} = 4.75$ V to 5.25 V, $V_{REF} = 5.0$ V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	< 1.0	50	µA
		$V_{OUT} = 0$	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = \pm750$ mA, L = 3.0 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, $I_{OUT} = +500$ mA	—	0.4	0.6	V
		Sink Driver, $I_{OUT} = +750$ mA	—	1.0	1.2	V
		Source Driver, $I_{OUT} = -500$ mA	—	1.0	1.2	V
		Source Driver, $I_{OUT} = -750$ mA	—	1.3	1.5	V
Clamp Diode Leakage Current	I_R	$V_R = 45$ V	—	<1.0	50	µA
Clamp Diode Forward Voltage	V_F	$I_F = 750$ mA	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	20	25	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	5.0	10	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All inputs	2.4	—	—	V
	$V_{IN(0)}$	All inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 2.4$ V	—	<1.0	20	µA
		$V_{IN} = 0.8$ V	—	- 3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{SENSE}	$I_0 = I_1 = 0.8$ V	9.5	10	10.5	—
		$I_0 = 2.4$ V, $I_1 = 0.8$ V	13.5	15	16.5	—
		$I_0 = 0.8$ V, $I_1 = 2.4$ V	25.5	30	34.5	—
Thermal Shutdown Temperature	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	$I_0 = I_1 = 8.0$ V, No Load	—	40	50	mA
	$I_{CC(OFF)}$	$I_0 = I_1 = 2.4$ V, No Load	—	10	12	mA

APPLICATIONS INFORMATION

PWM CURRENT CONTROL:

The UDN2916B/EB/LB dual bridges are designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

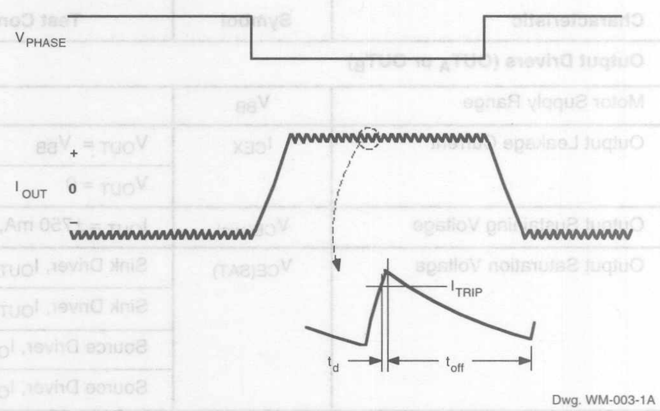
When the bridge is turned ON, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{SENSE}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

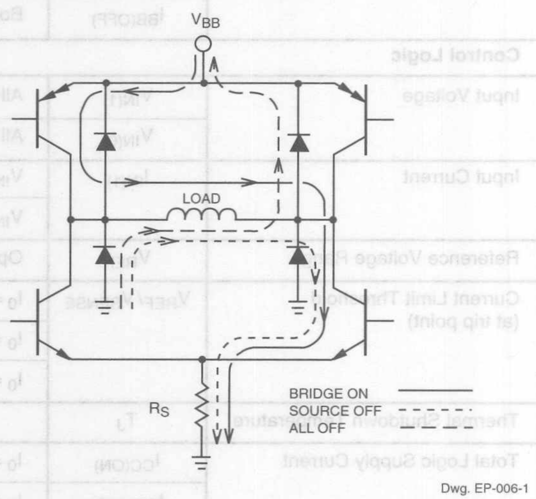
The comparator then triggers the monostable which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_T C_T$ within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

PWM OUTPUT CURRENT WAVE FORM



LOAD CURRENT PATHS



Loads with high distributed capacitances may result in high turn-ON current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An external $R_C C_C$ time delay should be used to further delay the action of the comparator. Depending on load type, many applications will not require these external components (SENSE connected to E).

LOGIC CONTROL OF OUTPUT CURRENT:

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns OFF all drivers in the bridge and can be used as an OUTPUT ENABLE function.

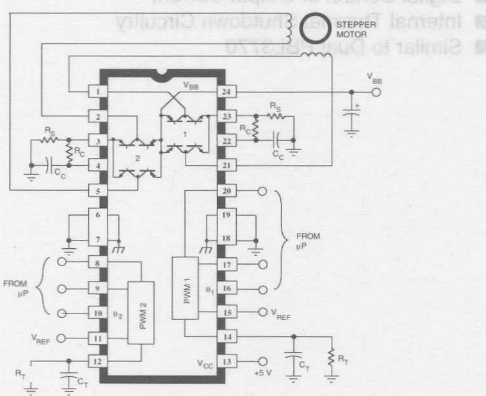
CURRENT-CONTROL TRUTH TABLE

I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

These logic level inputs greatly enhance the implementation of µP-controlled drive formats.

During half-step operations, the I_0 and I_1 allow the µP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is ON and 67% drive current when two phases are ON. Logic highs on both I_0 and I_1 turn OFF all drivers to allow rapid current decay when switching phases. This helps to ensure proper motor operation at high step rates.

TYPICAL APPLICATION



Dwg. EP-008 B

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

GENERAL:

To avoid excessive voltage spikes on the LOAD SUPPLY pin (V_{BB}), a large-value capacitor (≥22µF) should be connected from V_{BB} to ground as close as possible to the device. Under no circumstances should the voltage at LOAD SUPPLY exceed 45 V.

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 µs) prevents crossover currents that can occur when switching the PHASE input.

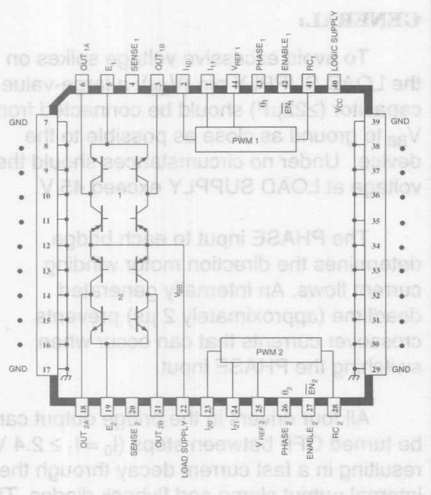
All four drivers in the bridge output can be turned OFF between steps ($I_0 = I_1 \geq 2.4$ V) resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, I_0, and I_1 inputs float high.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for micro-stepping applications.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

The UDN2916B/EB/LB output drivers are optimized for low output saturation voltages—less than 1.8 V total (source plus sink) at 500 mA. Under normal operating conditions, when combined with the excellent thermal properties of the batwing package design, this allows continuous operation of both bridges simultaneously at 500 mA.

DUAL FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PP-021

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} .... **45 V**

Output Current, I_{OUT} ($t_w \leq 20$ μs) ..... **±1.75 A**

(Continuous) .... **±1.5 A**

Logic Supply Voltage, V_{CC} .... **7.0 V**

Logic Input Voltage Range,

V_{IN} .... **-0.3 V to +7.0 V**

Output Emitter Voltage, V_E .... **1.0 V**

Package Power Dissipation,

P_D .... **See Graph**

Operating Temperature Range,

T_A .... **-20°C to +85°C**

Storage Temperature Range,

T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The UDN2917EB motor driver is designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 1.5 A.

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction. Active-low ENABLE inputs control the four drivers in each bridge.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

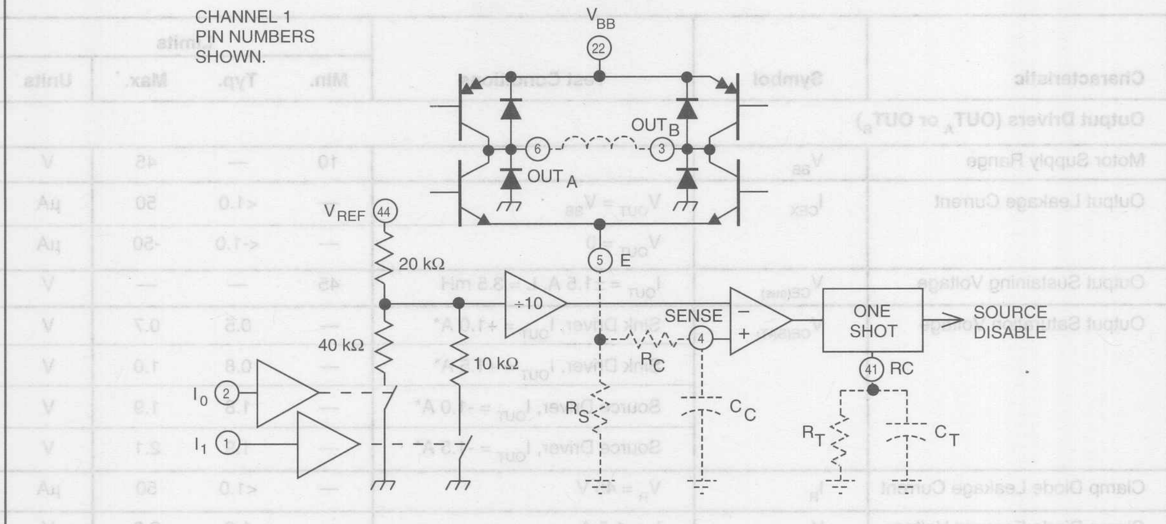
The UDN2917EB is supplied in a 44-lead power PLCC for surface-mount applications. Its batwing construction provides for maximum package power dissipation in the smallest possible construction.

FEATURES

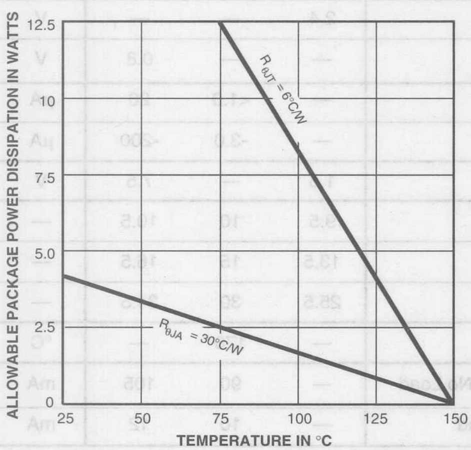
- 1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Digital Control of Output Current
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3770

Always order by complete part number: **UDN2917EB** .

PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007-2A



Dwg. GP-020B

TRUTH TABLE

Enable	Phase	Out_A	Out_B
L	H	H	L
L	L	L	H
H	X	Z	Z

X = Don't care
Z = High impedance

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 5.0 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	µA
		$V_{OUT} = 0$	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±1.5 A, L = 3.5 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +1.0 A*	—	0.5	0.7	V
		Sink Driver, I_{OUT} = +1.5 A*	—	0.8	1.0	V
		Source Driver, I_{OUT} = -1.0 A*	—	1.8	1.9	V
		Source Driver, I_{OUT} = -1.5 A*	—	1.9	2.1	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.5 A	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	9.0	12	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	4.0	6.0	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{SENSE}	$I_0 = I_1$ = 0.8 V	9.5	10	10.5	—
		I_0 = 2.4 V, I_1 = 0.8 V	13.5	15	16.5	—
		I_0 = 0.8 V, I_1 = 2.4 V	25.5	30	34.5	—
Thermal Shutdown Temp.	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	$I_0 = I_1 = V_{EN}$ = 0.8 V, No Load	—	90	105	mA
	$I_{CC(OFF)}$	$I_0 = I_1$ = 2.4 V, No Load	—	10	12	mA

Negative current is defined as coming out of (sourcing) the specified device pin.

Typical Data is for design information only.

* Pulse test (<10 ms).

APPLICATIONS INFORMATION

PWM CURRENT CONTROL:

The UDN2917EB dual bridge is designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{SENSE}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

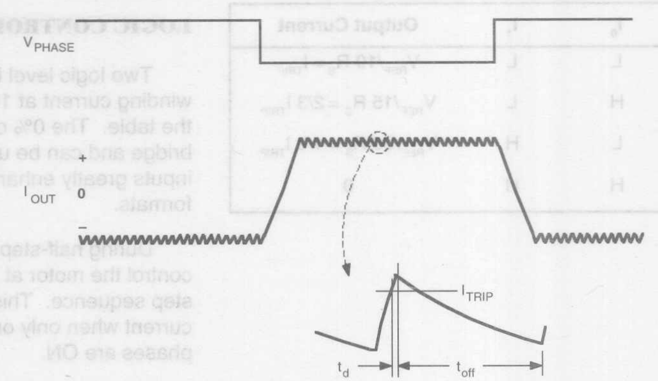
The comparator then triggers the monostable which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current will normally decay, circulating through the ground clamp diode and sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_TC_T$ within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Special circuitry has been included to prevent runaway current control when the fixed OFF time (t_{off}) is set too short. This circuitry prevents the source driver from being re-enabled until the load current has decayed to below the I_{TRIP} level.

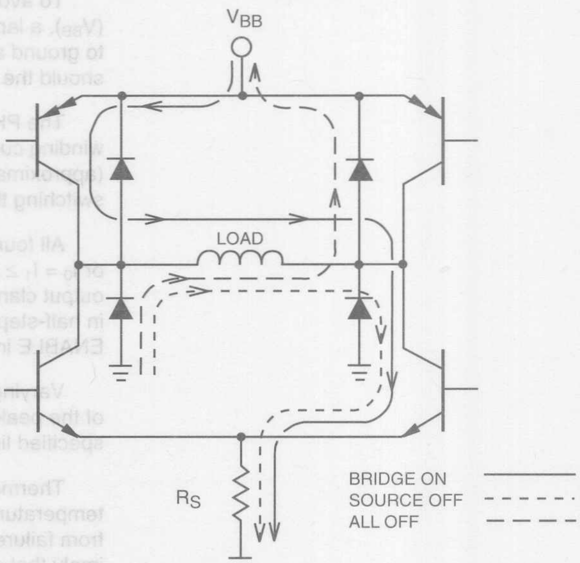
Loads with high distributed capacitances may result in high turn-ON current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous

PWM OUTPUT CURRENT WAVEFORM



Dwg. WM-003-1A

LOAD CURRENT PATHS



Dwg. EP-006-1

CURRENT-CONTROL TRUTH TABLE

I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

current control or high-frequency oscillations. An external R_CC_C low-pass filter may be needed to delay the action of the comparator.

LOGIC CONTROL OF OUTPUT CURRENT:

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns OFF all drivers in the bridge and can be used as an output enable function. These logic level inputs greatly enhance the implementation of μP-controlled drive formats.

During half-step operations, the I_0 and I_1 inputs allow the μP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is ON and 67% drive current when two phases are ON.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

GENERAL:

To avoid excessive voltage spikes on the LOAD SUPPLY pin (V_{BB}), a large-value capacitor (≥47 μF) should be connected from V_{BB} to ground as close as possible to the device. Under no circumstances should the voltage at LOAD SUPPLY exceed 45 V.

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 3 μs) prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned OFF ($V_{EN} \geq 2.4$ V or $I_0 = I_1 \geq 2.4$ V), resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. All logic inputs float high; the ENABLE input must be tied low if it is not used.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for micro-stepping applications, within the specified limits for V_{REF}.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

2918

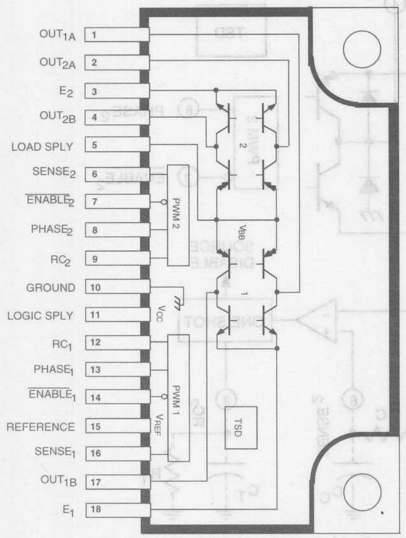
DUAL FULL-BRIDGE PWM MOTOR DRIVER

The A2918SWH and A2918SWV motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. All bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 1.5 A.

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. A PHASE input to each bridge determines load current direction. Active low ENABLE inputs control the four drivers in each bridge.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The A2918SWH/V are supplied in an 18-lead power-tab package with staggered lead forming. The tab is internally insulated from the device and requires no external isolation.



Dwg. PP-051

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} . . . . **45 V**

Output Current, I_{OUT} ($t_w \leq 20$ µs) . . **±1.75 A**

(Continuous) . . . . **±1.5 A**

Logic Supply Voltage, V_{CC} . . . . **7.0 V**

Logic Input Voltage Range, V_{IN} . . . . **-0.3 V to +7.0 V**

Output Emitter Voltage, V_E . . . . **1.5 V**

Package Power Dissipation, P_D . . . . **See Graph**

Operating Temperature Range, T_A . . . . **-20°C to +85°C**

Storage Temperature Range, T_S . . . . **-40°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

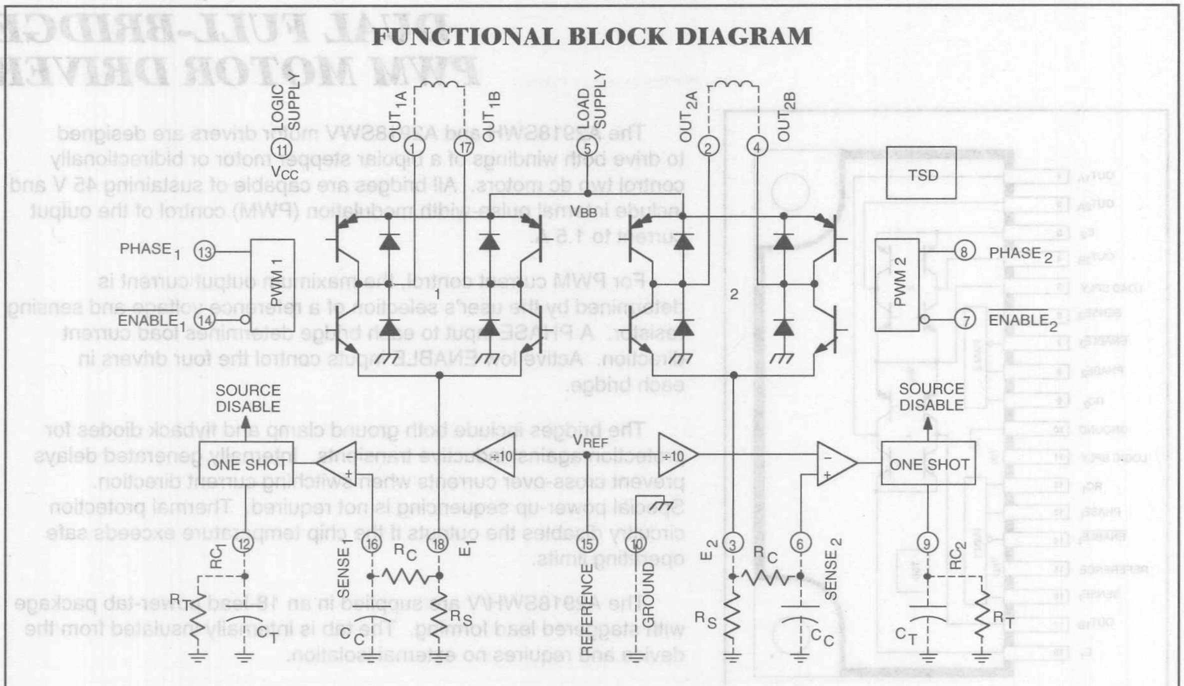
FEATURES

- ±1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Clamp Diodes
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3718 or Dual PBL3770

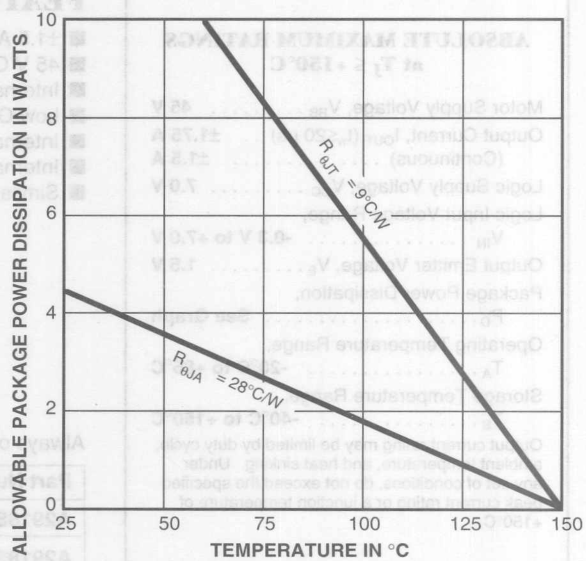
Always order by complete part number:

Part Number	Application
A2918SWH	**For Horizontal Mount**
A2918SWV	**For Vertical Mount**

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-033



Dwg. GP-043

TRUTH TABLE

Enable	Phase	Out_A	Out_B
L	H	H	L
L	L	L	H
H	X	Z	Z

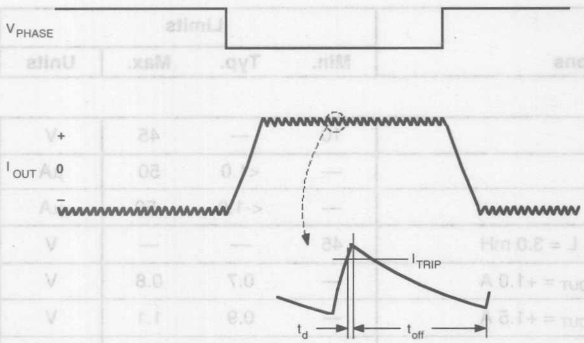
X = Don't care
Z = High impedance

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	µA
		V_{OUT} = 0	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±1.5 A, L = 3.0 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +1.0 A	—	0.7	0.8	V
		Sink Driver, I_{OUT} = +1.5 A	—	0.9	1.1	V
		Source Driver, I_{OUT} = -1.0 A	—	1.8	2.0	V
		Source Driver, I_{OUT} = -1.5 A	—	1.9	2.2	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.5 A	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	12	15	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	8.0	10	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	V_{CC}	V
Current Limit Threshold	V_{REF}/V_{SENSE}	At Trip Point	9.5	10	10.5	—
Thermal Shutdown Temp.	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	V_{EN} = 0.8 V, No Load	—	105	140	mA
	$I_{CC(OFF)}$	V_{EN} = 2.4 V, No Load	—	10	12	mA

Negative current is defined as coming out of (sourcing) the specified device pin.
Typical Data is for design information only.

PWM OUTPUT CURRENT WAVEFORM



Dwg. WM-003-1A

APPLICATIONS INFORMATION

PWM Current Control:

The A2918SWH/V dual bridges are designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), an internal comparator, and an internal monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and it is sensed by R_S until the sense voltage (V_{SENSE}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

The comparator then triggers the monostable which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of internal logic and switching delays. This delay (t_d) is 2 µs typically. After turn-off, the motor current decays, circulating through the ground clamp diode and sink transistor. The source driver's OFF time t_{off}, and therefore the magnitude of the current decrease, is determined by the monostable's external RC timing components, where $t_{off} = R_T C_T$ within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF.

When the source driver is re-enabled, the winding current (the sense voltage) again is allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Special circuitry has been included to prevent runaway current control when t_{off} is set too short. This circuitry prevents the source driver from being re-enabled until the load current has decayed to below the I_{TRIP} level.

Loads with high distributed capacitances may result in high turn-ON current peaks. This peak, appearing across R_S, will attempt to trip the comparator, resulting in possible erroneous current control or high-frequency oscillations. An external $R_C C_C$ low-pass filter may be used to delay the action of the comparator, and thus ignore turn-on spikes.

General:

To avoid excessive voltage spikes on the LOAD SUPPLY pin (V_{BB}), a large-value capacitor (≥47 μF) should be connected from V_{BB} to the ground pin as close as possible to the device. Under no circumstances should the voltage at V_{BB} exceed 45 V.

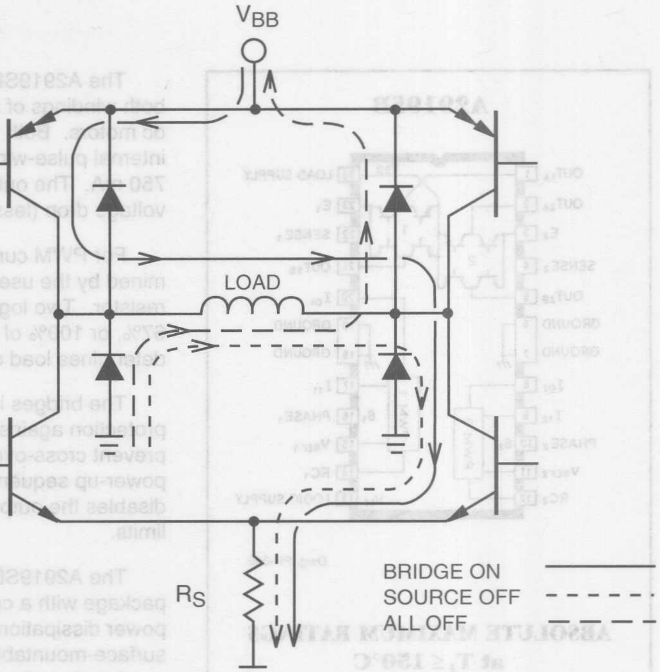
The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime, of approximately 3 μs, prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned OFF, with $V_{EN} \geq 2.4$, resulting in a fast current decay through the internal ground clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The ENABLE input must be tied low if it is not used.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches approximately +170°C. It is intended only to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to approximately +145°C.

LOAD CURRENT PATHS



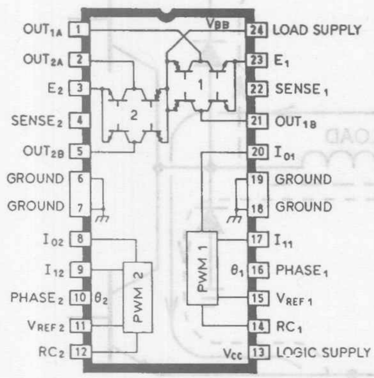
Dwg. EP-006-1

2919

29319.21

DUAL FULL-BRIDGE PWM MOTOR DRIVER

A2919SB



Dwg. PP-006

ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Motor Supply Voltage, V_{BB} .... **45 V**
Output Current, I_{OUT}
(Peak, $t_w \leq 20$ µs) .... **±1.0 A**
(Continuous) .... **±750 mA**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E .... **1.5 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The A2919SB and A2919SLB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output-saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0%, 41%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The A2919SB is supplied in a 24-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. The A2919SLB is supplied in a 24-lead surface-mountable SOIC. Their batwing construction provides for maximum package power dissipation in the smallest possible construction. For applications not requiring quarter-step operation, but desire lower detent or running current, the similar UDN2916B/EB/LB may be preferred.

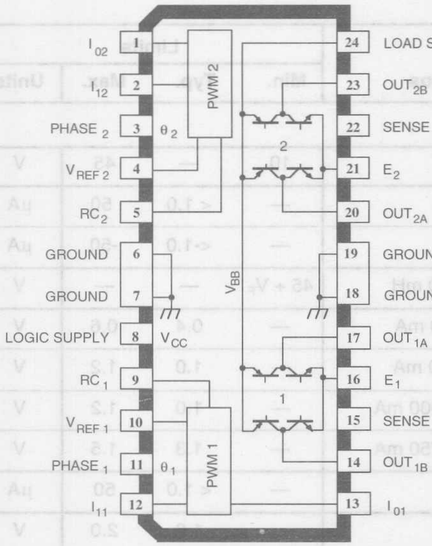
FEATURES

- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Half- or Quarter-Step Operation of Bipolar Stepper Motors

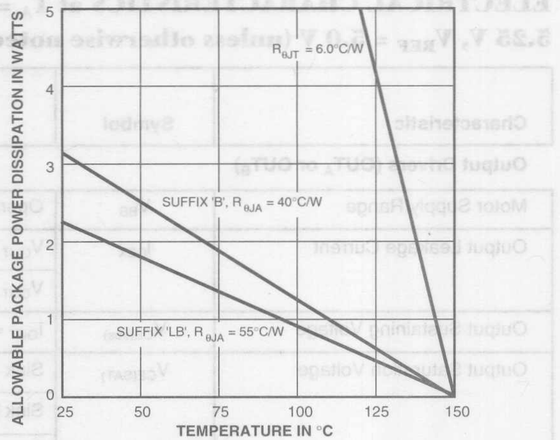
Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JT}$
A2919SB	24-Pin DIP	40°C/W	6.0°C/W
A2919SLB	24-Lead SOIC	50°C/W	6.0°C/W

A2919SLB



Dwg. PP-047

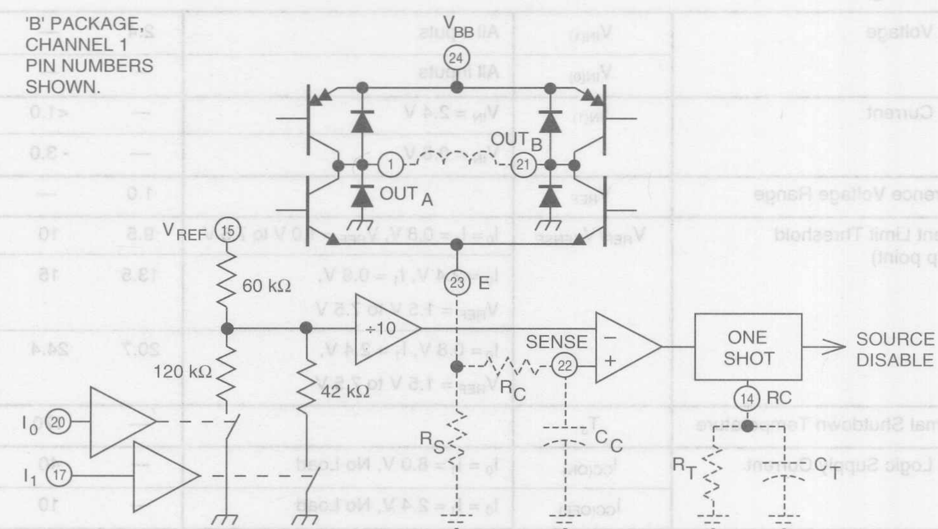


DWG. GP-049A

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007-3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ 150°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}	Operating	10	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	< 1.0	50	µA
		V_{OUT} = 0	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±750 mA, L = 3.0 mH	45 + V_F	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +500 mA	—	0.4	0.6	V
		Sink Driver, I_{OUT} = +750 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -500 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -750 mA	—	1.3	1.5	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	< 1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges ON, No Load	—	20	25	mA
	$I_{BB(OFF)}$	Both Bridges OFF	—	5.0	10	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All inputs	2.4	—	—	V
	$V_{IN(0)}$	All inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
		V_{IN} = 0.8 V	—	- 3.0	-200	µA
Reference Voltage Range	V_{REF}		1.0	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{SENSE}	$I_0 = I_1$ = 0.8 V, V_{REF} = 1.0 V to 7.5 V	9.5	10	10.5	—
		I_0 = 2.4 V, I_1 = 0.8 V, V_{REF} = 1.5 V to 7.5 V	13.5	15	16.5	—
		I_0 = 0.8 V, I_1 = 2.4 V, V_{REF} = 1.5 V to 7.5 V	20.7	24.4	28.0	—
Thermal Shutdown Temperature	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	$I_0 = I_1$ = 8.0 V, No Load	—	40	50	mA
	$I_{CC(OFF)}$	$I_0 = I_1$ = 2.4 V, No Load	—	10	12	mA
Total Reference Current	$I_{REF1} + I_{REF2}$	$V_{REF1} = V_{REF2}$ = 7.5 V, $I_0 = 1_1$ = 2.4 V	140	185	250	µA

APPLICATIONS INFORMATION

PWM CURRENT CONTROL

The A2919SB/SLB dual bridges are designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

When the bridge is turned ON, current increases in the motor winding and flows through the external sense resistor until the sense voltage (V_S) reaches the level set at the comparator's input:

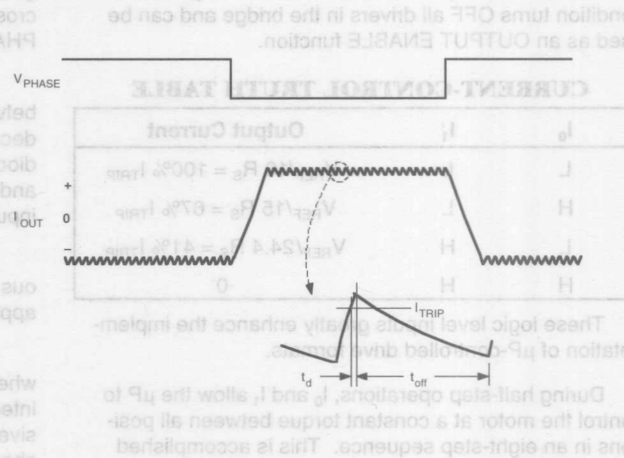
$$I_{TRIP} = V_{REF}/10\ R_S$$

The comparator then triggers the monostable, which turns OFF the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_T C_T$ within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

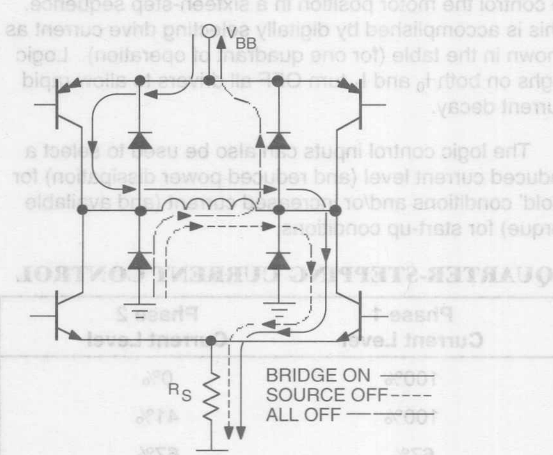
Loads with high distributed capacitances may cause current spikes capable of tripping the comparator, resulting in erroneous current control. An external $R_C C_C$ time delay should be used to delay the action of the comparator. Depending on load type, many applications will not require these external components (SENSE connected to E).

PWM OUTPUT CURRENT WAVE FORM



Dwg. WM-003-1A

LOAD CURRENT PATHS



Dwg. EP-006-1

LOGIC CONTROL OF OUTPUT CURRENT

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 41%, or 0% of the maximum level per the table. The 0% output current condition turns OFF all drivers in the bridge and can be used as an OUTPUT ENABLE function.

CURRENT-CONTROL TRUTH TABLE

I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S$ = 100% I_{TRIP}
H	L	$V_{REF}/15\ R_S$ = 67% I_{TRIP}
L	H	$V_{REF}/24.4\ R_S$ = 41% I_{TRIP}
H	H	0

These logic level inputs greatly enhance the implementation of μP-controlled drive formats.

During half-step operations, I_0 and I_1 allow the μP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is ON and 67% drive current when two phases are ON. Logic highs on both I_0 and I_1 turn OFF all drivers to allow rapid current decay.

During quarter-step operation, I_0 and I_1 allow the μP to control the motor position in a sixteen-step sequence. This is accomplished by digitally selecting drive current as shown in the table (for one quadrant of operation). Logic highs on both I_0 and I_1 turn OFF all drivers to allow rapid current decay.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

QUARTER-STEPPING CURRENT CONTROL

Phase 1 Current Level	Phase 2 Current Level
100%	0%
100%	41%
67%	67%
41%	100%
0%	100%

GENERAL

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 μs) prevents crossover currents that can occur when switching the PHASE input.

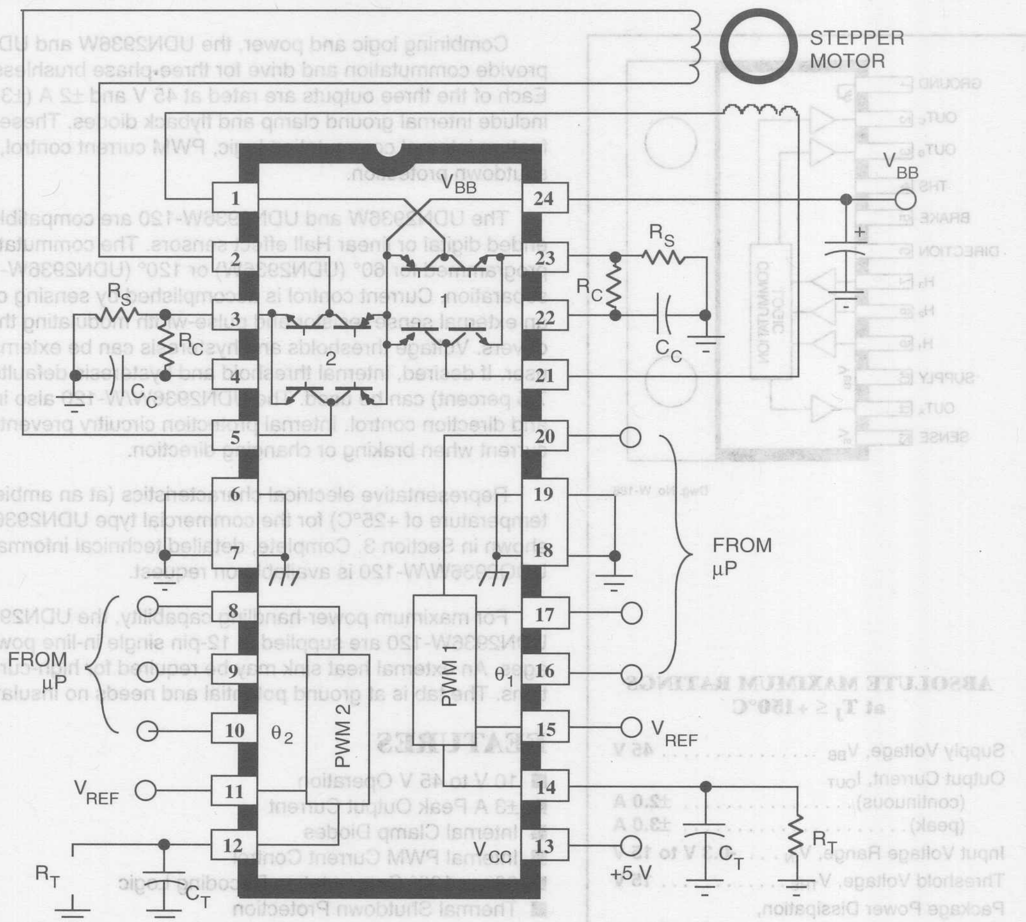
All four drivers in the bridge output can be turned OFF between steps ($I_0 = I_1 \geq 2.4$ V) resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, I_0, and I_1 inputs float high.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for micro-stepping applications.

Thermal protection circuitry turns OFF all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

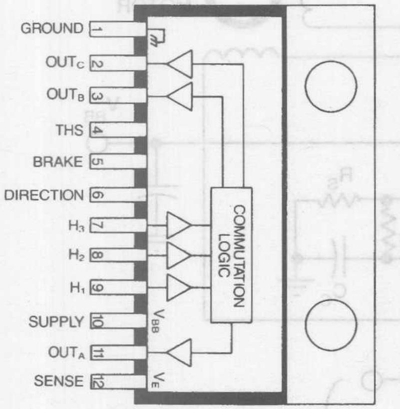
The A2919SB/SLB output drivers are optimized for low output saturation voltages—less than 1.8 V total (source plus sink) at 500 mA. Under normal operating conditions, when combined with the excellent thermal properties of the batwing package design, this allows continuous operation of both bridges simultaneously at 500 mA.

TYPICAL APPLICATION



Dwg. EP-008B

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS



Dwg. No W-188

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{BB} . . . . **45 V**
Output Current, I_{OUT}
(continuous) . . . . **±2.0 A**
(peak) . . . . **±3.0 A**
Input Voltage Range, V_{IN} . . . **-0.3 V to 15 V**
Threshold Voltage, V_{THS} . . . . **15 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Note: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

Combining logic and power, the UDN2936W and UDN2936W-120 provide commutation and drive for three-phase brushless dc motors. Each of the three outputs are rated at 45 V and ±2 A (±3 A peak), and include internal ground clamp and flyback diodes. These drivers also feature internal commutation logic, PWM current control, and thermal shutdown protection.

The UDN2936W and UDN2936W-120 are compatible with single-ended digital or linear Hall effect sensors. The commutating logic is programmed for 60° (UDN2936W) or 120° (UDN2936W-120) electrical separation. Current control is accomplished by sensing current through an external sense resistor and pulse-width modulating the source drivers. Voltage thresholds and hysteresis can be externally set by the user. If desired, internal threshold and hysteresis defaults (300 mV, 7.5 percent) can be used. The UDN2936W/W-120 also include braking and direction control. Internal protection circuitry prevents crossover current when braking or changing direction.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2936W/W-120 are shown in Section 3. Complete, detailed technical information on the UDQ2936W/W-120 is available on request.

For maximum power-handling capability, the UDN2936W and UDN2936W-120 are supplied in 12-pin single in-line power tab packages. An external heat sink may be required for high-current applications. The tab is at ground potential and needs no insulation.

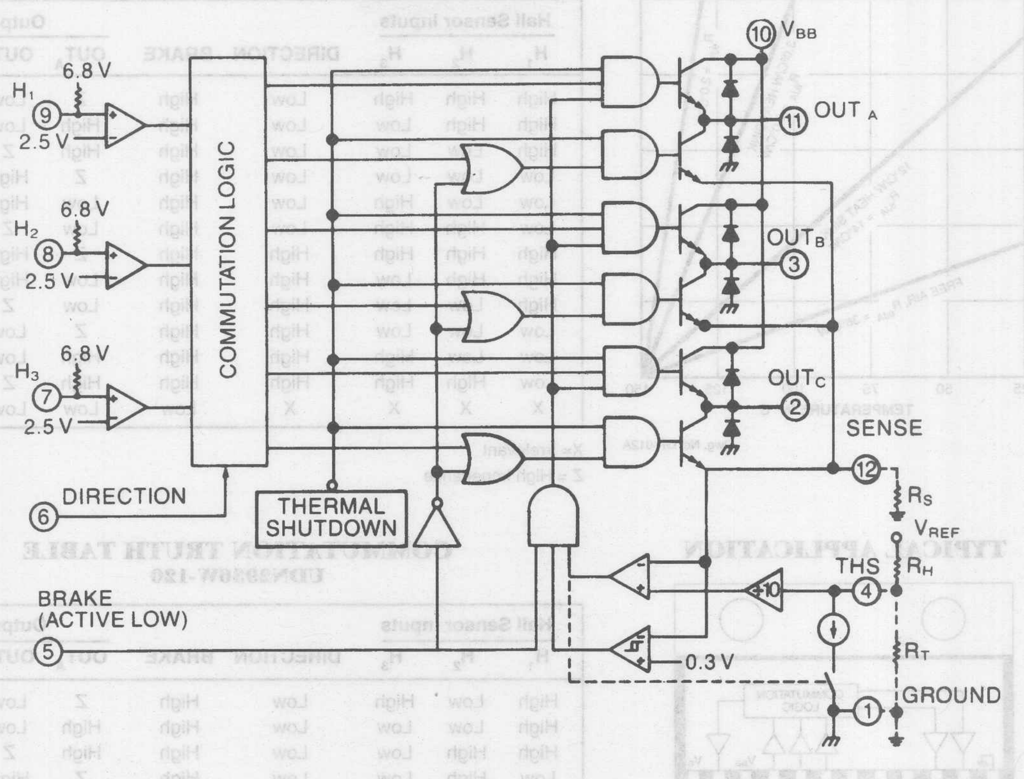
FEATURES

- 10 V to 45 V Operation
- ±3 A Peak Output Current
- Internal Clamp Diodes
- Internal PWM Current Control
- 60° or 120° Commutation Decoding Logic
- Thermal Shutdown Protection
- Compatible with Single-Ended or Differential Hall Effect Sensors
- Braking and Direction Control

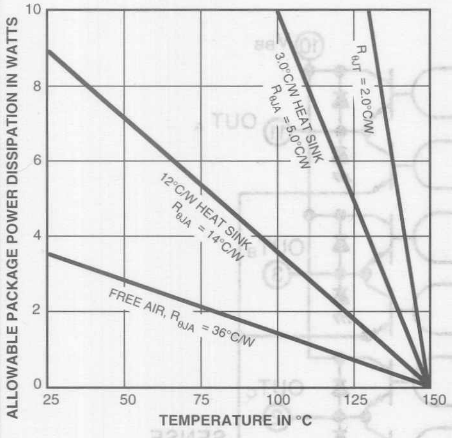
Always order by complete part number:

Part Number	Sensor Inputs
UDN2936W	Single-Ended, 60° Separation
UDN2936W-120	Single-Ended, 120° Separation

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. W-190A



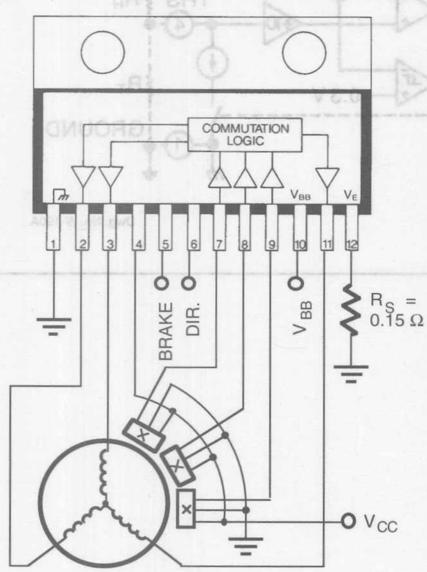
Dwg. No. GP-012A

COMMUTATION TRUTH TABLE
UDN2936W

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	OUT_A	OUT_B	OUT_C
High	High	High	Low	High	Z	Low	High
High	High	Low	Low	High	High	Low	Z
High	Low	Low	Low	High	High	Z	Low
Low	Low	Low	Low	High	Z	High	Low
Low	Low	High	Low	High	Low	High	Z
Low	High	High	Low	High	Low	Z	High
High	High	High	High	High	Z	High	Low
High	High	Low	High	High	Low	High	Z
High	Low	Low	High	High	Low	Z	High
Low	Low	Low	High	High	Z	Low	High
Low	Low	High	High	High	High	Low	Z
Low	High	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X= Irrelevant
Z = High Impedance

TYPICAL APPLICATION



Dwg. No. EP-033

COMMUTATION TRUTH TABLE
UDN2936W-120

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	DIRECTION	BRAKE	OUT_A	OUT_B	OUT_C
High	Low	High	Low	High	Z	Low	High
High	Low	Low	Low	High	High	Low	Z
High	High	Low	Low	High	High	Z	Low
Low	High	Low	Low	High	Z	High	Low
Low	High	High	Low	High	Low	High	Z
Low	Low	High	Low	High	Low	Z	High
High	Low	High	High	High	Z	High	Low
High	Low	Low	High	High	Low	High	Z
High	High	Low	High	High	Low	Z	High
Low	High	Low	High	High	Z	Low	High
Low	High	High	High	High	High	Low	Z
Low	Low	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X= Irrelevant
Z = High Impedance

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_J \leq +150°C$, $V_{BB} = 45$ V

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{BB}	Operating	10	—	45	V
Supply Current	I_{BB}	Outputs Open	—	32	40	mA
		$V_{BRAKE} = 0.8$ V	—	42	50	mA
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	25	—	°C
Output Drivers						
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	—	50	µA
		$V_{OUT} = 0$ V	—	—	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = -1$ A	—	1.7	1.9	V
		$I_{OUT} = +1$ A	—	1.1	1.3	V
		$I_{OUT} = -2$ A	—	1.9	2.1	V
		$I_{OUT} = +2$ A	—	1.4	1.6	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = \pm 2$ A, L = 2 mH	45	—	—	V
Clamp Diode Forward Voltage	V_F	$I_F = 2$ A	—	1.8	2.0	V
Clamp Diode Leakage Current	I_R	$V_R = 45$ V	—	—	50	µA
Output Switching Time	t_r	$I_{OUT} = \pm 2$ A, Resistive Load	—	2.0	—	µs
	t_f	$I_{OUT} = \pm 2$ A, Resistive Load	—	2.0	—	µs
Turn-ON Delay (Resistive Load)	t_{on}	Source Drivers, 0 to -2 A	—	1.25	—	µs
		Sink Drivers, 0 to +2 A	—	1.9	—	µs
Turn-OFF Delay (Resistive Load)	t_{off}	Source Drivers, -2 A to 0	—	1.7	—	µs
		Sink Drivers, +2 A to 0	—	0.9	—	µs

Continued next page...

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_J \leq +150°C$, $V_{BB} = 45$ V continued

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	V_{DIR} or V_{BRAKE}	2.0	—	—	V
	$V_{IN(0)}$	V_{DIR} or V_{BRAKE}	—	—	0.8	V
Sensor Input Voltage Threshold	V_{IN}	H_1, H_2, or H_3	—	2.5	—	V
Input Current	$I_{IN(1)}$	V_{DIR} = 2 V	—	150	200	µA
		V_{BRAKE} = 2 V	—	<1.0	5.0	µA
		V_H = 5 V	—	-190	-220	µA
	$I_{IN(0)}$	V_{DIR} = 0.8 V	—	35	50	µA
		V_{BRAKE} = 0.8 V	—	-5.0	-20	µA
		V_H = 0.8 V	—	-0.64	-1.0	mA
	I_{THS}	$V_{THS} \geq 3.0$ V	—	-8.0	-15	µA
		$V_{THS} < 3.0$ V, $V_{SENSE} < V_{THS}/10.5$	—	-15	-30	µA
		$V_{THS} < 3.0$ V, $V_{SENSE} > V_{THS}/9.5$	190	250	310	µA
Current Limit Threshold		V_{THS}/V_{SENSE} at trip point, $V_{THS} < 3.0$ V	9.5	10	10.5	—
Default Sense Trip Voltage	V_{SENSE}	$V_{THS} \geq 3.0$ V	270	300	330	mV
Default Hysteresis		$V_{THS} \geq 3.0$ V	—	7.5	—	%
Deadtime	t_d	BRAKE or DIRECTION	—	2.0	—	µs

APPLICATIONS INFORMATION

The UDN2936W and UDN2936W-120 power drivers provide commutation logic and power outputs to drive three-phase brushless dc motors.

The UDN2936W and UDN2936W-120 are designed to interface with single-ended linear or digital Hall effect devices (HEDs). Internal pull-up resistors allow for direct use with open-collector digital HEDs. The H_N inputs have 2.5 V thresholds.

The commutation logic provides decoding for HEDs with 60° (UDN2936W) or 120° (UDN2936W-120) electrical separation. At any one step in the logic sequencing, one half-bridge driver is sourcing current, one driver is sinking current, and one driver is in a high-impedance state (see Truth Table).

A logic low on the BRAKE pin turns ON the three sink drivers and turns OFF the three source drivers, essentially shorting the motor windings to ground. During braking, the back-electromotive force generated by the motor produces a current which dynamically brakes the motor. Depending upon the rotational velocity of the motor, this current can approach the locked rotor current level (which is limited only by the motor winding resistance). During braking the output current limiting circuitry is disabled and care should be taken to ensure that the back-EMF generated brake current does not exceed the maximum rating (3 A peak) of the sink drivers and ground clamp diodes.

Changing the logic level of the DIRECTION pin inverts the output states, thus reversing the direction of the motor. Changing the direction of a rotating motor produces a back-EMF current similar to when braking the motor. The load current should not be allowed to exceed the maximum rating (±3 A peak) of the drivers.

An internally generated dead time (t_d) of approximately 2 µs prevents potentially destructive crossover currents that can occur when changing direction or braking.

Motor current is internally controlled by pulse-width modulating the source drivers with a preset hysteresis format. Load current through an external sense resistor (R_S) is constantly monitored. When the current reaches the set trip point (determined by an external reference voltage or internal default), the source driver is disabled. Current recirculates through the ground clamp diode, motor winding, and sink driver. An internal constant-current sink reduces the trip point (hysteresis). When the decaying current reaches this lower threshold, the source driver is enabled again and the cycle repeats.

Thresholds and hysteresis can be set with external resistors or internal defaults can be used. With $V_{THS} > 3.0$ V, the trip point is internally set at 300 mV with 7.5% hysteresis. Load current is then determined by the equation:

$$I_{TRIP} = 0.3/R_S$$

With $V_{THS} < 3.0$ V, the threshold, hysteresis percentage, and peak current are set with external resistors according to the equations:

$$\text{Threshold Voltage } (V_{THS}) = V_{REF} \bullet R_T/(R_H + R_T)$$

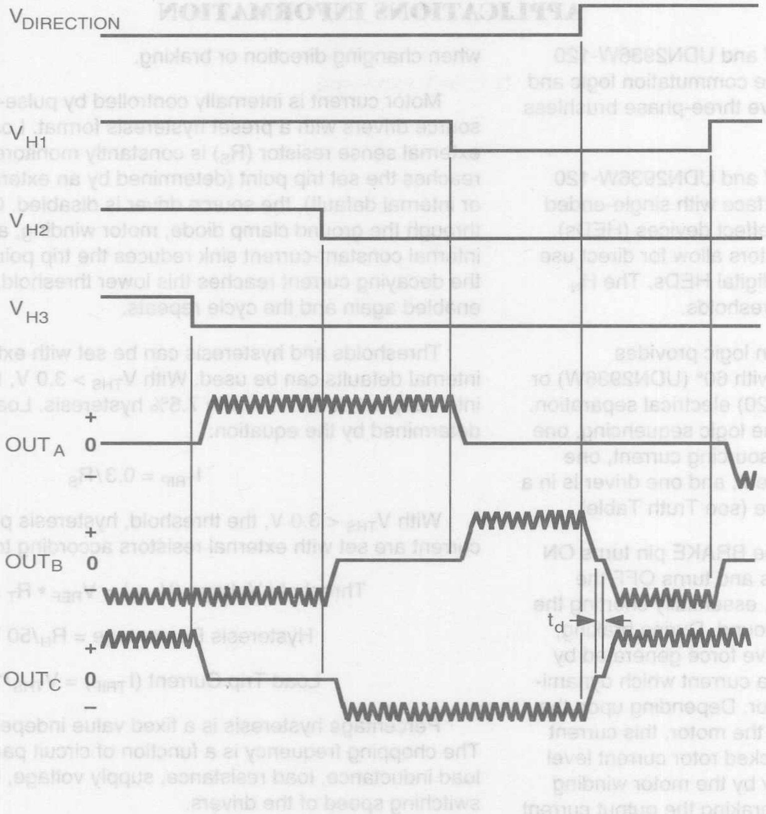
$$\text{Hysteresis Percentage} = R_H/50\ V_{REF}$$

$$\text{Load Trip Current } (I_{TRIP}) = V_{THS}/10\ R_S$$

Percentage hysteresis is a fixed value independent of load current. The chopping frequency is a function of circuit parameters including load inductance, load resistance, supply voltage, hysteresis, and switching speed of the drivers.

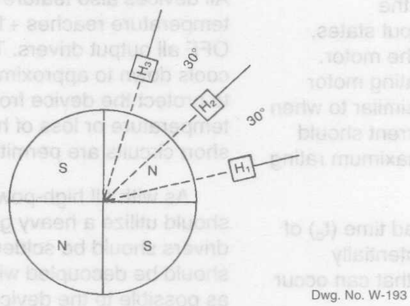
The UDN2936W and UDN2936W-120 outputs are rated for normal operating currents of up to ±2 A and startup currents to ±3 A (see cautions above regarding braking and changing of motor direction). Internal power ground clamp and flyback diodes protect the outputs from the voltage transients that occur when switching inductive loads. All devices also feature thermal protection circuitry. If the junction temperature reaches +165°C, the thermal shutdown circuitry turns OFF all output drivers. The outputs are re-enabled when the junction cools down to approximately +140°C. This protection is only intended to protect the device from failures due to excessive junction temperature or loss of heat sinking and should not imply that output short circuits are permitted.

As with all high-power integrated circuits, the printed wiring board should utilize a heavy ground plane. For optimum performance, the drivers should be soldered directly into the board. The power supply should be decoupled with an electrolytic capacitorb (>10 µF) as close as possible to the device supply pin (V_{BB}).



Dwg. No. WM-002-1

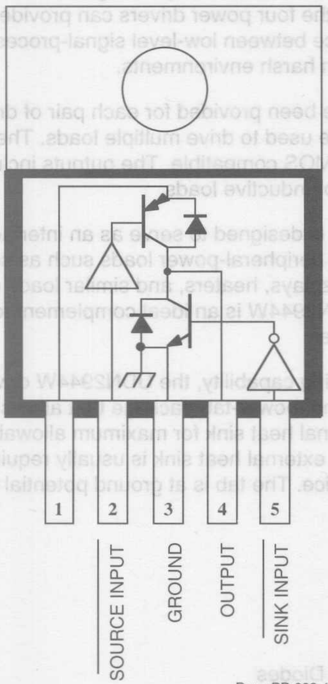
TYPICAL HALL EFFECT SENSOR LOCATIONS



Dwg. No. W-193

2943

HIGH-CURRENT HALF-BRIDGE MOTOR DRIVER



Dwg. PP-022-1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Range V_S .... **8.5 V to 35 V***
Output Voltage, $V_{CE(sus)}$ .... **18 V**
Input Voltage Range, V_{IN} .... **-0.3 V to +18 V**
Continuous Output Current, I_{OUT} ...... **±1.0 A**
Operating Temperature Range, T_A
  Prefix 'UDN' .... **-20°C to +85°C**
  Prefix 'UDQ' .... **-40°C to +85°C**
Storage Temperature Range,
  T_S .... **-55°C to +150°C**

*Internal high-voltage shutdown above 24 V.

Designed for use as a general-purpose motor driver, the UDN and UDQ2943Z half-bridge drivers combine high-current sink and source drivers with logic stages, level shifting, diode transient protection, and a voltage regulator for single-supply operation. Capable of operating in extremely harsh environments, this device can withstand high ambient temperatures, output overloads, and repeated power supply transient voltages without damage. The driver can be used in pairs for full-bridge operation, or in triplets in three-phase brushless dc motor-drive applications. Complete, detailed technical information is given in Section 5.

The input circuitry is compatible with TTL and low-voltage CMOS logic. Logic lockout prevents both source and sink drivers from turning ON simultaneously. Each driver is turned ON by an active-low input, making the UDN/UDQ2943Z especially appropriate in many microprocessor applications. An accidental input open circuit will turn OFF the corresponding output. The device also provides an internally-generated dead time to prevent crossover currents during output switching. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Saturated sink output drivers provide for low saturation voltage at the maximum rated current. Internal short-circuit protection, activated at load currents above 1 A, protects the source driver from accidental short-circuits between the output and ground.

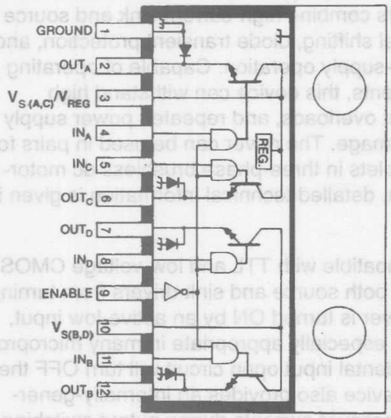
The UDN/UDQ2943Z driver is rated for continuous operation with inductive loads at supply voltages of up to 24 V. With supply voltage transients (to 35 V maximum), a high-voltage protection circuit becomes operative, shutting OFF both output drivers. The internal thermal shutdown is triggered by a nominal junction temperature of 160°C.

Single-chip construction and a 5-lead power-tab TS-001 plastic package provide cost-effective and reliable systems designs. It also features excellent power dissipation ratings, minimum size, and ease of installation. The heat-sink tab is at ground potential and does not require insulation.

FEATURES

- ±1 A Output Current
- Saturated Output Drivers
- Logic-Compatible Inputs
- Output-Transient Protection
- Tri-State Output
- 8.5 V to 24 V Operating Range
- Crossover-Current Protected
- Withstands 35 V Supply Transients
- Internal Over-Voltage Protection
- Internal Short-Circuit Protection

QUAD HIGH-CURRENT, HIGH-VOLTAGE SOURCE DRIVER



Dwg. No. A-13,054

Capable of driving loads to 4 A at supply voltages to 60 V (inductive loads to 35 V), the UDN2944W is a quad high-current, high-voltage source driver. Each of the four power drivers can provide space- and cost-saving interface between low-level signal-processing circuits and high-power loads in harsh environments.

Individual supply lines have been provided for each pair of drivers so that different supplies can be used to drive multiple loads. The controlling inputs are TTL or CMOS compatible. The outputs include transient-suppression diodes for inductive loads.

This quad Darlington array is designed to serve as an interface between low-level circuitry and peripheral-power loads such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 240 W per channel. The UDN2944W is an ideal complement to the UDN2878W quad 4 A sink driver.

For maximum power-handling capability, the UDN2944W driver is supplied in a 12-pin single in-line, power-tab package that allows efficient attachment of an external heat sink for maximum allowable package power dissipation. An external heat sink is usually required for proper operation of this device. The tab is at ground potential and needs no insulation.

FEATURES

- Output Current to 4 A
- Output Voltage to 60 V
- Loads to 960 W
- Integral Output Suppression Diodes
- TTL and CMOS Compatible Inputs
- Plastic Single In-Line Package
- Heat-Sink Tab

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Supply Voltage Range, V_S .... **10 V to 60 V**

Output Current, I_{OUT}

(dc) .... **-4 A**

(peak) .... **-5 A**

Input Voltage, V_{IN} .... **15 V**

Package Power Dissipation,

P_D .... **See Graph**

Operating Temperature Range,

T_A .... **-20°C to +85°C**

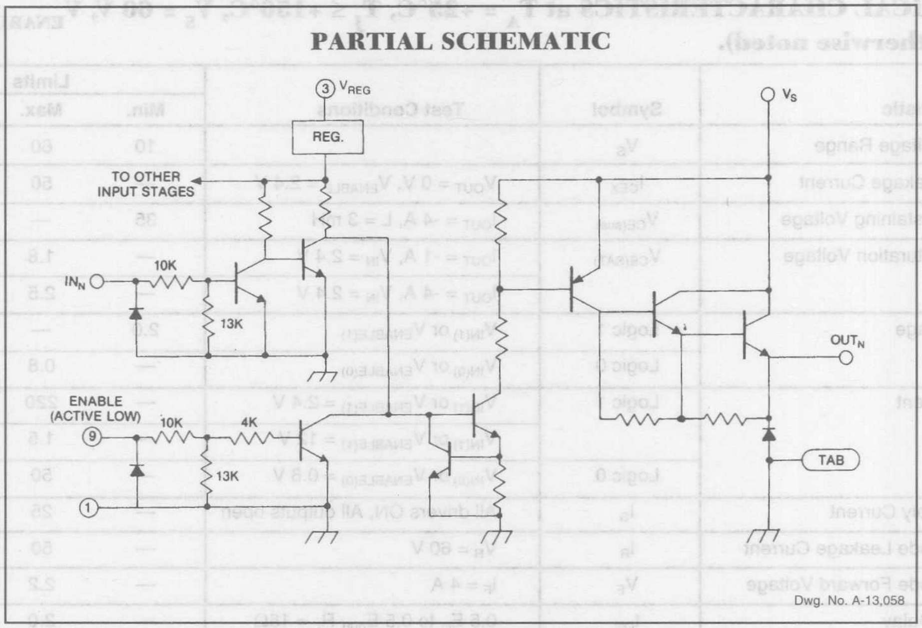
Storage Temperature Range,

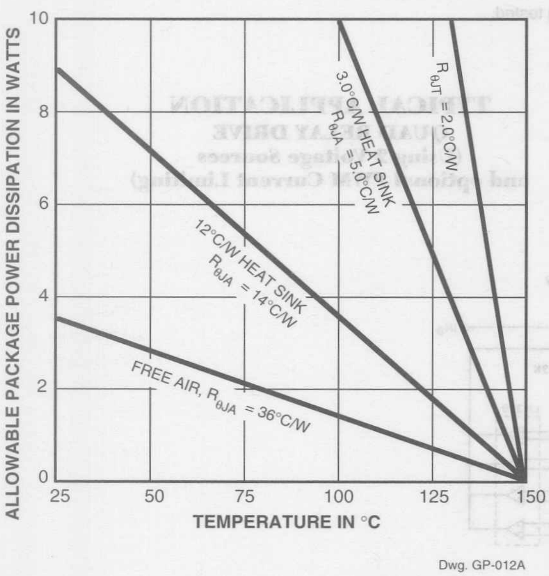
T_S .... **-55°C to +150°C**

Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the -5.0 A peak current and a junction temperature of +150°C.

Always order by complete part number: **UDN2944W**.

PARTIAL SCHEMATIC





TRUTH TABLE

INPUT	ENABLE	OUTPUT
L	L	L
H	L	H
L	H	L
H	H	L

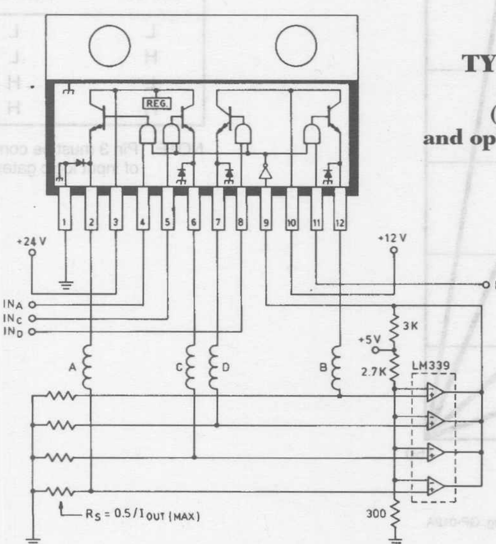
NOTE: Pin 3 must be connected to V_S for operation of input logic gates.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \le$ +150°C, V_S = 60 V, V_{ENABLE} = 0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Supply Voltage Range	V_S		10	60	V
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, V_{ENABLE} = 2.4 V		50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -4 A, L = 3 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -1 A, V_{IN} = 2.4 V	—	1.8	V
		I_{OUT} = -4 A, V_{IN} = 2.4 V	—	2.5	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.4 V	—	220	µA
		$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 12 V	—	1.5	mA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8 V	—	50	µA
Total Supply Current	I_S	All drivers ON, All outputs open	—	25	mA
Clamp Diode Leakage Current	I_R	V_R = 60 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 4 A	—	2.2	V
Turn-On Delay	t_{ON}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	2.0	µs
Turn-Off Delay	t_{OFF}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	10	µs

NOTE: Negative current is defined as coming out of (sourcing) the device being tested.

TYPICAL APPLICATION
QUAD RELAY DRIVE
(Using 2 Voltage Sources and optional PWM Current Limiting)



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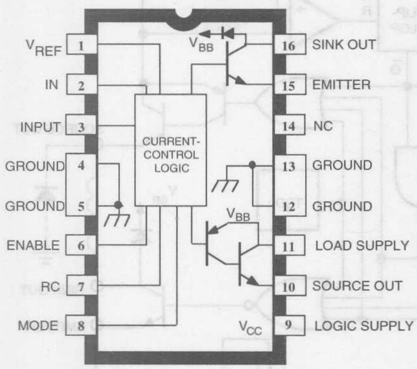
HIGH-CURRENT HALF-BRIDGE PRINTHEAD/MOTOR DRIVER—WITH INTERNAL CURRENT SENSING AND CONTROL

UDN2961B



Dwg. No. PP-035

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{BB} . . . . **45 V**
Output Current, I_{OUT} (continuous) . . **±3.4 A**
($t_w \leq 20\ \mu s$, 10% duty cycle) . . . **±4.0 A**
Logic Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage Range,
V_{IN} . . . . **-0.3 V to +7.0 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Junction Temperature, T_J . . . . **+150°C***
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The UDN2961B and UDN2961W are 3.4 A half bridges designed specifically for driving solenoid printheads, stepper motors, and dc motors. The UDN2961B/W consists of a power source driver output, a power sink driver output, a flyback recovery diode, internal current sensing circuitry, and a user-selectable fixed off-time chopper circuit.

The output drivers are capable of sustaining 45 V with continuous currents of ±3.4 A and peak transient currents of ±4 A permitted. The outputs have been optimized for a low output saturation voltage (typically 2.6 V total source plus sink drops at 3.4 A).

For output current control, load current is sensed internally and limited by chopping the output driver(s) in a user-selectable fixed off-time PWM mode. The maximum output current is determined by the user's selection of a reference voltage. The MODE pin determines whether the current control circuitry will chop in a slow current-decay mode (only the source driver switching) or in a fast current-decay mode (source and sink switching). A user-selectable blanking window prevents false triggering of the current control circuitry during chopping.

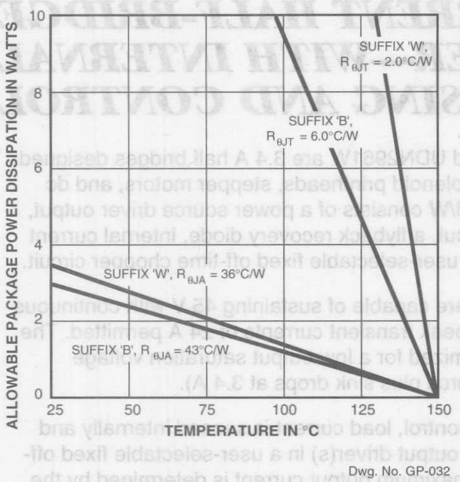
The UDN2961B is supplied in a 16-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. For higher power dissipation requirements, the UDN2961W is supplied in a 12-pin single in-line power tab package.

FEATURES

- 3.4 A, 45 V Source and Sink Drivers
- Internal Current Sensing
- User-Selectable Fixed Off-Time PWM Current Control
- Internal Flyback Diode
- Low Output Saturation Voltage
- Chip Enable
- Fast or Slow Current-Decay Modes
- Programmable Blanking Window
- Internal Thermal Shutdown Circuitry

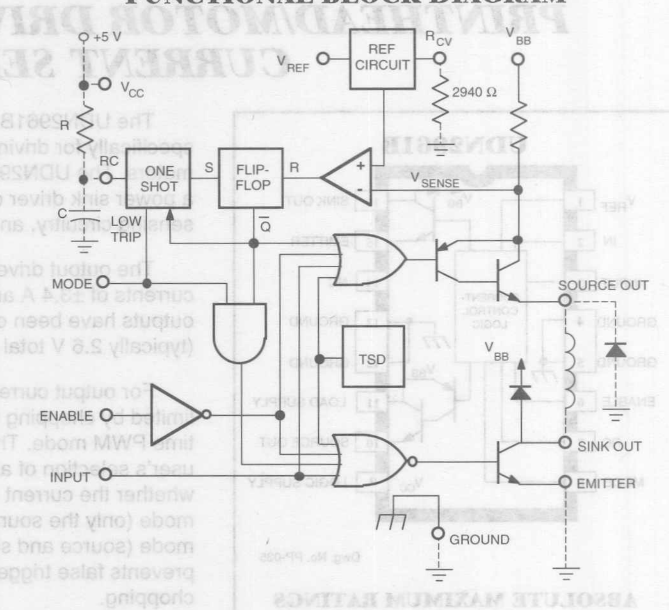
Always order by complete part number:

Part Number	Package
UDN2961B	16-Pin DIP
UDN2961W	12-Pin Power-Tab SIP



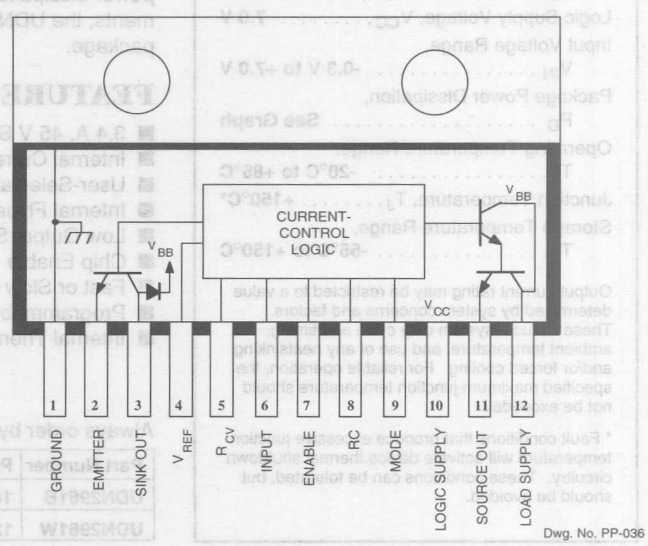
Dwg. No. GP-032

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FP-019A

UDN2961W



Dwg. No. PP-036

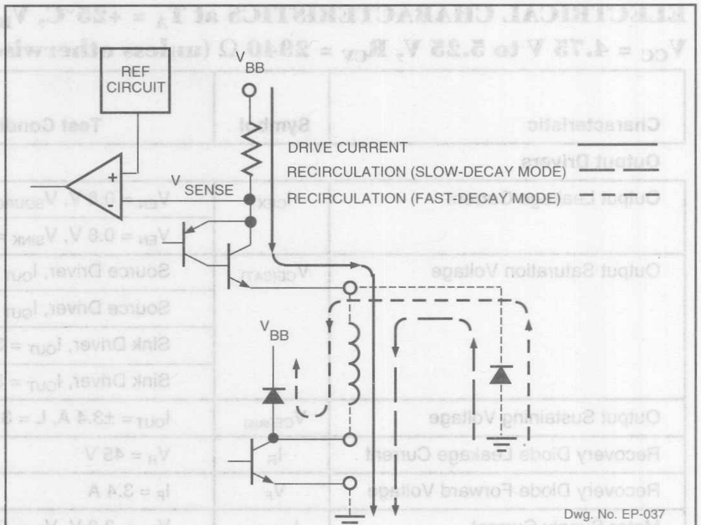
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, R_{CV} = 2940 Ω (unless otherwise noted).

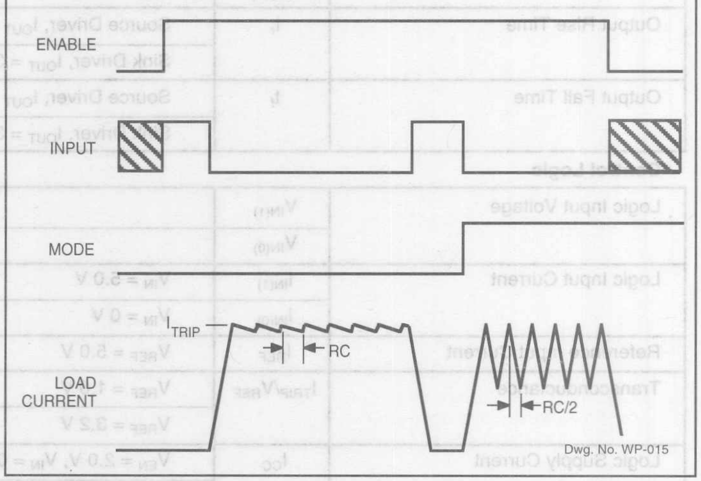
Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers						
Output Leakage Current	I_{CEX}	V_{EN} = 0.8 V, V_{SOURCE} = 0 V	—	<-1.0	-100	µA
		V_{EN} = 0.8 V, V_{SINK} = 45 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -3.4 A	—	1.6	2.2	V
		Source Driver, I_{OUT} = -3.0 A	—	1.5	—	V
		Sink Driver, I_{OUT} = 3.4 A	—	1.0	1.4	V
		Sink Driver, I_{OUT} = 3.0 A	—	0.9	—	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±3.4 A, L = 3 mH	45	—	—	V
Recovery Diode Leakage Current	I_R	V_R = 45 V	—	<1.0	100	µA
Recovery Diode Forward Voltage	V_F	I_F = 3.4 A	—	—	2.0	V
Motor Supply Current	$I_{BB(on)}$	V_{EN} = 2.0 V, V_{IN} = 0.8 V, No Load	—	—	70	mA
	$I_{BB(off)}$	V_{EN} = 0.8 V	—	—	2.5	mA
Output Rise Time	t_r	Source Driver, I_{OUT} = -3.4 A	—	—	600	ns
		Sink Driver, I_{OUT} = 3.4 A	—	—	600	ns
Output Fall Time	t_f	Source Driver, I_{OUT} = -3.4 A	—	—	600	ns
		Sink Driver, I_{OUT} = 3.4 A	—	—	600	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	10	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-1.0	mA
Reference Input Current	I_{REF}	V_{REF} = 5.0 V	—	—	50	µA
Transconductance	I_{TRIP}/V_{REF}	V_{REF} = 1.0 V	0.9	1.0	1.1	A/V
		V_{REF} = 3.2 V	0.9	1.0	1.1	A/V
Logic Supply Current	I_{CC}	V_{EN} = 2.0 V, V_{IN} = 0.8 V, No Load	—	—	160	mA
		V_{EN} = 0.8 V	—	—	15	mA
Turn On Delay	$t_{pd(on)}$	Source Driver	—	—	600	ns
		Sink Driver	—	—	600	ns
Turn Off Delay	$t_{pd(off)}$	Source Driver	—	—	2.0	µs
		Sink Driver	—	—	2.0	µs
Thermal Shutdown Temperature	T_J		—	165	—	°C

Negative current is defined as coming out of (sourcing) the specified device terminal.

APPLICATIONS INFORMATION

The UDN2961B/W is a high current half-bridge designed to drive a number of inductive loads such as printer solenoids, stepper motors, and dc motors. Load current is sensed internally and is controlled by pulse-width modulating (PWM) the output driver(s) in a fixed off-time, variable-frequency format. The peak current level is set by the user's selection of a reference voltage. A slow current-decay mode (chopping only the source driver) or a fast current-decay mode (chopping both the source and sink drivers) can be selected via the MODE pin.





PWM CURRENT CONTROL

A logic low on the MODE pin sets the current-control circuitry into the slow-decay mode. The RS flip-flop is set initially, and both the source driver and the sink driver are turned ON when the INPUT pin is at a logic low. As current in the load increases, it is sensed by the internal sense resistor until the sense voltage equals the trip voltage of the comparator. At this time, the flip-flop is reset and the source driver is turned OFF. Over the range of V_{REF} = 0.8 V to 3.4 V, the output current trip point transfer function is a direct linear function of the reference voltage:

$$I_{TRIP} = V_{REF}$$

To ensure an accurate chop current level (±10%), an external 2940 Ω ±1% resistor (R_{CV}) is used. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays (typically 1.5 µs). After the source driver turns OFF, the load current decays, circulating through an external ground clamp diode, the load, and the sink transistor. The source driver's OFF time (and therefore the magnitude of the current decrease) is determined by the one-shot's external RC timing components:

$$t_{OFF} = RC$$

within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF. When the one-shot times out, the flip-flop is set again, the source driver is re-enabled, and the load current again is allowed to rise to the set peak value and trip the comparator. This cycle repeats itself, maintaining the average load current at the desired level.

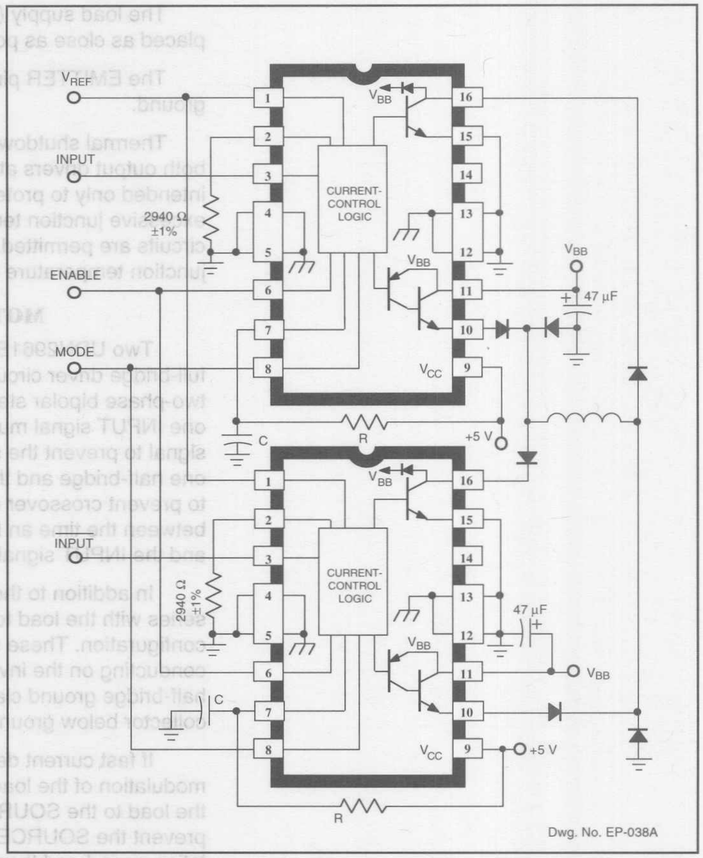
A logic high on the MODE pin sets the current-control circuitry into the fast-decay mode. When the peak current threshold is detected, the flip-flop is reset and both the source driver and the sink driver turn OFF. Load current decays quickly through the external ground clamp diode, the load, and the internal flyback diode. In the fast-decay mode, the OFF time period is one-half the time that is set by the external RC network for the slow-decay mode:

$$t_{OFF} = \frac{RC}{2}$$

The amount of ripple current, when chopping in the fast-decay mode, is considerably higher than when chopping in the slow-decay mode.

The frequency of the PWM current control is determined by the time required for the load current to reach the set peak threshold (a function of the load characteristics and V_{BB}) plus the OFF time of the switching driver(s) (set by the external RC components).

To prevent false resetting of the flip-flop, due to switching transients and noise, a blanking time for the comparator can be set by the user where $t_B \approx 3600 \times C$ in the slow-decay mode or $t_B \approx 2400 \times C$ in the fast-decay mode. For C between 100 pF and 1000 pF, t_B is in µs.



Dwg. No. EP-038A

POWER CONSIDERATIONS

The UDN2961B/W outputs are optimized for low power dissipation. The sink driver has a maximum saturation voltage drop of only 1.4 V at 3.4 A, while the source driver has a 2.2 V drop at -3.4 A. Device power dissipation is minimized in the slow-decay mode, as the chopping driver (the source driver) is ON for less than 50% of the chop period. When the source driver is OFF during a chop cycle, power is dissipated on chip only by the sink driver; the rest of the power is dissipated through the external ground clamp diode. In the fast-decay mode, the ON time of the chopping drivers (both the source driver and the sink driver) may be greater than 50%, and the power dissipation will be greater.

GENERAL

A logic low on the ENABLE pin prevents the source driver and the sink driver from turning ON, regardless of the state of the INPUT pin or the supply voltages. With the ENABLE pin high, a logic low on the INPUT pin turns ON the output drivers.

To protect against inductive load voltage transients, an external ground clamp diode is required. A fast-recovery diode is recommended to reduce power dissipation in the UDN2961B/W. The blanking time prevents false triggering of the current sense comparator, which can be caused by the recovery current spike of the ground clamp diode when the chopping source driver turns ON.

The load supply (V_{BB}) should be well decoupled with a capacitor placed as close as possible to the device.

The EMITTER pin should be connected to a high-current power ground.

Thermal shutdown protection circuitry is activated and turns OFF both output drivers at a junction temperature of typically +165°C. It is intended only to protect the device from catastrophic failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools down to approximately +145°C.

MOTOR DRIVER APPLICATIONS

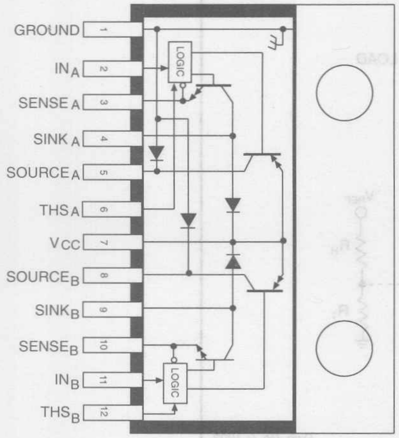
Two UDN2961B/Ws can be cross connected as shown to form a full-bridge driver circuit. Two full-bridge circuits are needed to drive a two-phase bipolar stepper motor. When in a full-bridge configuration, one INPUT signal must be logically inverted from the other INPUT signal to prevent the simultaneous conduction of a source driver from one half-bridge and the sink driver from the other half-bridge. In order to prevent crossover currents, a turn-ON delay time of 3 µs is needed between the time an INPUT signal for one of the half bridges goes high and the INPUT signal for the other half bridge goes low.

In addition to the two external ground clamp diodes, diodes in series with the load to the SINK OUT are needed in a full-bridge configuration. These series diodes prevent the sink drivers from conducting on the inverse mode, which can occur when the opposite half-bridge ground clamp diode is conducting and forces the sink driver collector below ground.

If fast current decay is used (MODE = logic high) or pulse width modulation of the load-current direction is used, diodes in series with the load to the SOURCE OUT are needed. These series diodes prevent the SOURCE OUT from inverse conducting during the recirculation period and thereby prevent shoot-through currents from occuring as the drivers turn back ON.

2962

DUAL SOLENOID/MOTOR DRIVER —PULSE-WIDTH MODULATED CURRENT CONTROL



Dwg. No. D-1001

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{CC}	**45 V**
Peak Output Current, I_{OUT}	**±4 A**
Input Voltage Range, V_{IN}	**-0.3 V to +7.0 V**
Package Power Dissipation, P_D	**See Graph**
Operating Temperature Range, T_A	**-20°C to +85°C**
Storage Temperature Range, T_S	**-55°C to +150°C**

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

Using PWM to minimize power dissipation and maximize load efficiency, the UDN2962W dual driver is recommended for impact printer solenoids and stepper motors. It is comprised of two source/sink driver pairs rated for continuous operation to ±3 A. It can be connected to drive two independent loads or a single load in the full-bridge configuration. Both drivers include output clamp/flyback diodes, input gain and level shifting, a voltage regulator for single-supply operation, and pulse-width modulated output-current control circuitry. Inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The peak output current and hysteresis for each source/sink pair is set independently. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. At the specified output-current trip level, the source driver turns OFF. The internal clamp diode then allows current to flow without additional input from the power supply. When the lower current trip point is reached, the source driver turns back ON.

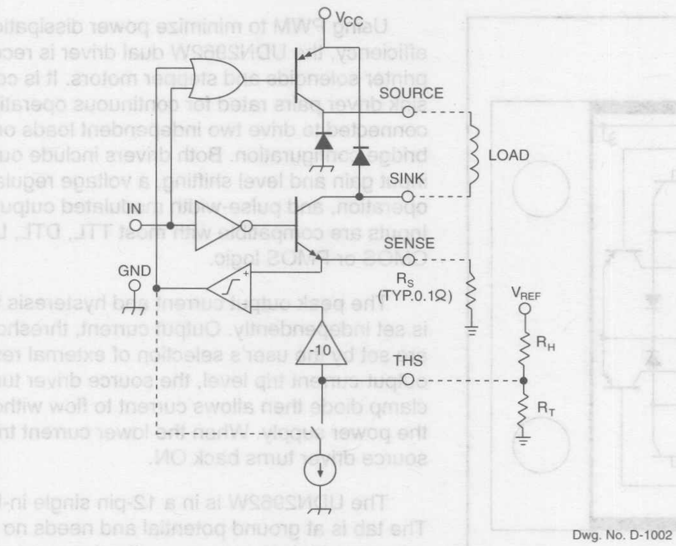
The UDN2962W is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. For high-current or high-frequency applications, external heat sinking may be required.

FEATURES

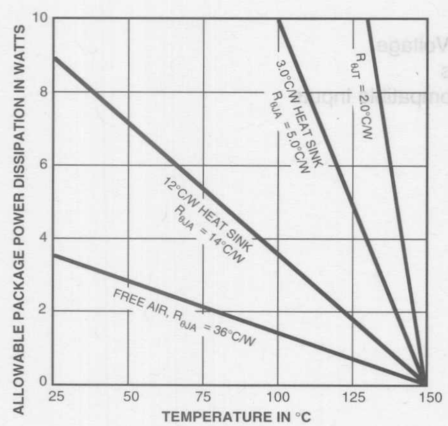
- 4 A Peak Output
- 45 V Min. Sustaining Voltage
- Internal Clamp Diodes
- TTL/PMOS/CMOS Compatible Inputs
- High-Speed Chopper

Always order by complete part number: **UDN2962W** .

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. D-1002



Dwg. GP-012A

TRUTH TABLE

V_{IN}	V_{SENSE}	SOURCE DRIVER	SINK DRIVER
High	NA	Off	Off
Low	$<V_{THS}/10$	On	On
Low	$>V_{THS}/10$	Off	On

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \le$ +150°C, V_{CC} = 45 V, V_{SENSE} = 0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	V_{CC}	Operating	20	—	45	V
Output Drivers						
Output Leakage Current	I_{CEX}	V_{IN} = 2.4 V, V_{SOURCE} = 0 V	—	<-1.0	-100	µA
		V_{IN} = 2.4 V, V_{SINK} = 45 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Drivers, I_{LOAD} = 3.0 A	—	2.1	2.3	V
		Source Drivers, I_{LOAD} = 1.0 A	—	1.7	2.0	V
		Sink Drivers, I_{LOAD} = 3.0 A	—	1.7	2.0	V
		Sink Drivers, I_{LOAD} = 1.0 A	—	1.1	1.3	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±3.0 A, L = 3.5 mH	45	—	—	V
Output Current Regulation	ΔI_{OUT}	V_{THS} = 0.6 V to 1.0 V, L = 3.5 mH	—	—	±25	%
		V_{THS} = 1.0 V to 2.0 V, L = 3.5 mH	—	—	±10	%
		V_{THS} = 2.0 V to 5.0 V, L = 3.5 mH	—	—	±5.0	%
Clamp Diode Forward Voltage	V_F	I_F = 3.0 A	—	1.7	2.0	V
Output Rise Time	t_r	I_{LOAD} = 3.0 A, 10% to 90%, Resistive Load	—	0.5	1.0	µs
Output Fall Time	t_f	I_{LOAD} = 3.0 A, 90% to 10%, Resistive Load	—	0.5	1.0	µs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	1.0	10	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-20	-100	µA
	$I_{THS(ON)}$	$V_{THS} \ge$ 500 mV, $V_{SENSE} \le V_{THS}/10.5$	—	-2.0	—	µA
	$I_{THS(HYS)}$	$V_{SENSE} \ge V_{THS}/9.5$, V_{THS} = 0.6 V to 5.0 V	140	200	260	µA
V_{THS}/V_{SENSE} Ratio	—	At Trip Point, V_{THS} = 2.0 V to 5.0 V	9.5	10	10.5	—
Supply Current (Total Device)	I_{CC}	V_{IN} = 2.4 V, Outputs OFF	—	8.0	12	mA
		V_{IN} = 0.8 V, Outputs Open	—	25	40	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	2.5	µs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	µs
		100% V_{SENSE} to 50% V_{OUT}*	—	—	3.0	µs

* Where $V_{SENSE} \ge V_{THS}/9.5$

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

CIRCUIT DESCRIPTION AND APPLICATIONS INFORMATION

The UDN2962W high-current driver is intended for use as a free-running, pulse-width modulated solenoid driver.

Circuit Description. In operation, the source and sink drivers are both turned ON by a low level at the input. The load current rises with time as a function of the load inductance, total circuit resistance, and supply voltage and is sensed by the external sense resistor (R_S). When the load current reaches the trip point (I_{TRIP}), the comparator output goes high and turns OFF the source driver. The actual load current will peak slightly higher than I_{TRIP} because of the internal logic and switching delays.

After the source driver is turned OFF, the load current continues to circulate through the sink driver and an internal ground clamp diode. The rate of current decay is a function of the load inductance and total circuit resistance.

An internal constant current sink reduces the trip point (hysteresis) until the decaying load current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Load current is again allowed to rise to the trip point and the cycle repeats.

Maximum load current and hysteresis is determined by the user.

Determining Maximum Load Current and Hysteresis. Trip current (I_{TRIP}) is determined as a function of resistance R_S and the threshold voltage, V_{THS}:

$$I_{TRIP} = \frac{V_{THS}}{10\ R_S}$$

where $V_{THS} = 10 \bullet V_{SENSE} = 0.6$ V to 5.0 V.

Hysteresis percentage (H) is determined by resistance R_H and is independent of the load current:

$$H = \frac{R_H}{50 \bullet V_{REF}}$$

The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Resistance R_T is determined as:

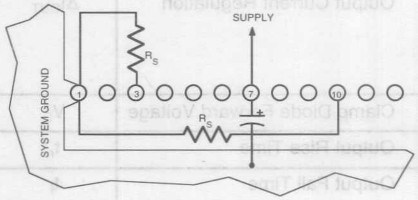
$$R_T = \frac{R_H V_{THS}}{V_{REF} - V_{THS}}$$

Note that if $V_{THS} = V_{REF,}$ then $R_T = \infty$.

Circuit Layout. To prevent interaction between channels, each of the two high-level power ground returns (the low side of the sense resistors) must be returned independently to the low-level signal ground (pin 1). The circuit common (pin 1) can then be routed to the system ground.

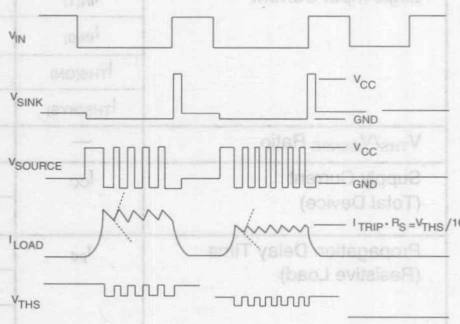
The printed wiring board should utilize a heavy ground plane. For optimum performance, the driver should be soldered directly into the board.

The power supply (V_{CC}) should be decoupled with an electrolytic capacitor (≥10 µF) as close as possible to pin 7.



Dwg. OP-001

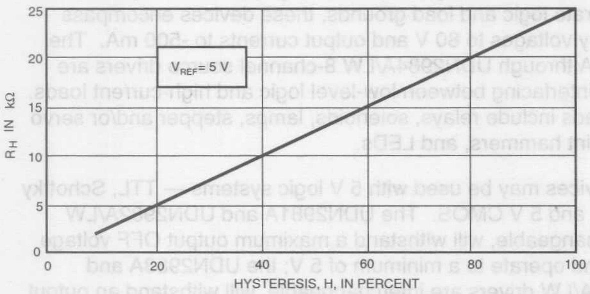
TYPICAL WAVESHAPES



Dwg. WP-006

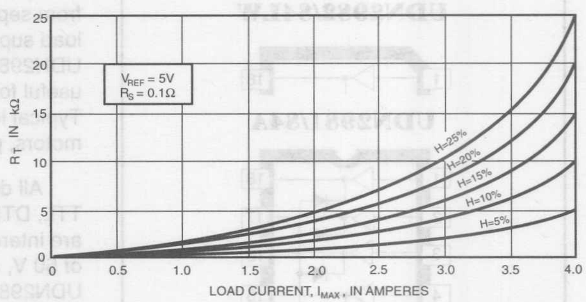
APPLICATIONS INFORMATION

RESISTOR R_H VALUE AS A FUNCTION OF HYSTERESIS

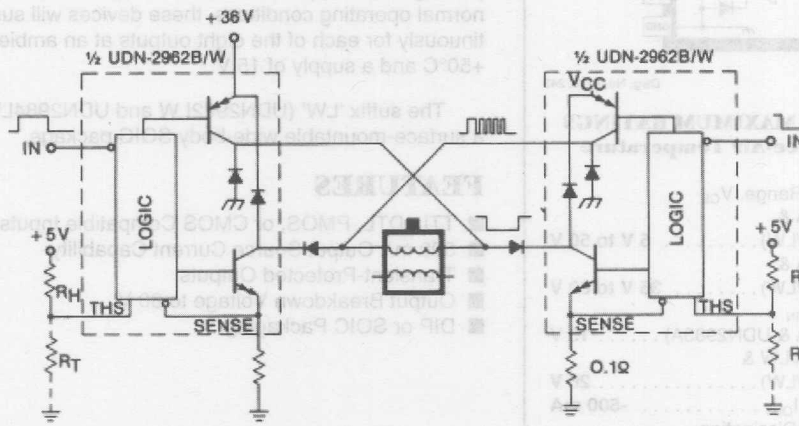


Dwg. No. A-12,417

RESISTOR R_T VALUE AS A FUNCTION OF PEAK LOAD CURRENT



Dwg. No. A-12,416



Dwg. No. D-1004

R_H AND R_T DETERMINE HYSTERESIS AND PEAK CURRENT

NOTE: Each of the drivers includes an internal logic delay to prevent potentially destructive crossover currents within the driver during phase changes. However, never simultaneously enable both inputs in the full-bridge configurations: A destructive short-circuit to ground will result.

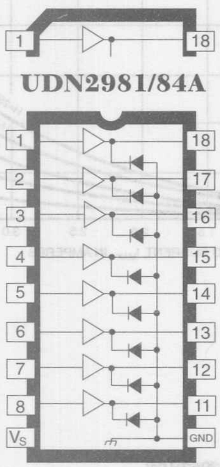
2981 THRU 2984

29310B

8-CHANNEL SOURCE DRIVERS

UDN2982/84LW

UDN2981/84A



Dwg. No. A-10, 243

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage Range, V_{CE}
(UDN2981A & UDN2982A/LW) . . . . **5 V to 50 V**
(UDN2983A & UDN2984A/LW) . . . . **35 V to 80 V**
Input Voltage, V_{IN}
(UDN2981A & UDN2983A) . . . . . . **15 V**
(UDN2982A/LW & UDN2984A/LW) . . . . **20 V**
Output Current, I_{OUT} . . . . **-500 mA**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Note that the UDN2982/84A (dual in-line package) and UDN2982/84LW (small-outline IC package) are electrically identical and share a common terminal number assignment.

Recommended for high-side switching applications that benefit from separate logic and load grounds, these devices encompass load supply voltages to 80 V and output currents to -500 mA. The UDN2981A through UDN2984A/LW 8-channel source drivers are useful for interfacing between low-level logic and high-current loads. Typical loads include relays, solenoids, lamps, stepper and/or servo motors, print hammers, and LEDs.

All devices may be used with 5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. The UDN2981A and UDN2982A/LW are interchangeable, will withstand a maximum output OFF voltage of 50 V, and operate to a minimum of 5 V; the UDN2983A and UDN2984A/LW drivers are interchangeable, will withstand an output voltage of 80 V, and operate to a minimum of 35 V. All devices in this series integrate input current limiting resistors and output transient suppression diodes, and are activated by an active high input.

The suffix 'A' (all devices) indicates an 18-lead plastic dual in-line package with copper lead frame for optimum power dissipation. Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of 15 V.

The suffix 'LW' (UDN2982LW and UDN2984LW only) indicates a surface-mountable wide-body SOIC package.

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V
- DIP or SOIC Packaging

Always order by complete part number, e.g., UDN2981A.
Note that all devices are not available in both package types.

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise specified).

Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	UDN2981/82†	V_{IN} = 0.4 V*, V_S = 50 V, T_A = +70°C	1	—	—	200	µA
		UDN2983/84†	V_{IN} = 0.4 V*, V_S = 80 V, T_A = +70°C	1	—	—	200	µA
Output Sustaining	$V_{CE(SUS)}$	UDN2981/82†	I_{OUT} = -45 mA	—	35	—	—	V
Voltage		UDN2983/84†	I_{OUT} = -70 mA	—	45	—	—	V
Collector-Emitter			V_{IN} = 2.4 V, I_{OUT} = -100 mA	2	—	1.6	1.8	V
Saturation Voltage	$V_{CE(SAT)}$	All	V_{IN} = 2.4 V, I_{OUT} = -225 mA	2	—	1.7	1.9	V
			V_{IN} = 2.4 V, I_{OUT} = -350 mA	2	—	1.8	2.0	V
Input Current		UDN2981/83A	V_{IN} = 2.4 V	3	—	140	200	µA
	$I_{IN(ON)}$		V_{IN} = 3.85 V	3	—	310	450	µA
		UDN2982/84†	V_{IN} = 2.4 V	3	—	140	200	µA
			V_{IN} = 12 V	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
(Outputs Open)		UDN2982/84†	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
Supply Current	I_S	UDN2981/82†	V_{IN} = 2.4 V*, V_S = 50 V	4	—	—	10	mA
Leakage Current		UDN2983/84†	V_{IN} = 2.4 V*, V_S = 80 V	4	—	—	10	mA
Clamp Diode	I_R	UDN2981/82†	V_R = 50 V, V_{IN} = 0.4 V*	5	—	—	50	µA
Forward Voltage		UDN2983/84†	V_R = 80 V, V_{IN} = 0.4 V*	5	—	—	50	µA
Clamp Diode	V_F	All	I_F = 350 mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	1.0	2.0	µs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V, See Note	—	—	5.0	10	µs

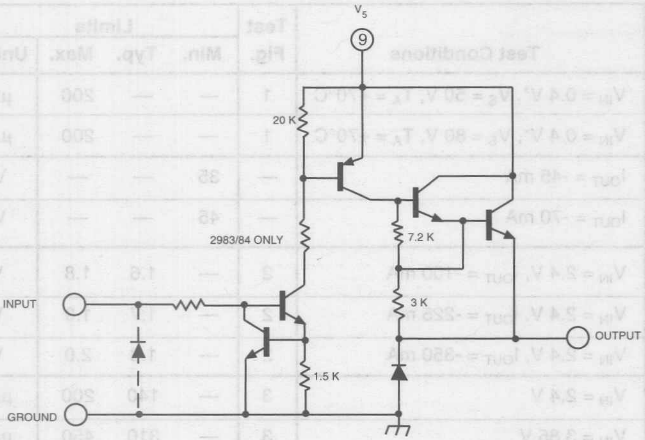
NOTES: Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing consider ations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

Negative current is defined as coming out of (sourcing) the specified device terminal.

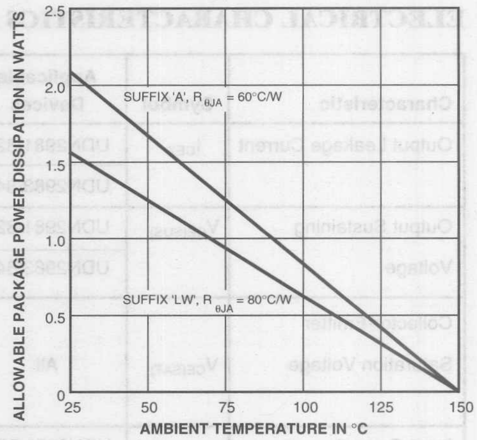
* All inputs simultaneously.

†Complete part number includes suffix to identify package style: A = DIP, LW = SOIC.

One of Eight Drivers



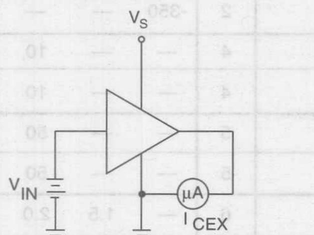
Dwg. No. A-10,242B



Dwg. GP-018B

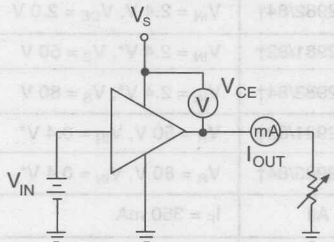
TEST FIGURES

FIGURE 1



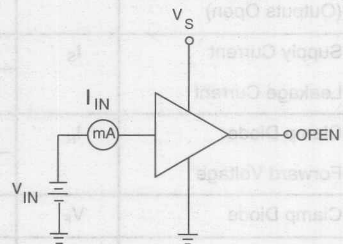
Dwg. No. A-11,083

FIGURE 2



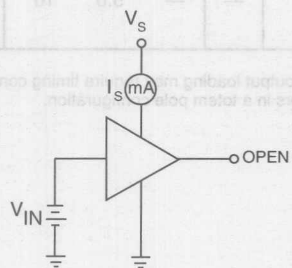
Dwg. No. A-11,084

FIGURE 3



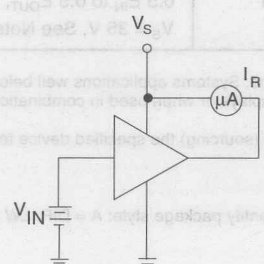
Dwg. No. A-11,085

FIGURE 4



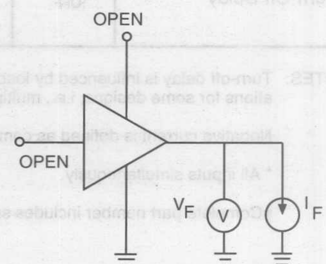
Dwg. No. A-11,086

FIGURE 5



Dwg. No. A-11,087

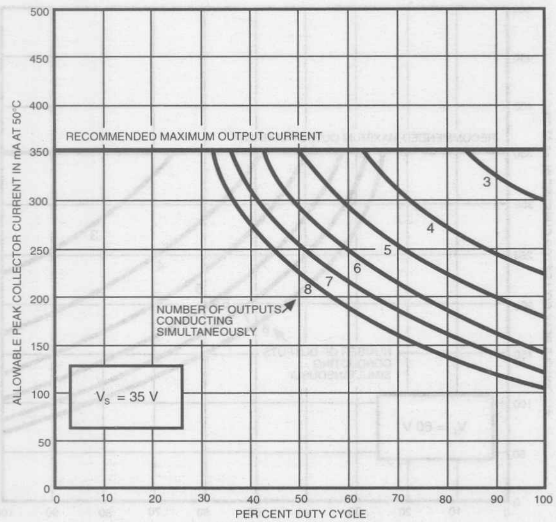
FIGURE 6



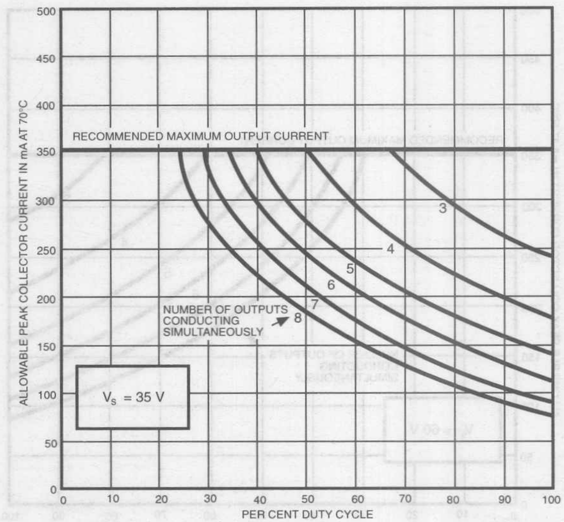
Dwg. No. A-11,088

Allowable peak collector current as a function of duty cycle

Series UDN2980A

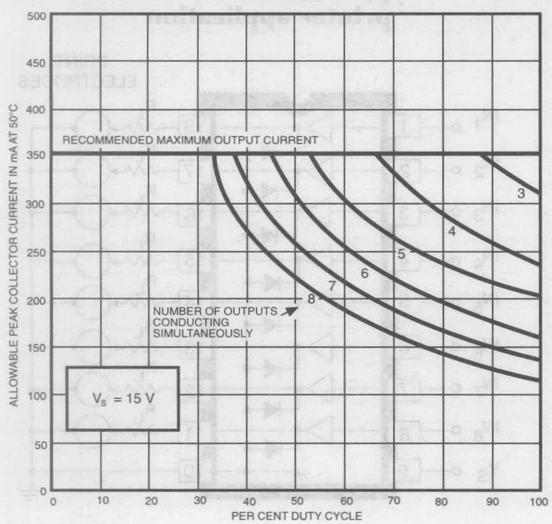


Dwg. No. A-11,106B

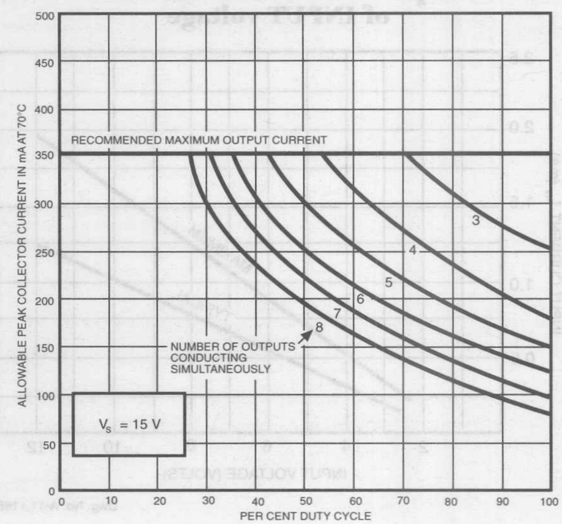


Dwg. No. A-11,111B

SERIES UDN2981/82A



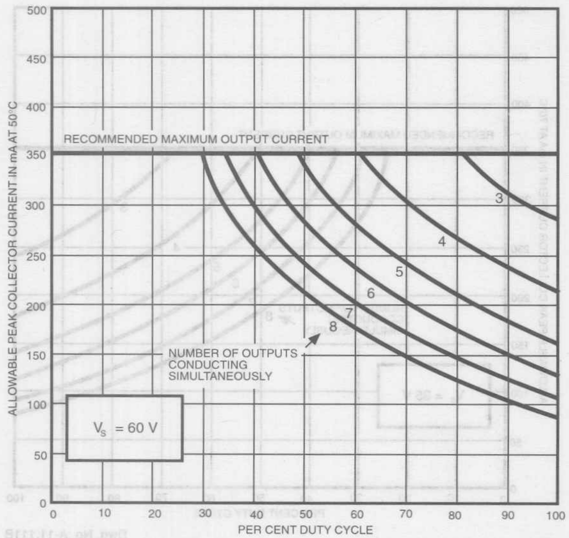
Dwg. No. A-11,107B



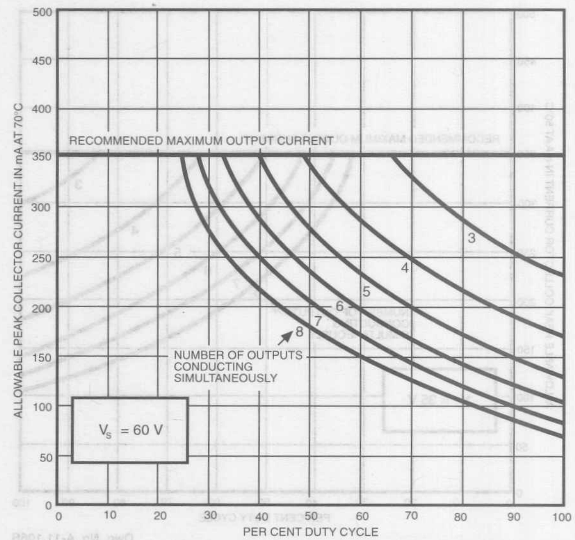
Dwg. No. A-11,108B

Allowable peak collector current as a function of duty cycle

SERIES UDN2983/84A

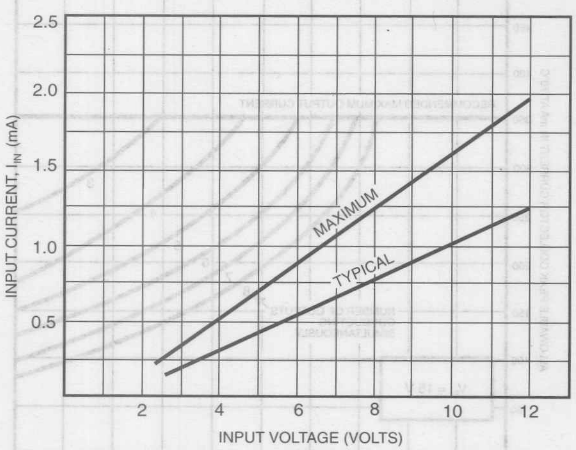


Dwg. No. A-11,109B



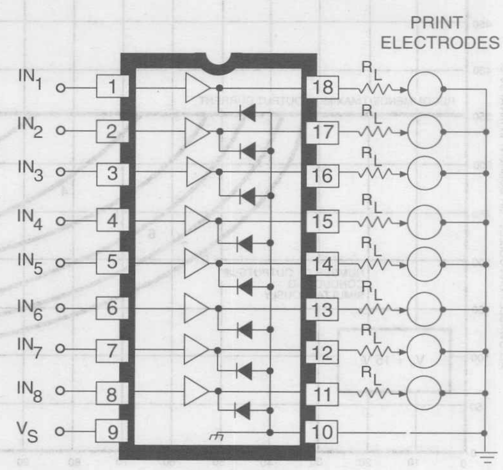
Dwg. No. A-11,110B

Input current as a function of INPUT voltage



Dwg. No. A-11,115B

Typical Electrosensitive printer application

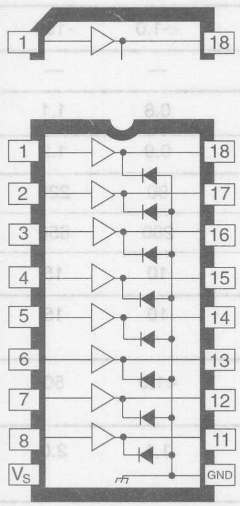


Dwg. No. A-11,113A

2985

29310.2A

8-CHANNEL SOURCE DRIVER



Dwg. No. A-10,243

Recommended for applications requiring separate logic and load grounds, load supply voltages to 30 V, and load currents to 250 mA, the UDN2985A source driver is used as an interface between standard low-power digital logic and LEDs, relays and solenoids. The outputs feature saturated transistors for low collector-emitter saturation voltages.

The UDN2985A driver is for use with 5 V logic systems—TTL, Schottky TTL, DTL, and CMOS. This device has a minimum output breakdown rating of 30 V with a minimum output sustaining voltage of 15 V. The output is switched ON by an active high input level.

Under normal operating conditions, this device can source up to 120 mA for each of the eight outputs at an ambient temperature of 75°C and a supply voltage of 15 V. It incorporates input current-limiting resistors and output transient suppression diodes.

The UDN2985A source driver is supplied in an 18-lead dual in-line package. All inputs are on one side of the package, output pins on the other, to simplify printed wiring board layout.

FEATURES

- TTL, DTL, or CMOS Compatible Inputs
- 250 mA Output Source Current Capability
- Output Transient-Suppression Diodes
- 30 V Minimum Output Breakdown Voltage
- Low Output-Saturation Voltage

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Driver Supply Voltage, V_S .... **30 V**

Continuous Output Current,
I_{OUT} .... **-250 mA**

Input Voltage, V_{IN} .... **20 V**

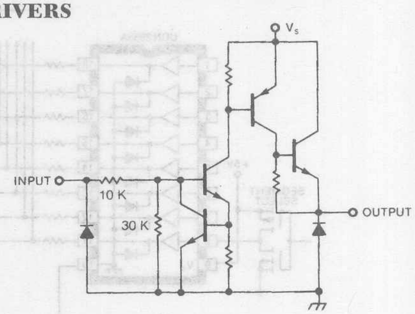
Package Power Dissipation,
P_D .... **2.2 W***

Operating Temperature Range,
T_A .... **-20°C to +85°C**

Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Derate at the rate of 18 mW/°C above T_A = 25°C

PARTIAL SCHEMATIC DIAGRAM
1 OF 8 DRIVERS



Dwg. No. DS-1013

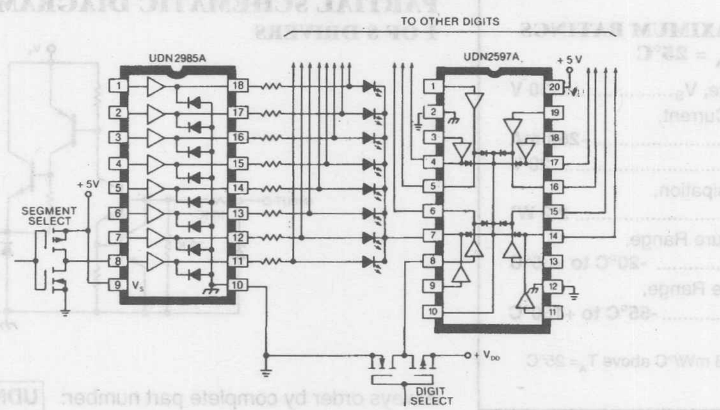
Always order by complete part number: **UDN2985A** .

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 30 V (unless otherwise noted).

Characteristics	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V, V_{OUT} = 0 V	—	<-1.0	-100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -120 mA, L = 3 mH	15	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 2.4, I_{OUT} = -60 mA	—	0.8	1.1	V
		V_{IN} = 2.4, I_{OUT} = -120 mA	—	0.9	1.2	V
Input Current Voltage	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	90	225	µA
		V_{IN} = 5.0 V	—	280	650	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	10	15	µA
Supply Current (outputs open)	I_S	V_S = 30 V, V_{IN} = 2.4 V	—	10	15	mA
Clamp Diode Leakage Current	I_R	V_R = 30 V, T_A = 70°C	—	<1.0	50	µA
Clamp Diode Foward Voltage	V_F	I_F = 120 mA	—	1.1	2.0	V
Turn-On Delay	t_{ON}		—	0.5	1.0	µs
Turn-Off Delay	t_{OFF}		—	5.0	10	µs

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

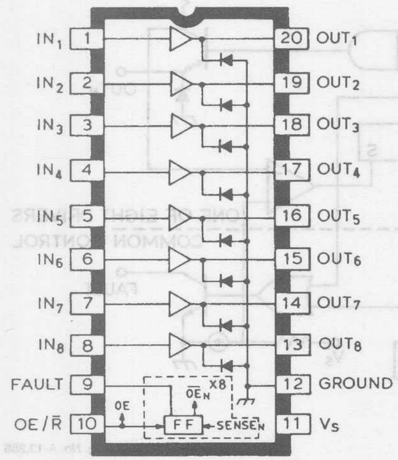
COMMON-CATHODE LED DRIVER



Dwg. No. DS-1014

2987

8-CHANNEL SOURCE DRIVER WITH OVER-CURRENT PROTECTION



Dwg. No. A-13,285

Providing over-current protection for each of its eight sourcing outputs, the UDN2987A driver is used as an interface between standard low-level logic and relays, motors, solenoids, LEDs, and incandescent lamps. The device includes thermal shutdown and output transient protection/clamp diodes for use with sustaining voltages to 35 V.

In this driver, each channel includes a latch to turn OFF that channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common FAULT output is used to indicate either chip thermal shutdown or any over-current condition. All outputs are enabled by pulling the common OE/R input high. When OE/R is low, all outputs are inhibited and the eight latches are reset. The UDN2987A is supplied in a 20-lead dual in-line plastic package.

Under normal operating conditions, each of eight outputs will source in excess of 100 mA continuously at an ambient temperature of 25°C and a supply of 35 V. The over-current fault circuit will protect the device from short-circuits to ground with supply voltages of up to 35 V.

The inputs are compatible with 5 V and 12 V logic systems—TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

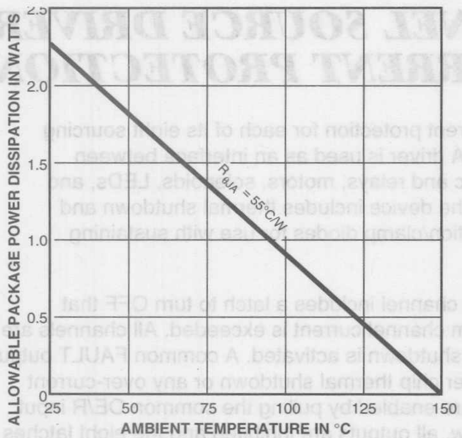
Driver Supply Voltage, V_S	**35 V**
Output Sustaining Voltage, $V_{CE(sus)}$	**35 V**
Continuous Output Current, I_{OUT}	**-500 mA***
FAULT Output Voltage, V_{CE}	**35 V**
FAULT Output Current, I_C	**30 mA**
Input Voltage, V_{IN}	**15 V**
Package Power Dissipation, P_D	**See Graph**
Operating Temperature Range, T_A	**-20°C to +85°C**
Storage Temperature Range, T_S	**-55°C to +150°C**

* Outputs are disabled at approximately -500 mA per driver.

FEATURES

- 350 mA Output Source Current
- Over-Current Protected
- Internal Ground Clamp Diodes
- Output Breakdown Voltage 35 V, Minimum
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Internal Thermal Shutdown
- Automotive Capable

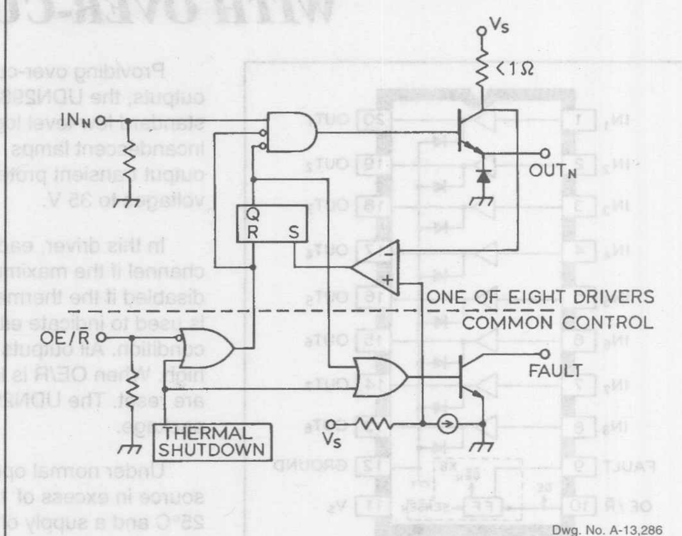
Always order by complete part number: **UDN2987A** .



Dwg. GS-004-1

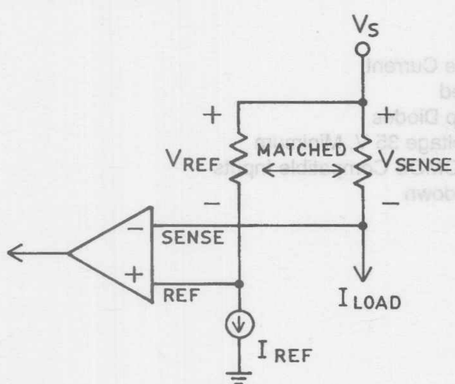
Dwg. No. GS-004-1

FUNCTIONAL BLOCK DIAGRAM



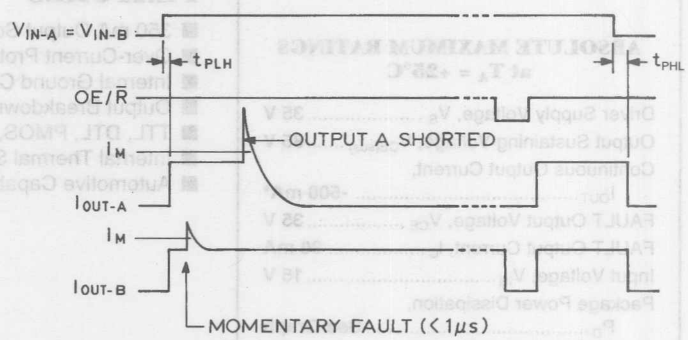
Dwg. No. A-13,286

OVER-CURRENT FAULT SENSE



Dwg. No. A-13,292

OUTPUT CURRENT WAVESHAPES



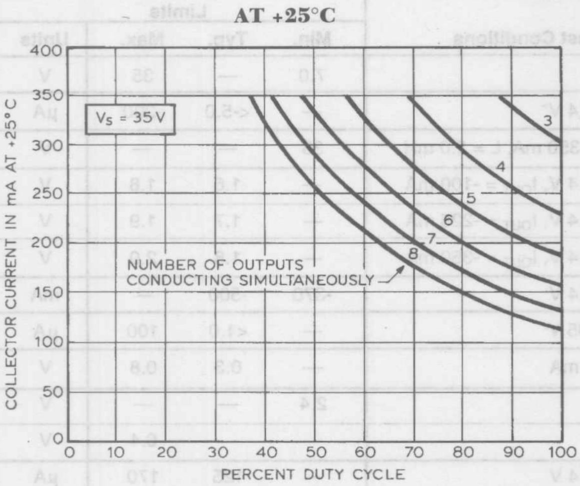
Dwg. No. A-13,293

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{OE} = 2.4 V, V_S = 35 V (unless otherwise noted).

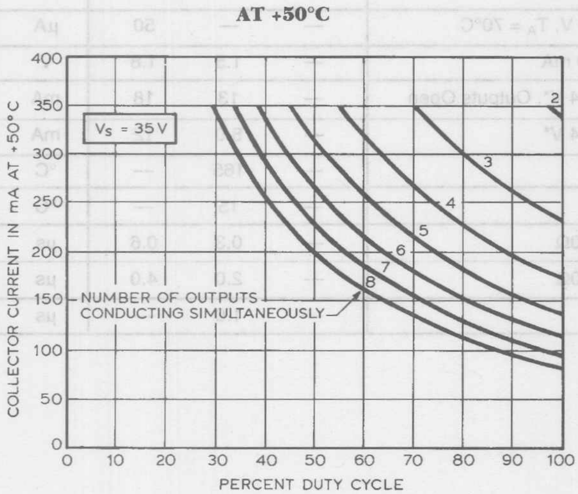
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Functional Supply Range	V_S		7.0	—	35	V
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V*	—	<-5.0	-200	µA
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = -350 mA, L = 2.0 mH	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{IN} = 2.4 V, I_{OUT} = -100 mA	—	1.6	1.8	V
		V_{IN} = 2.4 V, I_{OUT} = -225 mA	—	1.7	1.9	V
		V_{IN} = 2.4 V, I_{OUT} = -350 mA	—	1.8	2.0	V
Channel Shutdown Threshold	I_M	V_{IN} = 2.4 V	-370	-500	—	mA
FAULT Leakage Current	I_{CEX}	V_{CC} = 35 V	—	<1.0	100	µA
FAULT Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 mA	—	0.3	0.8	V
Input Voltage	$V_{IN(ON)}$		2.4	—	—	V
	$V_{IN(OFF)}$		—	—	0.4	V
Input Current	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	125	170	µA
		V_{IN} = 5.0 V	—	840	1020	µA
		V_{IN} = 12 V	—	1500	1800	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	—	15	µA
Clamp Diode Leakage Current	I_R	V_R = 35 V, T_A = 70°C	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	1.8	V
Supply Current	$I_{S(ON)}$	V_{IN} = 2.4 V*, Outputs Open	—	13	18	mA
	$I_{S(OFF)}$	V_{IN} = 0.4 V*	—	8.0	12	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	ΔT_J		—	15	—	°C
Propagation Delay Time	t_{PLH}	R_L = 100Ω	—	0.3	0.6	µs
	t_{PHL}	R_L = 100Ω	—	2.0	4.0	µs
Dead Time	t_d		—	1.0	—	µs

*All inputs simultaneously.

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



Dwg. No. A-13,288



Dwg. No. A-13,289

APPLICATIONS INFORMATION AND CIRCUIT DESCRIPTION

As with all power integrated circuits, the UDN2987A has a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as -370 mA, minimum; therefore, attempted operation at current levels greater than -370 mA may cause a fault indication and channel shutdown. The device is tested at a maximum of -350 mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 35 V.

All outputs are enabled by pulling the OE/R input high. When OE/R is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. Note that the RESET pulse duration (OE/R low) should be at least 1 μs. This will ensure safe operation under attempted RESET conditions with a shorted load. The latches are also reset during power-up, regardless of the state of the OE/R input.

The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is compared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An over-current fault ($V_{SENSE} > V_{REF}$) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a 1 μs delay (t_d) to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the delay and output switching times will allow a brief, permissable current in excess of the trip current before the output driver is turned OFF.

A common thermal shutdown disables all outputs if the chip temperature exceeds +165°C. At thermal shutdown, all latches are reset. The outputs are disabled until the chip cools down to about +150°C (thermal hysteresis).

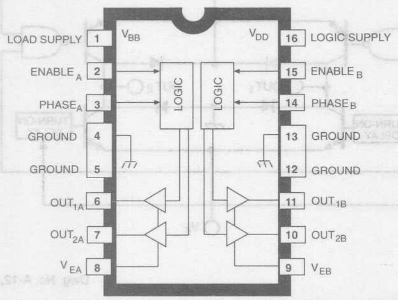
A common open-collector FAULT output is used to indicate any channel over-current condition or chip thermal shutdown.

2993

29319.5A

DUAL H-BRIDGE MOTOR DRIVERS

UDN2993B



Dwg. No. A-12,455

Cost-effective monolithic drive electronics for bipolar stepper and dc (brush) servo motors to 30 V and 500 mA is very practical with the UDN2993B and UDN2993LB. These dual full-bridge motion control ICs integrate separate inputs, level shifting for upper power outputs, control logic, integral inductive transient protection, and source (upper) and sink (lower) drivers in an H-bridge configuration. The single-chip power IC provides improved space utilization and reliability unmatched by discrete component circuitry.

Excepting the power supply connections, the two H-bridges are independent. An ENABLE input is provided for each bridge and permits pulse-width modulation (PWM) through the use of external circuitry. PWM drive techniques provide the benefits of reduced power dissipation, improved motor performance (especially torque), and positively affect system efficiency. Separate PHASE inputs for each bridge determine the direction of current flow in the load. Additionally, each pair of (sink) emitters are terminated to package connections. This allows the use of current-sensing circuitry. Both devices incorporate an intrinsic “dead time” to preclude high crossover (or cross-conduction) currents during changes in direction (phase).

These devices are packaged in plastic DIPs (suffix B) or surface-mountable wide-body SOICs (suffix LB) with copper lead frames for optimum power dissipation without heat sinks. The lead configurations allow automatic insertion, fit standard IC sockets or printed wiring board layouts, and enable easy attachment of a heat sink for maximum power-handling capability. The heat-sink tabs are at ground potential and require no insulation.

Dual full-bridge drivers with peak current ratings of ±3 A are supplied as the UDN2998W.

ABSOLUTE MAXIMUM RATINGS at $T_J \le +150°C$

Load Supply Voltage, V_{BB} .... **30 V**
Logic Supply Voltage, V_{DD} .... **7.0 V**
Logic Input Voltage Range, V_{PHASE} or
V_{ENABLE} .... **-0.3 V to V_{DD} + 0.3 V**
Output Current, I_{OUT} .... **±600 mA**
Sink Driver Emitter Voltage,
V_E .... **1.5 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

IMPORTANT: Load supply voltage must never be applied without logic supply voltage present.

NOTE: Output current rating may be limited by chopping frequency, ambient temperature, airflow, and heat sinking. Under any set of conditions, do not exceed the specified maximum current and a junction temperature of +150°C.

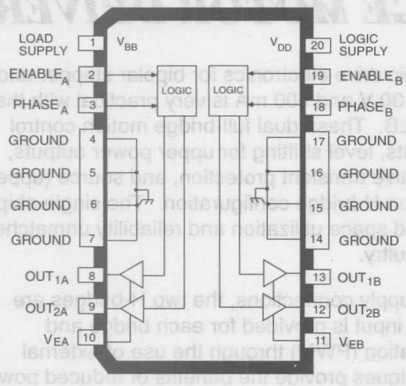
FEATURES

- ±600 mA Output Current
- Output Voltage to 30 V
- Crossover Current Protection
- TTL/NMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Automotive Capable

Always order by complete part number:

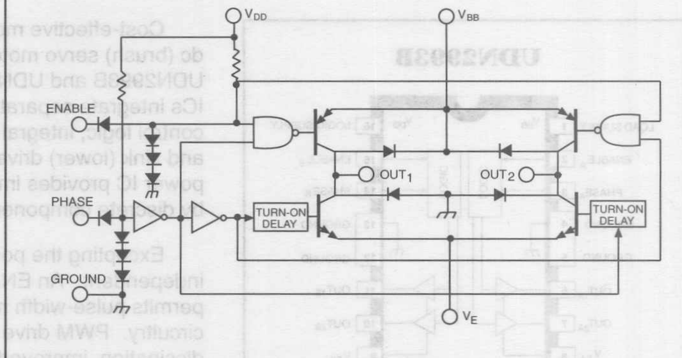
Part Number	Package
UDN2993B	**16-Pin DIP**
UDN2993LB	**20-Lead Wide-Body SOIC**

UDN2993LB



Dwg. No. A-14,340

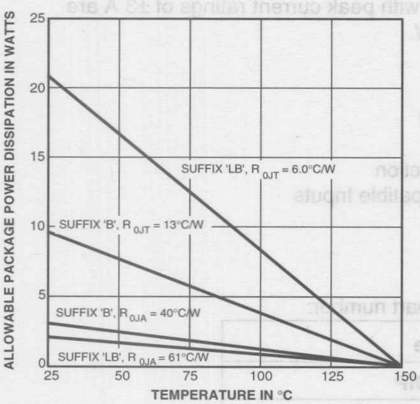
FUNCTIONAL BLOCK DIAGRAM
(One of Two Drivers)



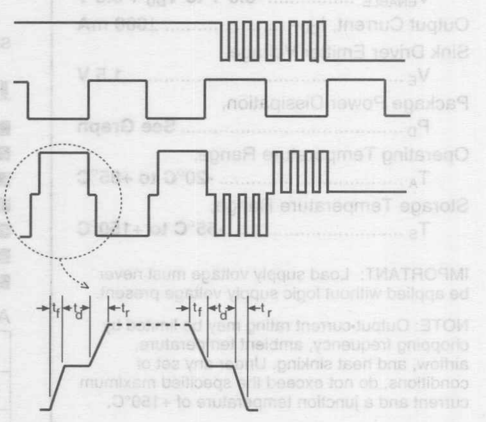
Dwg. No. A-12,447

TRUTH TABLE

Enable Input	Phase Input	Output 1	Output 2
High	High	Low	High
High	Low	High	Low
Low	High	Low	Open
Low	Low	Open	Low



Dwg. GP-021A



Dwg. No. A-12,448

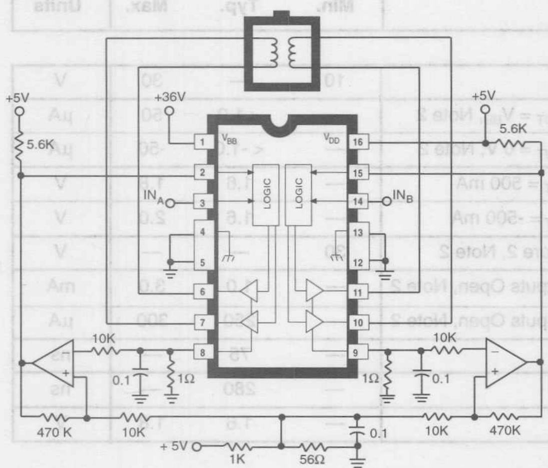
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{DD} = 5 V, V_E = 0 V, $T_J \leq$ +150°C Figure 1 (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	30	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 0.8 V, V_{OUT} = V_{BB}, Note 2	—	< 1.0	50	µA
		V_{ENABLE} = 0.8 V, V_{OUT} = 0 V, Note 2	—	< -1.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 2.4 V, I_{OUT} = 500 mA	—	1.6	1.8	V
		V_{ENABLE} = 2.4 V, I_{OUT} = -500 mA	—	1.6	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±500 mA, Figure 2, Note 2	30	—	—	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 2.4 V, Outputs Open, Note 2	—	1.0	3.0	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 0.8 V, Outputs Open, Note 2	—	250	300	µA
Source Driver Rise Time	t_r	I_{OUT} = -500 mA,	—	75	—	ns
Source Driver Fall Time	t_f	I_{OUT} = -500 mA,	—	280	—	ns
Clamp Diode Forward Voltage	V_F	I_F = 500 mA	—	1.6	1.8	V
Control Logic (PHASE or ENABLE)						
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.4 V	—	< 1.0	10	µA
	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	-200	-300	µA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	14	20	mA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	250	—	ns
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	500	—	ns

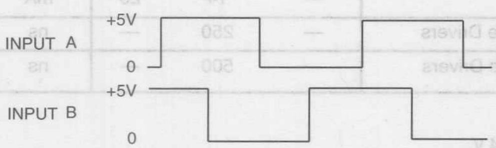
NOTES: 1. Each driver is tested separately.
2. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.4 V.
3. Negative current is defined as coming out of (sourcing) the specified device pin.

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)



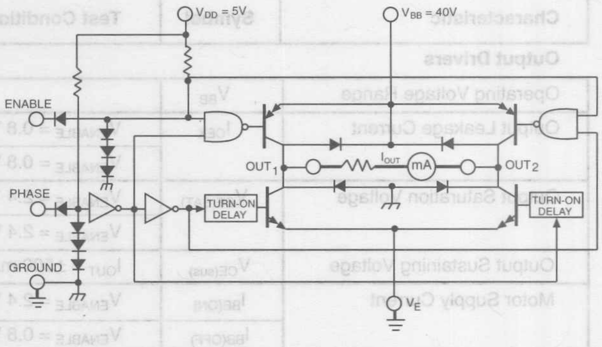
Dwg. No. A-12,453



Dwg. No. A-12,454

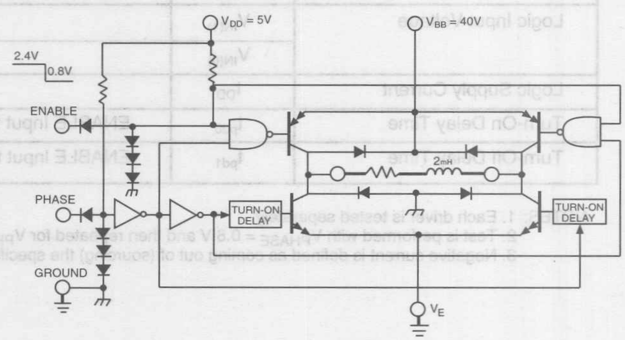
TEST FIGURES

FIGURE 1



Dwg. No. A-12,449

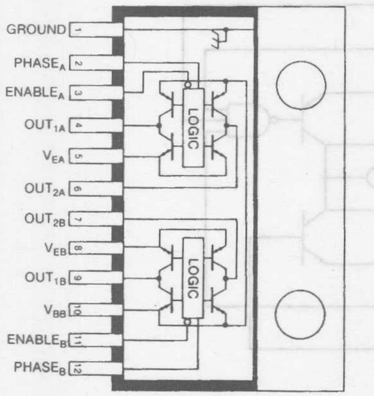
FIGURE 2



Dwg. No. A-12,450

29319.6B

DUAL FULL-BRIDGE MOTOR DRIVER



Dwg. No. W-106

As an interface between low-level logic and solenoids, brushless dc motors, or stepper motors, the UDN2998W dual full-bridge driver will operate inductive loads up to 50 V with continuous output currents of up to 2 A per bridge or peak (start-up) currents to 3 A. The control inputs are compatible with TTL, DTL, and 5 V CMOS logic. Except for a common supply voltage and thermal shutdown, the two drivers in each package are completely independent.

For external PWM control, an Output Enable for each bridge circuit is provided and the sink driver emitters are pinned out for connection to external current-sensing resistors. The chopper drive mode is characterized by low power dissipation levels and maximum efficiency. A PHASE input to each bridge determines load-current direction.

Extensive circuit protection is provided on-chip. Both ground-clamp and flyback diodes for each bridge are provided. A thermal shutdown circuit disables the load drive if chip temperature rating (package power dissipation) is exceeded. Internally-generated delays provide crossover-current protection.

The UDN2998W is packaged in a 12-pin single in-line power tab package for high power capabilities. Driving either of the bridges at the full 2 A dc rating requires the use of an external heat-sink. The tab is at ground potential and needs no insulation.

A similar dual full-bridge driver for use with continuous load currents to ±500 mA is the UDN2993B.

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{BB} .... **50 V**
Output Current, I_{OUT} (DC) .... **±2 A**
(Peak) .... **±3 A**
Sink Driver Emitter Voltage, V_E .... **1.5 V**
Logic Input Voltage Range,
V_{PHASE} or V_{ENABLE} .... **-0.3 V to 15 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

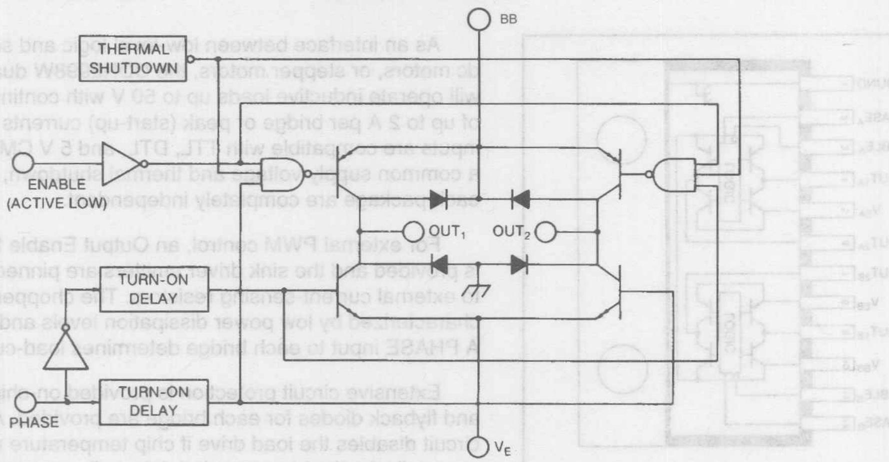
NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, or heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

FEATURES

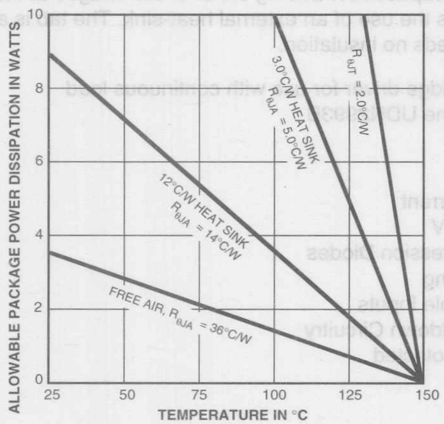
- ±3 A Peak Output Current
- Output Voltage to 50 V
- Integral Output Suppression Diodes
- Output Current Sensing
- TTL/CMOS Compatible Inputs
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected
- Automotive Capable

Always order by complete part number: UDN2998W

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. W-107A



Dwg. GP-012A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

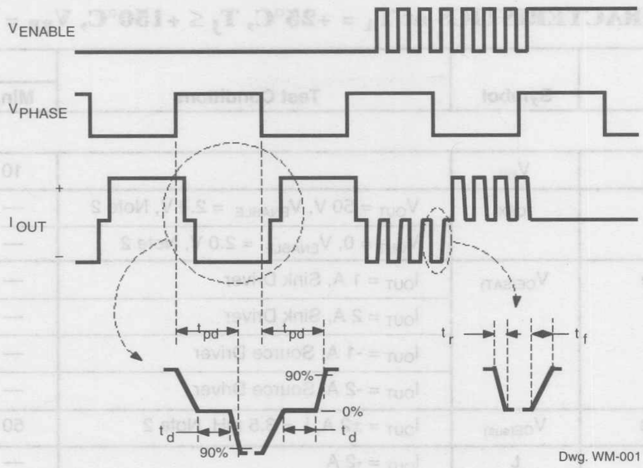
TRUTH TABLE

ENABLE INPUT	PHASE INPUT	OUTPUT 1	OUTPUT 2
Low	High	High	Low
Low	Low	Low	High
High	High	Open	Low
High	Low	Low	Open

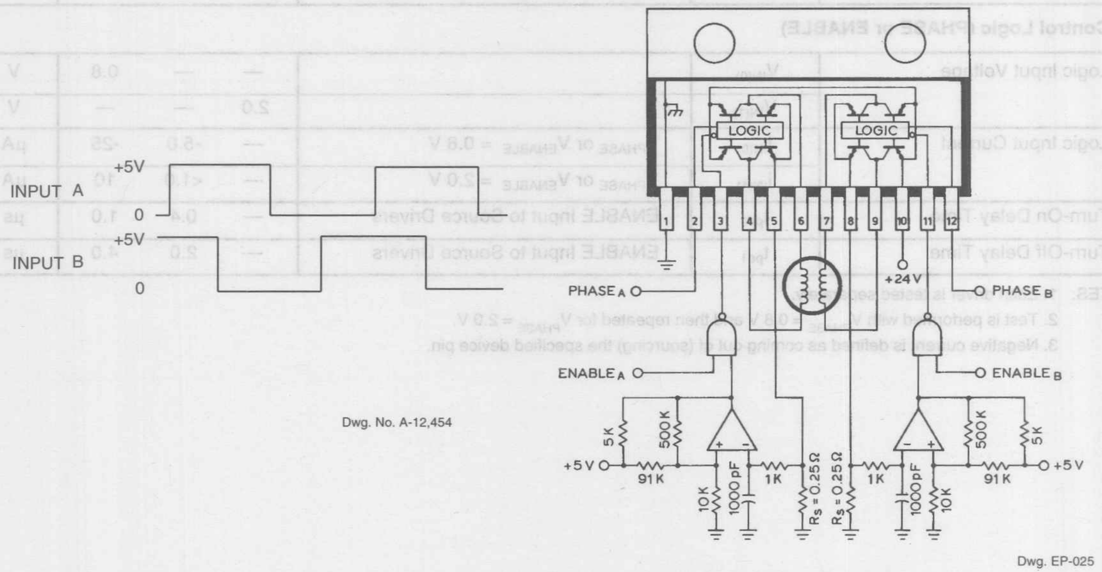
ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ +150°C, V_{BB} = 50 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	50	V
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V, V_{ENABLE} = 2.0 V, Note 2	—	<5.0	50	µA
		V_{OUT} = 0, V_{ENABLE} = 2.0 V, Note 2	—	<-5.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 1 A, Sink Driver	—	1.2	1.4	V
		I_{OUT} = 2 A, Sink Driver	—	1.7	1.9	V
		I_{OUT} = -1 A, Source Driver	—	1.7	1.9	V
		I_{OUT} = -2 A, Source Driver	—	2.0	2.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 3.5 mH, Note 2	50	—	—	V
Source Driver Rise Time	t_r	I_{OUT} = -2 A	—	500	—	ns
Source Driver Fall Time	t_f	I_{OUT} = -2 A	—	750	—	ns
Deadtime	t_d	I_{OUT} = ±2 A	—	2.5	—	µs
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	<5.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.5	2.0	V
Supply Current	I_{BB}	$V_{ENABLE(1)} = V_{ENABLE(2)}$ = 0.8 V	—	30	35	mA
Control Logic (PHASE or ENABLE)						
Logic Input Voltage	$V_{IN(0)}$		—	—	0.8	V
	$V_{IN(1)}$		2.0	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8 V	—	-5.0	-25	µA
	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.0 V	—	<1.0	10	µA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	0.4	1.0	µs
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	2.0	4.0	µs

NOTES: 1. Each driver is tested separately.
2. Test is performed with V_{PHASE} = 0.8 V and then repeated for V_{PHASE} = 2.0 V.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



TYPICAL APPLICATION
2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)

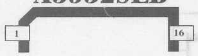


3952

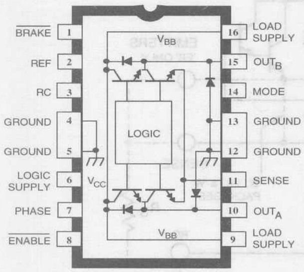
29319.1

FULL-BRIDGE PWM MOTOR DRIVER

A3952SLB



A3952SB



Dwg. PP-056

Note that the A3952SB (DIP) and the A3952SLB (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} .... **50 V**
Output Current, I_{OUT}
($t_w \le 20$ µs) .... **±3.5 A**
(Continuous) .... **±2.0 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to V_{CC} + 0.3 V**
Sense Voltage, V_{SENSE} .... **1.5 V**
Reference Voltage, V_{REF} .... **15 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **–20°C to +85°C**
Junction Temperature, T_J .... **+150°C***
Storage Temperature Range,
T_S .... **–55°C to + 150°C**

Output current rating may be limited by duty cycle, ambient temperature, heat sinking and/or forced cooling. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed for bidirectional pulse-width modulated current control of inductive loads, the A3952S– is capable of continuous output currents to ±2 A and operating voltages to 50 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed OFF-time pulse duration is set by a user-selected external RC timing network. Internal circuit protection includes thermal shutdown with hysteresis, transient suppression diodes, and cross-over-current protection. Special power-up sequencing is not required.

With the ENABLE input held low, the PHASE input controls load current polarity by selecting the appropriate source and sink driver pair. The MODE input determines whether the PWM current-control circuitry operates in a slow current-decay mode (only the selected sink driver switching) or in a fast current-decay mode (selected source and sink switching). A user-selectable blanking window prevents false triggering of the PWM current control circuitry. With the ENABLE input held high, all output drivers are disabled. A sleep mode is provided to reduce power consumption when inactive.

When a logic low is applied to the BRAKE input, the braking function is enabled. This overrides ENABLE and PHASE to turn OFF both source drivers and turn ON both sink drivers. The brake function can be safely used to dynamically brake brush dc motors. The A3952S– is supplied in a choice of four power packages. In all package styles, the batwing/power tab is at ground potential and needs no isolation.

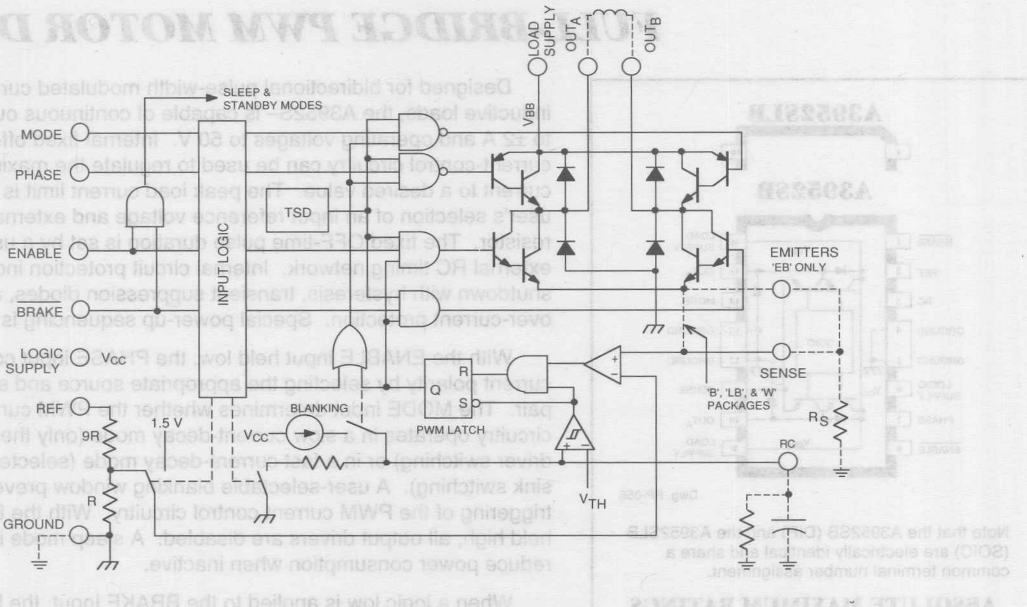
FEATURES

- ±2 A Continuous Output Current Rating
- 50 V Output Voltage Rating
- Internal PWM Current Control
- Fast and Slow Current-Decay Modes
- Under-Voltage Lockout
- Sleep (Low Current Consumption) Mode
- Internal Transient Suppression Diodes
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protection
- Automotive Capable

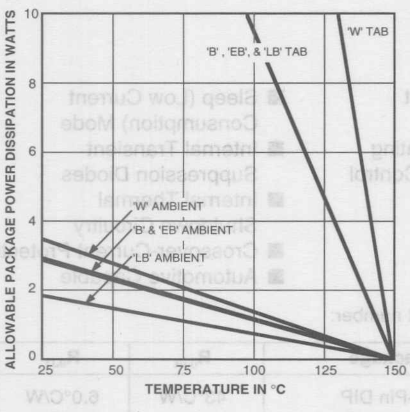
Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JT}$
A3952SB	16-Pin DIP	43°C/W	6.0°C/W
A3952SEB	28-Lead PLCC	42°C/W	6.0°C/W
A3952SLB	16-Lead SOIC	67°C/W	6.0°C/W
A3952SW	12-Pin Power-Tab SIP	36°C/W	2.0°C/W

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-036



Dwg. GP-007-1

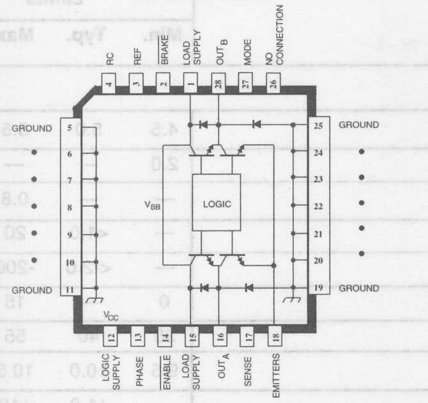
TRUTH TABLE

BRAKE	ENABLE	PHASE	MODE	OUT_A	OUT_B	DESCRIPTION
H	H	X	H	Z	Z	Sleep Mode
H	H	X	L	Z	Z	Standby, Note 1
H	L	H	H	H	L	Forward, Fast-Decay Mode
H	L	H	L	H	L	Forward, Slow-Decay Mode
H	L	L	H	L	H	Reverse, Fast-Decay Mode
H	L	L	L	L	H	Reverse, Slow-Decay Mode
L	X	X	H	L	L	Brake, Fast-Decay Mode
L	X	X	L	L	L	Brake, No Current Control, Note 2

X = Irrelevant Z = High Impedance (source and sink both OFF)

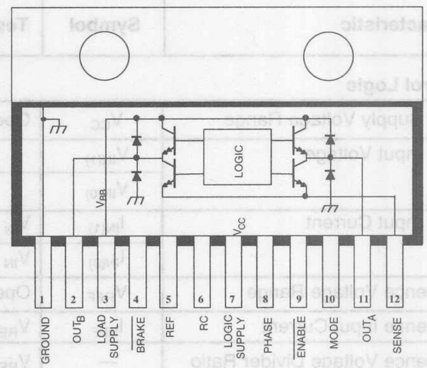
NOTES: 1. Includes active pull-offs for power outputs.
2. Includes internal default V_{sense} level for over-current protection.

A3952SEB



Dwg. PP-057

A3952SW



Dwg. PP-068

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{CC} = 5.0 V, V_{BRAKE} = 2.0 V, V_{SENSE} = 0 V, RC = 20 kΩ/1000 pF to Ground (unless noted otherwise).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±2.0 A, L = 3 mH	V_{CC}	–	50	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	–	<1.0	50	µA
		V_{OUT} = 0 V	–	<-1.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -0.5 A	–	0.9	1.2	V
		Source Driver, I_{OUT} = -1.0 A	–	1.0	1.4	V
		Source Driver, I_{OUT} = -2.0 A	–	1.2	1.8	V
		Sink Driver, I_{OUT} = +0.5 A	–	0.9	1.2	V
		Sink Driver, I_{OUT} = +1.0 A	–	1.0	1.4	V
		Sink Driver, I_{OUT} = +2.0 A	–	1.3	1.8	V
Clamp Diode Forward Voltage	V_F	I_F = 0.5 A	–	1.0	1.4	V
(Source or Sink)		I_F = 1.0 A	–	1.1	1.6	V
		I_F = 2.0 A	–	1.4	2.0	V
Load Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V	–	2.9	6.0	mA
(No Load)	$I_{BB(OFF)}$	V_{ENABLE} = 2.0 V, V_{MODE} = 0.8 V	–	3.1	6.5	mA
		V_{BRAKE} = 0.8 V	–	3.1	6.5	mA
	$I_{BB(Sleep)}$	$V_{ENABLE} = V_{MODE}$ = 2.0 V	–	<1.0	50	µA

Continued next page …

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic						
Logic Supply Voltage Range	V_{CC}	Operating	4.5	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	0	—	15	V
Reference Input Current	I_{REF}	V_{REF} = 2.0 V	25	40	55	µA
Reference Voltage Divider Ratio	—	V_{REF} = 15 V	9.5	10.0	10.5	—
Comparator Input Offset Voltage	V_{IO}	V_{REF} = 0 V	—	±1.0	±10	mV
PWM RC Fixed OFF Time	t_{off}	C_T = 1000 pF, R_T = 20 kΩ	18	20	22	µs
PWM Minimum ON Time	$t_{on(min)}$	C_T = 820 pF, $R_T \geq$ 12 kΩ	—	1.7	3.0	µs
		C_T = 1200 pF, $R_T \geq$ 12 kΩ	—	2.5	3.8	µs
Propagation Delay Time	t_{pd}	I_{OUT} = ±2.0 A, 50% E_{IN} to 90% E_{OUT} Transition:				
		ENABLE ON to Source ON	—	2.9	—	µs
		ENABLE OFF to Source OFF	—	0.7	—	µs
		ENABLE ON to Sink ON	—	2.4	—	µs
		ENABLE OFF to Sink OFF	—	0.7	—	µs
		PHASE Change to Source ON	—	2.9	—	µs
		PHASE Change to Source OFF	—	0.7	—	µs
		PHASE Change to Sink ON	—	2.4	—	µs
		PHASE Change to Sink OFF	—	0.7	—	µs
	$t_{pd(pwm)}$	Comparator Trip to Sink OFF	—	0.8	1.5	µs
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Disable Threshold	$V_{CC(UVLO)}$		3.15	3.50	3.85	V
UVLO Hysteresis	$\Delta V_{CC(UVLO)}$		300	400	500	mV
Logic Supply Current	$I_{CC(ON)}$	V_{ENABLE} = 0.8 V, V_{BRAKE} = 2.0 V	—	20	30	mA
(No Load)	$I_{CC(OFF)}$	V_{ENABLE} = 2.0 V, V_{MODE} = 0.8 V	—	12	18	mA
	$I_{CC(BRAKE)}$	V_{BRAKE} = 0.8 V	—	26	40	mA
	$I_{CC(Sleep)}$	V_{ENABLE} = V_{MODE} = V_{BRAKE} = 2.0 V	—	3.0	5.0	mA

NOTES: 1. Typical Data is for design information only.
2. Each driver is tested separately.
3. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Internal PWM Current Control During Forward And Reverse Operation

The A3952S– contains a fixed OFF-time pulse-width modulated (PWM) current-control circuit that can be used to limit the load current to a desired value. The value of the current limiting (I_{TRIP}) is set by the selection of an external current sensing resistor (R_S) and reference input voltage (V_{REF}). The internal circuitry compares the voltage across the external sense resistor to one tenth the voltage on the REF input terminal, resulting in a function approximated by

$$I_{TRIP} = V_{REF}/(10 \bullet R_S).$$

In forward or reverse mode the current-control circuitry limits the load current. When the load current reaches I_{TRIP}, the comparator resets a latch to turn OFF the selected sink driver (in the slow-decay mode) or selected sink and source driver pair (in the fast-decay mode). In slow-decay mode, the selected sink driver is disabled; the load inductance causes the current to recirculate through the source driver and flyback diode (see figure 1). In fast-decay mode, the selected sink and source driver pair are disabled; the load inductance causes the current to flow from ground to the load supply via the ground clamp and flyback diodes.

FIGURE 1 — Load-Current Paths

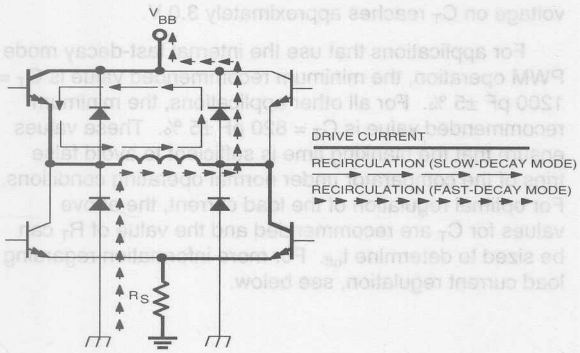
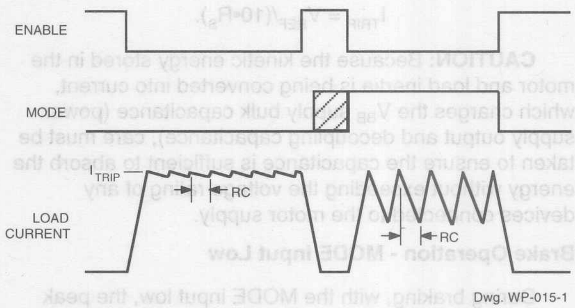


FIGURE 2 — Fast and Slow Current-Decay Waveforms



The user selects an external resistor (R_T) and capacitor (C_T) to determine the time period ($t_{off} = R_T \bullet C_T$) during which the drivers remain disabled (see "RC Fixed OFF Time" below). At the end of the R_TC_T interval, the drivers are re-enabled allowing the load current to increase again. The PWM cycle repeats, maintaining the load current at the desired value (see figure 2).

Internal PWM Current Control During Brake MODE Operation

The brake circuit turns OFF both source drivers and turns ON both sink drivers. For dc motor applications, this has the effect of shorting the motor's back-EMF voltage, resulting in current flow that brakes the motor dynamically. However, if the back-EMF voltage is large, and there is no PWM current limiting, then the load current can increase to a value that approaches a locked rotor condition. To limit the current, when the I_{TRIP} level is reached, the PWM circuit disables the conducting sink driver. The energy stored in the motor's inductance is then discharged into the load supply causing the motor current to decay.

As in the case of forward/reverse operation, the drivers are re-enabled after a time given by $t_{off} = R_T \bullet C_T$ (see "RC Fixed OFF Time" below). Depending on the back-EMF voltage (proportional to the motor's decreasing speed), the load current again may increase to I_{TRIP}. If so, the PWM cycle will repeat, limiting the load current to the desired value.

Brake Operation - MODE Input High

During braking, when the MODE input is high, the current limit can be approximated by

$$I_{TRIP} = V_{REF}/(10 \bullet R_S).$$

CAUTION: Because the kinetic energy stored in the motor and load inertia is being converted into current, which charges the V_{BB} supply bulk capacitance (power supply output and decoupling capacitance), care must be taken to ensure the capacitance is sufficient to absorb the energy without exceeding the voltage rating of any devices connected to the motor supply.

Brake Operation - MODE Input Low

During braking, with the MODE input low, the peak current limit defaults internally to a value approximated by

$$I_{TRIP} = 1.5\ V/R_S.$$

In this mode, the value of R_S determines the I_{TRIP} value independent of V_{REF}. This is useful in applications with differing run and brake currents and no practical method of varying V_{REF}.

Choosing a small value for R_S essentially disables the current limiting during braking. Therefore, care should be taken to ensure that the motor's current does not exceed the absolute maximum ratings of the device. The braking current can be measured by using an oscilloscope with a current probe connected to one of the motor's leads.

RC Fixed OFF Time

The internal PWM current control circuitry uses a one shot to control the time the driver(s) remain(s) OFF. The one shot time, t_{off} (fixed OFF time), is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected in parallel from the RC terminal to ground. The fixed OFF time, over a range of values of C_T = 820 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ, is approximated by

$$t_{off} = R_T \bullet C_T.$$

When the PWM latch is reset by the current comparator, the voltage on the RC terminal will begin to decay from approximately 3 volts. When the voltage on the RC terminal reaches approximately 1.1 volt, the PWM latch is set, thereby re-enabling the driver(s).

RC Blanking

In addition to determining the fixed OFF-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the comparator when the outputs are switched by the internal current control circuitry (or by the PHASE, BRAKE, or ENABLE inputs). The comparator output is blanked to prevent false over-current detections due to reverse recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{off} time, the comparator's output is blanked and C_T begins to be charged from approximately 1.1 V by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

Similarly, when a transition of the PHASE input occurs, C_T is discharged to near ground during the crossover delay time (the crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

Similarly, when the device is disabled via the ENABLE input, C_T is discharged to near ground. When the device is re-enabled, C_T is charged by the internal current source. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 V.

For applications that use the internal fast-decay mode PWM operation, the minimum recommended value is C_T = 1200 pF ±5 %. For all other applications, the minimum recommended value is C_T = 820 pF ±5 %. These values ensure that the blanking time is sufficient to avoid false trips of the comparator under normal operating conditions. For optimal regulation of the load current, the above values for C_T are recommended and the value of R_T can be sized to determine t_{off}. For more information regarding load current regulation, see below.

Load Current Regulation With The Internal PWM Current-Control Circuitry

When the device is operating in slow-decay mode, there is a limit to the lowest level that the PWM current-control circuitry can regulate load current. The limitation is the minimum duty cycle, which is a function of the user-selected value of t_{off} and the maxuimum value of the minimum ON-time pulse, $t_{on(min)}$, that occurs each time the PWM latch is reset. If the motor is not rotating, as in the case of a stepper motor in hold/detent mode, or a brush dc motor when stalled or at startup, the worst-case value of current regulation can be approximated by

$$I_{(AV)} \approx \frac{[(V_{BB} - V_{SAT(source+sink)}) \bullet t_{on(min)}max] - [1.05 (V_{SAT(sink)} + V_D) \bullet t_{off}]}{1.05 (t_{on(min)}max + t_{off}) \bullet R_{LOAD}}$$

where $t_{off} = R_T \bullet C_T$, R_{LOAD} is the series resistance of the load, V_{BB} is the load/motor supply voltage, and $t_{on(min)}max$ is specified in the electrical characteristics table. When the motor is rotating, the back EMF generated will influence the above relationship. For brush dc motor applications, the current regulation is improved. For stepper motor applications when the motor is rotating, the effect is more complex. A discussion of this subject is included in the section on stepper motors under "Applications".

The following procedure can be used to evaluate the worst-case slow-decay internal PWM load current regulation in the system:

Set V_{REF} to 0 volts. With the load connected and the PWM current control operating in slow-decay mode, use an oscilloscope to measure the time the output is low (sink ON) for the output that is chopping. This is the typical minimum ON time ($t_{on(min)}typ$) for the device. C_T then should be increased until the measured value of $t_{on(min)}$ is equal to $t_{on(min)}max) = 3.0$ µs as specified in the electrical characteristics table. When the new value of C_T has been set, the value of R_T should be decreased so the value for $t_{off} = R_T \bullet C_T$ (with the artificially increased value of C_T) is equal to 105% of the nominal design value. The worst-case load current regulation then can be measured in the system under operating conditions.

In applications utilizing both fast- and slow-decay internal PWM modes, the performance of the slow-decay current regulation should be evaluated per the above procedure and a $t_{on(min)}max$ of 3.8 µs. This corresponds to a C_T value of 1200 pF, which is required to ensure sufficient blanking during fast-decay internal PWM.

Load Current Regulation With External PWM of the Phase And Enable Inputs

The PHASE and ENABLE inputs can be pulse-width modulated to regulate load current. Typical propagation delays from the PHASE and ENABLE inputs to transitions of the power outputs are specified in the electrical characteristics table. If the internal PWM current control is used, then the comparator blanking function is active during phase and enable transitions. This eliminates false tripping of the over-current comparator caused by switching transients (see "RC Blanking" above).

Enable Pulse-Width Modulation

With the MODE input low, toggling the ENABLE input turns ON and OFF the selected source and sink drivers. The corresponding pair of flyback and ground clamp diodes conduct after the drivers are disabled, resulting in fast current decay. When the device is enabled, the internal current control circuitry will be active and can be used to limit the load current in a slow-decay mode.

For applications that PWM the ENABLE input, and desire that the internal current limiting circuit function in the fast-decay mode, the ENABLE input signal should be inverted and connected to the MODE input. This prevents the device from being switched into sleep mode when the ENABLE input is low.

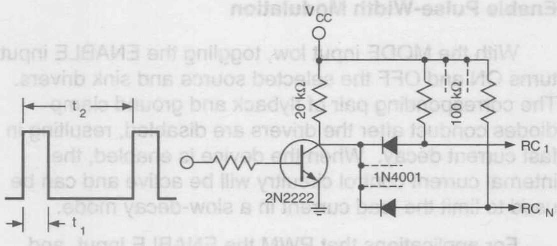
Phase Pulse-Width Modulation

Toggling the PHASE terminal determines/controls which sink/source pair is enabled, producing a load current that varies with the duty cycle and remains continuous at all times. This can have added benefits in bidirectional brush dc servo motor applications as the transfer function between the duty cycle on the phase input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low current levels). See also, "DC Motor Applications" below.

Synchronous Fixed-Frequency PWM

The internal PWM current-control circuitry of multiple A3952S– devices can be synchronized by using the simple circuit shown in figure 3. A 555 IC can be used to generate the reset pulse/blanking signal (t_1) and the period of the PWM cycle (t_2). The value of t_1 should be a minimum of 1.5 μs in slow-decay mode and 2 μs in fast-decay mode. When used in this configuration, the R_T and C_T components should be omitted. The PHASE and ENABLE inputs should not be PWMed with this circuit configuration due to the absence of a blanking function synchronous with their transitions.

FIGURE 3 — Synchronous Fixed-Frequency Control Circuit



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MISCELLANEOUS INFORMATION

A logic high applied to both the ENABLE and MODE terminals puts the device into a sleep mode to minimize current consumption when not in use.

An internally generated dead time prevents cross-over currents that can occur when switching phase or braking.

Thermal protection circuitry turns OFF all drivers should the junction temperature reach 165°C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The hysteresis of the thermal shutdown circuit is approximately 15°C.

If the internal current-control circuitry is not used; the V_{REF} terminal should be connected to V_{CC}, the SENSE terminal should be connected to ground, and the RC terminal should be left floating (no connection).

An internal under-voltage lockout circuit prevents simultaneous conduction of the outputs when the device is powered up or powered down.

APPLICATION NOTES

Current Sensing

The actual peak load current (I_{OUTP}) will be greater than the calculated value of I_{TRIP} due to delays in the turn OFF of the drivers. The amount of overshoot can be approximated as

$$I_{OUTP} \approx \frac{(V_{BB} - [(I_{TRIP} \bullet R_{LOAD}) + V_{BEMF}]) \bullet t_{pd(pwm)}}{L_{LOAD}}$$

where V_{BB} is the load/motor supply voltage, V_{BEMF} is the back-EMF voltage of the load, R_{LOAD} and L_{LOAD} are the resistance and inductance of the load respectively, and $t_{pd(pwm)}$ is the propagation delay as specified in the electrical characteristics table.

The reference terminal has an equivalent input resistance of 50 kΩ ±30%. This should be taken into account when determining the impedance of the external circuit that sets the reference voltage value.

To minimize current-sensing inaccuracies caused by ground trace I•R drops, the current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the I•R drops in the PCB can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_S.

Larger values of R_S reduce the aforementioned effects but can result in excessive heating and power loss in the sense resistor. The selected value of R_S must not cause the SENSE terminal absolute maximum voltage rating to be exceeded. The recommended value of R_S is in the range of

$$R_S = (0.375 \text{ to } 1.125)/I_{TRIP}.$$

The current-sensing comparator functions down to ground allowing the device to be used in microstepping, sinusoidal, and other varying current profile applications.

Thermal Considerations

For reliable operation, it is recommended that the maximum junction temperature be kept as low as possible, typically 90°C to 125°C. The junction temperature can be measured by attaching a thermocouple to the power tab/batwing of the device and measuring the tab temperature, T_T. The junction temperature can then be approximated by using the formula

$$T_J \approx T_T + (2 \bullet V_F \bullet I_{OUT} \bullet R_{\theta JT})$$

where V_F is the clamp diode forward voltage and can be determined from the electrical specification table for the given level of I_{OUT}. The value for R_{qJT} is given in the package thermal resistance table for the appropriate package.

The power dissipation of the batwing packages can be improved by 20 to 30% by adding a section of printed circuit board copper (typically 6 to 18 square centimeters) connected to the batwing terminals of the device.

The thermal performance in applications with high load currents and/or high duty cycles can be improved by adding external diodes in parallel with the internal diodes. In internal PWM slow-decay applications, only the two top-side (flyback) diodes need be added. For internal fast-decay PWM, or external PHASE or ENABLE input PWM applications, all four external diodes should be added for maximum junction temperature reduction.

PCB Layout

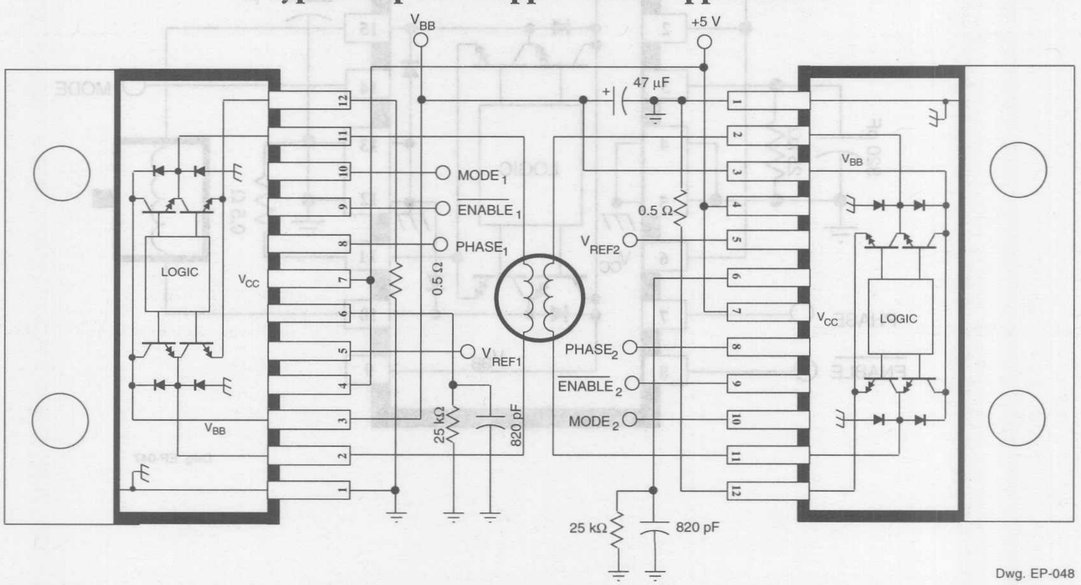
The load supply terminal, V_{BB}, should be decoupled (>47 µF electrolytic and 0.1 µF ceramic capacitors are recommended) as close to the device as is physically practical. To minimize the effect of system ground I•R drops on the logic and reference input signals, the system ground should have a low-resistance return to the load supply voltage.

See also "Current Sensing" and "Thermal Considerations" above.

Fixed Off-Time Selection

With increasing values of t_{off}, switching losses decrease, low-level load-current regulation improves, EMI is reduced, the PWM frequency will decrease, and ripple current will increase. The value of t_{off} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{off} are chosen to be in the range of 15 to 35 µs.

Typical Bipolar Stepper Motor Application



Stepper Motor Applications

The MODE terminal can be used to optimize the performance of the device in microstepping/sinusoidal stepper motor drive applications. When the average load current is increasing, slow-decay mode is used to limit the switching losses in the device and iron losses in the motor. This also improves the maximum rate at which the load current can increase (as compared to fast decay) due to the slow rate of decay during t_{off}. When the average load current is decreasing, fast-decay mode is used to regulate the load current to the desired level. This prevents tailing of the current profile caused by the back-EMF voltage of the stepper motor.

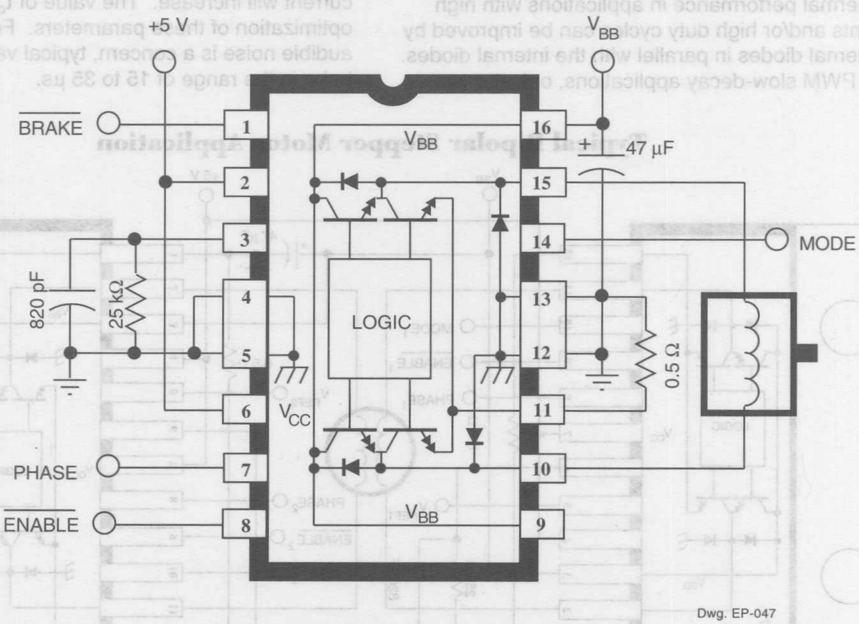
In stepper motor applications applying a constant current to the load, slow-decay mode PWM is used typically to limit the switching losses in the device and iron losses in the motor.

DC Motor Applications

In closed-loop systems, the speed of a dc motor can be controlled by PWM of the PHASE or ENABLE inputs, or by varying the REF input voltage (V_{REF}). In digital systems (microprocessor controlled), PWM of the PHASE or ENABLE input is used typically thus avoiding the need to generate a variable analog voltage reference. In this case, a dc voltage on the REF input is used typically to limit the maximum load current.

In dc servo applications that require accurate positioning at low or zero speed, PWM of the PHASE input is selected typically. This simplifies the servo-control loop because the transfer function between the duty cycle on the PHASE input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low-current levels).

Typical DC Servo Motor Application



With bidirectional dc servo motors, the PHASE terminal can be used for mechanical direction control. Similar to when braking the motor dynamically, abrupt changes in the direction of a rotating motor produce a current generated by the back EMF. The current generated will depend on the mode of operation. If the internal current-control circuitry is not being used, then the maximum load current generated can be approximated by

$$I_{LOAD} = (V_{BEMF} + V_{BB})/R_{LOAD}$$

where V_{BEMF} is proportional to the motor's speed. If the internal slow-decay current-control circuitry is used, then the maximum load current generated can be approximated by $I_{LOAD} = V_{BEMF}/R_{LOAD}$. For both cases, care must be taken to ensure the maximum ratings of the device are not exceeded. If the internal fast-decay current-control circuitry is used, then the load current will regulate to a value given by

$$I_{LOAD} = V_{REF}/(10 \bullet R_S).$$

CAUTION: In fast-decay mode, when the direction of the motor is changed abruptly, the kinetic energy stored in the motor and load inertia will be converted into current that charges the V_{BB} supply bulk capacitance (power supply output and decoupling capacitance). Care must be taken to ensure the capacitance is sufficient to absorb the energy without exceeding the voltage rating of any devices connected to the motor supply.

See also, the sections on brake operation under "Functional Description," above.

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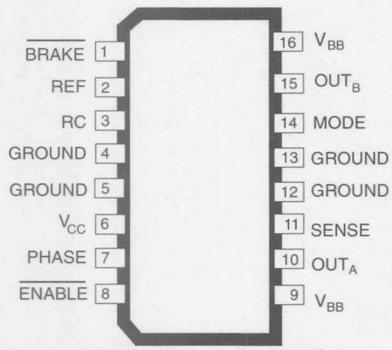
FULL-BRIDGE PWM MOTOR DRIVER



Note the A3953SB (DIP) and the A3953SLB (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} . . . . **50 V**

Output Current, I_{OUT}
(Continuous) . . . . **±1.3 A***

Logic Supply Voltage, V_{CC} . . . . **7.0 V**

Logic/Reference Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{CC} + 0.3 V**

Sense Voltage, V_{SENSE} D.C.
(V_{CC} = 5.0 V) . . . . **1.0 V**
(V_{CC} = 3.3 V) . . . . **0.4 V**

Package Power Dissipation,
P_D . . . . **See Graph**

Operating Temperature Range,
T_A . . . . **-20°C to +85°C**

Junction Temperature, T_J . . . . **+150°C†**

Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

† Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed for bidirectional pulse-width modulated (PWM) current control of inductive loads, the A3953S— is capable of continuous output currents to ±1.3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off-time pulse duration is set by a user-selected external RC timing network. Internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover current protection. Special power-up sequencing is not required.

With the ENABLE input held low, the PHASE input controls load current polarity by selecting the appropriate source and sink driver pair. The MODE input determines whether the PWM current-control circuitry operates in a slow current-decay mode (only the selected source driver switching) or in a fast current-decay mode (selected source and sink switching). A user-selectable blanking window prevents false triggering of the PWM current-control circuitry. With the ENABLE input held high, all output drivers are disabled. A sleep mode is provided to reduce power consumption.

When a logic low is applied to the BRAKE input, the braking function is enabled. This overrides ENABLE and PHASE to turn OFF both source drivers and turn ON both sink drivers. The brake function can be used to dynamically brake brush dc motors.

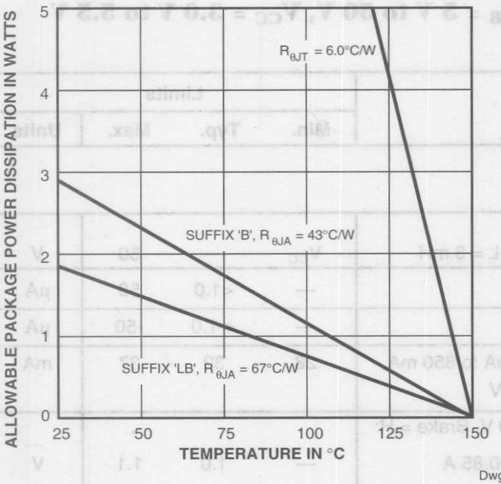
The A3953S— is supplied in a choice of two power packages: a 16-pin dual-in-line plastic package with copper heat-sink tabs, and a 16-lead plastic SOIC with copper heat-sink tabs. For both package styles, the power tab is at ground potential and needs no electrical isolation.

FEATURES

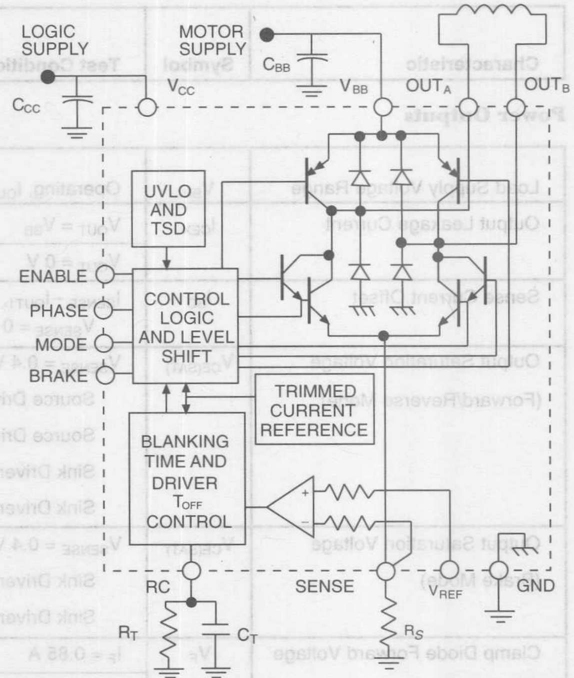
- ±1.3 A Continuous Output Current Rating, 50 V Output Voltage Rating
- 3.0 to 5.5 V Logic Supply Voltage
- Internal PWM Current Control, Saturated Sink Drivers
- Fast and Slow Current Decay Modes
- Automotive Capable
- Sleep (Low Current Consumption) Mode
- Internal Transient-Suppression Diodes
- Internal Thermal-Shutdown Circuitry
- Crossover-Current Protection, UVLO Protection

Always order by complete part number:

PART NUMBER	PACKAGE	$R_{\theta JA}$	$R_{\theta JT}$
A3953SB	16-Pin DIP	43°C/W	6°C/W
A3953SLB	16-Lead SOIC	67°C/W	6°C/W



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

BRAKE	ENABLE	PHASE	MODE	OUT_A	OUT_B	DESCRIPTION
H	H	X	H	Off	Off	Sleep Mode
H	H	X	L	Off	Off	Standby
H	L	H	H	H	L	Forward, Fast Current-Decay Mode
H	L	H	L	H	L	Forward, Slow Current-Decay Mode
H	L	L	H	L	H	Reverse, Fast Current-Decay Mode
H	L	L	L	L	H	Reverse, Slow Current-Decay Mode
L	X	X	H	L	L	Brake, Fast Current-Decay Mode
L	X	X	L	L	L	Brake, No Current Control

X = Irrelevant

ELECTRICAL CHARACTERISTICS at $T_J = 25^\circ C$, V_{BB} = 5 V to 50 V, V_{CC} = 3.0 V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Power Outputs						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±1.3 A, L = 3 mH	V_{CC}	—	50	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	μA
		V_{OUT} = 0 V	—	<-1.0	-50	μA
Sense Current Offset	I_{SO}	I_{SENSE} - I_{OUT1}, I_{OUT} = 50 mA to 850 mA, V_{SENSE} = 0 V, V_{CC} = 5 V	28	32	37	mA
Output Saturation Voltage (Forward/Reverse Mode)	$V_{CE(SAT)}$	V_{SENSE} = 0.4 V, V_{CC} = 3.0 V, Brake = H:				
		Source Driver, I_{OUT} = -0.85 A	—	1.0	1.1	V
		Source Driver, I_{OUT} = -1.3 A	—	1.7	1.9	V
		Sink Driver, I_{OUT} = 0.85 A	—	0.4	0.5	V
		Sink Driver, I_{OUT} = 1.3 A	—	1.1	1.3	V
Output Saturation Voltage (Brake Mode)	$V_{CE(SAT)}$	V_{SENSE} = 0.4 V, V_{CC} = 3.0 V, Brake = L:				
		Sink Driver, I_{OUT} = 0.85 A	—	1.0	1.2	V
		Sink Driver, I_{OUT} = 1.3 A	—	1.3	1.5	V
Clamp Diode Forward Voltage (Sink or Source)	V_F	I_F = 0.85 A	—	1.15	1.25	V
		I_F = 1.3 A	—	1.35	1.5	V

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ELECTRICAL CHARACTERISTICS at $T_J = 25°C$, $V_{BB} = 5$ V to 50 V, $V_{CC} = 3.0$ V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
AC Timing						
PWM RC Fixed Off-time	$t_{OFF\ RC}$	C_T = 680 pF, R_T= 30 kΩ, V_{CC} = 3.3 V	18.3	20.4	22.5	µs
PWM Turn Off Time	t_{PWM}	Comparator Trip to Source OFF	—	1.0	1.5	µs
PWM Turn On Time	t_{PWM}	IRC Charge ON to Source ON	0.3	0.4	0.7	µs
PWM Minimum On Time	$t_{ON(min)}$	$R_T \geq 12$ kΩ:				
		V_{CC} = 3.3 V, C_T = 680 pF ± 5%	0.8	1.3	1.9	µs
		V_{CC} = 5.0 V, C_T = 470 pF ± 5%	0.8	1.3	1.9	µs
Propagation Delay Times	t_{pd}	I_{OUT} = ± 1.3 A, 50% to 90%:				
		ENABLE ON to Source ON	—	1.0	—	µs
		ENABLE OFF to Source OFF	—	1.0	—	µs
		ENABLE ON to Sink ON	—	1.0	—	µs
		ENABLE OFF to Sink OFF	—	0.8	—	µs
		PHASE Change to Sink ON	—	2.4	—	µs
		PHASE Change to Sink OFF	—	0.8	—	µs
		PHASE Change to Source ON	—	2.4	—	µs
		PHASE Change to Source OFF	—	1.0	—	µs
Crossover Dead Time	t_{CODT}	1 kΩ Load to 25 V	0.3	1.5	3.0	µs

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ELECTRICAL CHARACTERISTICS at T_J = 25°C, V_{BB} = 5 V to 50 V, V_{CC} = 3.0 V to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Circuitry						
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Enable Threshold			2.5	2.75	3.0	V
UVLO Hysteresis			0.15	0.20	0.25	V
Logic Supply Current	$I_{CC(ON)}$	V_{ENABLE} = 0.8 V, V_{BRAKE} = 2.0 V	—	42	50	mA
	$I_{CC(OFF)}$	V_{ENABLE} = 2.0 V, V_{MODE} = 0.8 V	—	12	15	mA
	$I_{CC(Brake)}$	V_{BRAKE} = 0.8 V	—	42	50	mA
	$I_{CC(Sleep)}$	V_{ENABLE} = V_{MODE} = V_{BRAKE} = 2.0 V	—	400	800	μA
Motor Supply Current (No Load)	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V	—	3.0	5.0	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 2.0 V, V_{MODE} = 0.8 V	—	1.0	50	μA
	$I_{BB(Brake)}$	V_{BRAKE} = 0.8 V	—	1.0	50	μA
	$I_{BB(Sleep)}$	V_{ENABLE} = V_{MODE} = 2.0 V	—	1.0	50	μA
Logic Supply Voltage Range	V_{CC}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	<1.0	20	μA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-200	μA
V_{SENSE} Voltage Range	$V_{SENSE(3.3)}$	V_{CC} = 3.0 V to 3.6 V	0	—	0.4	V
	$V_{SENSE(5.0)}$	V_{CC} = 4.5 V to 5.5 V	0	—	1.0	V
Reference Input Current	I_{REF}	V_{REF} = 0 V to 1 V	—	—	±5.0	μA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V	—	±2.0	±5.0	mV

FUNCTIONAL DESCRIPTION

Internal PWM Current Control During Forward and Reverse Operation. The A3953 contains a fixed off-time pulse-width modulated (PWM) current control circuit that can be used to limit the load current to a desired value. The peak value of the current limiting (I_{TRIP}) is set by the selection of an external current sensing resistor (R_{SENSE}) and reference input voltage (V_{REF}). The internal circuitry compares the voltage across the external sense resistor to the voltage on the reference input terminal (REF) resulting in a transconductance function approximated by:

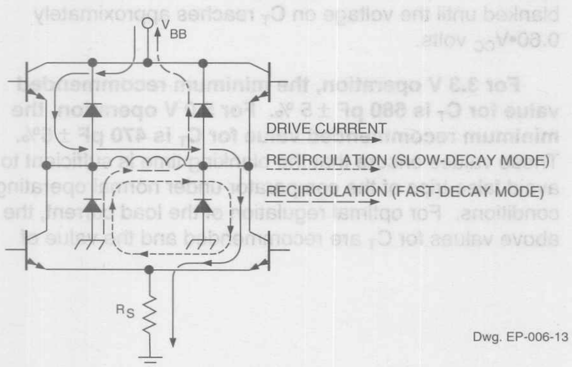
$$I_{TRIP} \approx \frac{V_{REF}}{R_{SENSE}} - I_{SO}$$

where I_{SO} is the offset due to base drive current.

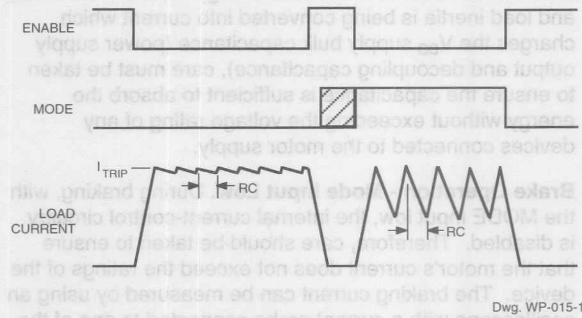
In forward or reverse mode the current-control circuitry limits the load current as follows: when the load current reaches I_{TRIP}, the comparator resets a latch that turns off the selected source driver or selected sink and source driver pair depending on whether the device is operating in slow or fast current-decay mode, respectively.

In slow current-decay mode, the selected source driver is disabled; the load inductance causes the current to recirculate through the sink driver and ground clamp diode. In fast current-decay mode, the selected sink and source driver pair are disabled; the load inductance causes the current to flow from ground to the load supply via the ground clamp and flyback diodes.

Figure 1 - Load-Current Paths



The user selects an external resistor (R_T) and capacitor (C_T) to determine the time period ($t_{OFF} = R_T \bullet C_T$) during which the drivers remain disabled (see “RC Fixed Off-time” below). At the end of the RC interval, the drivers are enabled allowing the load current to increase again. The PWM cycle repeats maintaining the peak load current at the desired value (see figure 2).



INTERNAL PWM CURRENT CONTROL DURING BRAKE MODE OPERATION

Brake Operation - Mode Input High. The brake circuit turns OFF both source drivers and turns ON both sink drivers. For dc motor applications, this has the effect of shorting the motor’s back-EMF voltage resulting in current flow that dynamically brakes the motor. If the back-EMF voltage is large, and there is no PWM current limiting, the load current can increase to a value that approaches that of a locked rotor condition. To limit the current, when the I_{TRIP} level is reached, the PWM circuit disables the conducting sink drivers. The energy stored in the motor’s inductance is discharged into the load supply causing the motor current to decay.

As in the case of forward/reverse operation, the drivers are enabled after a time given by $t_{OFF} = R_T \bullet C_T$ (see “RC Fixed Off-time” below). Depending on the back-EMF voltage (proportional to the motor’s decreasing speed), the load current again may increase to I_{TRIP}. If so, the PWM cycle will repeat, limiting the peak load current to the desired value.

During braking, when the MODE input is high, the peak current limit can be approximated by:

$$I_{TRIP\ BRAKE\ MH} \approx \frac{V_{REF}}{R_{SENSE}}$$

CAUTION: Because the kinetic energy stored in the motor and load inertia is being converted into current which charges the V_{BB} supply bulk capacitance (power supply output and decoupling capacitance), care must be taken to ensure the capacitance is sufficient to absorb the energy without exceeding the voltage rating of any devices connected to the motor supply.

Brake Operation - Mode Input Low. During braking, with the MODE input low, the internal current-control circuitry is disabled. Therefore, care should be taken to ensure that the motor's current does not exceed the ratings of the device. The braking current can be measured by using an oscilloscope with a current probe connected to one of the motor's leads, or if the back-EMF voltage of the motor is known, approximated by:

$$I_{PEAK\ BRAKE\ ML} \approx \frac{V_{BEMF} - 1V}{R_{LOAD}}$$

RC Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one-shot time, t_{OFF} (fixed off-time), is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected in parallel from the RC timing terminal to ground. The fixed off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ, is approximated by:

$$t_{OFF} \approx R_T \bullet C_T$$

The operation of the circuit is as follows: when the PWM latch is reset by the current comparator, the voltage on the RC terminal will begin to decay from approximately 0.60•V_{CC} volts. When the voltage on the RC terminal reaches approximately 0.22•V_{CC} volts, the PWM latch is set, thereby enabling the driver(s).

RC Blanking. In addition to determining the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the comparator when the outputs are switched by the internal current-control circuitry (or by the PHASE, BRAKE or ENABLE inputs). The comparator output is blanked to prevent false over-current detections due to reverse recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{OFF} time, the comparator's output is blanked and C_T begins to be charged from approximately 0.22•V_{CC} by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 0.60•V_{CC} volts.

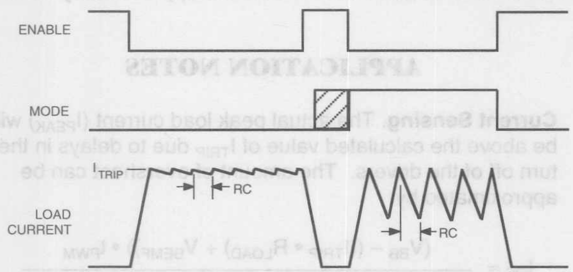
When a transition of the PHASE input occurs, C_T is discharged to <u>near ground</u> during the crossover delay time (The crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 0.60•V_{CC} volts.

When the device is disabled, via the ENABLE input, C_T is discharged to <u>near ground</u>. When the device is re-enabled, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 0.60•V_{CC} volts.

For 3.3 V operation, the minimum recommended value for C_T is 680 pF ± 5 %. For 5.0 V operation, the minimum recommended value for C_T is 470 pF ± 5%. These values ensure that the blanking time is sufficient to avoid false trips of the comparator under normal operating conditions. For optimal regulation of the load current, the above values for C_T are recommended and the value of

R_T can be sized to determine the load current. For more information regarding load current regulation, see below.

Figure 2
Fast and Slow Current-Decay Waveforms



LOAD CURRENT REGULATION WITH THE INTERNAL PWM CURRENT-CONTROL CIRCUITRY

When the device is operating in slow current-decay mode, there is a limit to the lowest level that the PWM current-control circuitry can regulate load current. The limitation is the minimum duty cycle, which is a function of the user-selected value of t_{OFF} and the minimum on-time pulse $t_{ON\ (min)}$ max that occurs each time the PWM latch is reset. If the motor is not rotating, as in the case of a stepper motor in hold/detent mode, a brush dc motor when stalled or at startup, the worst case value of current regulation can be approximated by:

$$I_{AVE} \approx \frac{[(V_{BB} - V_{SAT(source+sink)}) \bullet t_{ON(min)}\text{max}] - (1.05(V_{SAT(sink)} + V_F) \bullet t_{OFF})}{1.05 \bullet (t_{ON(min)}\text{max} + t_{OFF}) \bullet R_{LOAD}}$$

where $t_{OFF} = R_T{\bullet}C_T$, R_{LOAD} is the series resistance of the load, V_{BB} is the motor supply voltage and $t_{ON\ (min)}$max is specified in the electrical characteristics table. When the motor is rotating, the back EMF generated will influence the above relationship. For brush dc motor applications, the current regulation is improved. For stepper motor applications when the motor is rotating, the effect is more complex. A discussion of this subject is included in the section on stepper motors below.

The following procedure can be used to evaluate the worst case slow current-decay internal PWM load current regulation in the system:

Set V_{REF} to 0 volts. With the load connected and the PWM current control operating in slow current-decay mode, use an oscilloscope to measure the time the output is low (sink ON) for the output that is chopping. This is the typical minimum ON time ($t_{ON\ (min)}$ typ) for the device. The C_T then should be increased until the measured value of $t_{ON\ (min)}$ is equal to $t_{ON\ (min)}$ max as specified in the electrical characteristics table. When the new value of C_T has been set, the value of R_T should be decreased so the value for $t_{OFF} = R_T{\bullet}C_T$ (with the artificially increased value of C_T) is equal to the nominal design value. The worst-case load-current regulation then can be measured in the system under operating conditions.

PWM of the Phase And Enable Inputs. The PHASE and ENABLE inputs can be pulse-width modulated to regulate load current. Typical propagation delays from the PHASE and ENABLE inputs to transitions of the power outputs are specified in the electrical characteristics table. If the internal PWM current control is used, the comparator blanking function is active during phase and enable transitions. This eliminates false tripping of the over-current comparator caused by switching transients (see “RC Blanking” above).

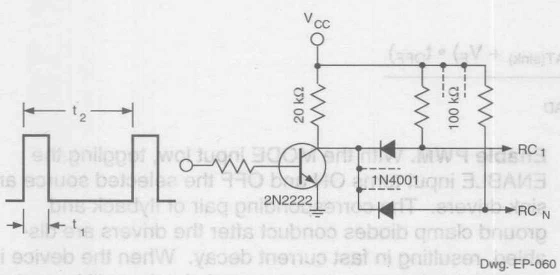
Enable PWM. With the MODE input low, toggling the ENABLE input turns ON and OFF the selected source and sink drivers. The corresponding pair of flyback and ground clamp diodes conduct after the drivers are disabled, resulting in fast current decay. When the device is enabled the internal current control circuitry will be active and can be used to limit the load current in a slow current-decay mode.

For applications that PWM the ENABLE input and desire that the internal current-limiting circuit to function in the fast decay mode, the ENABLE input signal should be inverted and connected to the MODE input. This prevents the device from being switched into sleep mode when the ENABLE input is low.

Phase PWM. Toggling the PHASE terminal selects which sink/source pair is enabled, producing a load current that varies with the duty cycle and remains continuous at all times. This can have added benefits in bidirectional brush dc servo motor applications as the transfer function between the duty cycle on the PHASE input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low current levels). For more information see "DC Motor Applications" below.

Synchronous Fixed Frequency PWM. The internal PWM current control circuitry of multiple A3953S— devices can be synchronized by using the simple circuit shown in figure 3. A 555 IC can be used to generate the reset pulse/blanking signal (t_1) for the device and the period of the PWM cycle (t_2). The value of t_1 should be a minimum of 1.5 µs. When used in this configuration the R_T and C_T components should be omitted. The PHASE and ENABLE inputs should not be PWM with this circuit configuration due to the absence of a blanking function synchronous with their transitions.

Figure 3
Synchronous Fixed Frequency Control Circuit



Miscellaneous Information. A logic high applied to both the ENABLE and MODE terminals puts the device into a sleep mode to minimize current consumption when not in use.

An internally generated dead time prevents crossover currents that can occur when switching phase or braking.

Thermal protection circuitry turns OFF all drivers should the junction temperature reach 165°C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The hysteresis of the thermal shutdown circuit is approximately 15°C.

APPLICATION NOTES

Current Sensing. The actual peak load current (I_{PEAK}) will be above the calculated value of I_{TRIP} due to delays in the turn off of the drivers. The amount of overshoot can be approximated by:

$$I_{OS} \approx \frac{(V_{BB} - ((I_{TRIP} \bullet R_{LOAD}) + V_{BEMF})) \bullet t_{PWM}}{L_{LOAD}}$$

where V_{BB} is the motor supply voltage, V_{BEMF} is the back-EMF voltage of the load, R_{LOAD} and L_{LOAD} are the resistance and inductance of the load respectively, and t_{PWM} is specified in the electrical characteristics table.

The reference input terminal has a bias current of ± 5 µs. This current should be taken into account when determining the impedance of the external circuit that sets the reference voltage value.

To minimize current sensing inaccuracies caused by ground trace I•R drops, the current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the I•R drops in the PCB can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_{SENSE}.

Generally, larger values of R_{SENSE} reduce the aforementioned effects but can result in excessive heating and power loss in the sense resistor. The selected value of R_{SENSE} should not cause the absolute maximum voltage rating of 1.0 V (0.4 V for V_{CC} = 3.3 V operation), for the SENSE terminal, to be exceeded.

The current-sensing comparator functions down to ground allowing the device to be used in microstepping, sinusoidal, and other varying current-profile applications.

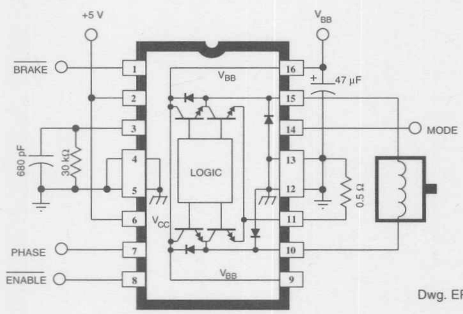
Thermal Considerations. For reliable operation it is recommended that the maximum junction temperature be kept below 110 to 125°C. The junction temperature can

be measured best by attaching a thermocouple to the power tab/batwing of the device and measuring the tab temperature, T_{TAB}. The junction temperature can then be approximated by using the formula:

$$T_J \approx T_{TAB} + (I_{LOAD} \bullet 2 \bullet V_F \bullet R_{\theta JT})$$

Where V_F can be chosen from the electrical specification table for the given level of I_{LOAD}. The value for $R_{\theta JT}$ is given in the package thermal resistance table for the appropriate package.

The power dissipation of the batwing packages can be improved by 20 to 30% by adding a section of printed circuit board copper (typically 6 to 18 square centimeters) connected to the batwing terminals of the device.



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The thermal performance in applications that run at high load currents and/or high duty cycles can be improved by adding external diodes in parallel with the internal diodes. In internal PWM slow decay applications only the two ground clamp diodes need be added. For internal fast decay PWM, or external PHASE or ENABLE input PWM applications, all four external diodes should be added for maximum junction temperature reduction.

PCB Layout. The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (> 47 µF is recommended) placed as close to the device as is physically practical. To minimize the effect of system ground I•R drops on the logic and reference input signals the system ground should have a low-resistance return to the motor supply voltage.

See also "Current Sensing" and "Thermal Considerations" above.

Fixed Off-Time Selection. With increasing values of t_{OFF}, switching losses will decrease, low-level load current regulation will improve, EMI will be reduced, the PWM frequency will decrease, and ripple current will increase. The value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} are chosen to be in the range of 15 to 35 µs.

Stepper Motor Applications. The MODE terminal can be used to optimize the performance of the device in microstepping/sinusoidal stepper motor drive applications. When the load current is increasing, slow decay mode is used to limit the switching losses in the device and iron losses in the motor. This also improves the maximum rate at which the load current can increase (as compared to fast decay) due to the slow rate of decay during t_{OFF}. When the load current is decreasing, fast decay mode is used to regulate the load current to the desired level. This prevents tailing of the current profile caused by the back EMF voltage of the stepper motor.

In stepper motor applications applying a constant current to the load, slow decay mode PWM is typically used to limit the switching losses in the device and iron losses in the motor.

DC Motor Applications. In closed loop systems, the speed of a dc motor can be controlled by PWM of the PHASE or ENABLE inputs, or by varying the reference (REF) input voltage. In digital systems (microprocessor controlled), PWM of the PHASE or ENABLE input is used typically thus avoiding the need to generate a variable analog voltage reference. In this case, a dc voltage on the REF input is used typically to limit the maximum load current.

In dc servo applications that require accurate positioning at low or zero speed, PWM of the PHASE input is selected typically. This simplifies the servo control loop because the transfer function between the duty cycle on the PHASE input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low current levels).

With bidirectional dc servo motors, the PHASE terminal can be used for mechanical direction control. Similar to when braking the motor dynamically, abrupt changes in the direction of a rotating motor produces a current generated by the back-EMF. The current gener-

ated will depend on the mode of operation. If the internal current control circuitry is not being used, then the maximum load current generated can be approximated by $I_{LOAD} = (V_{BEMF}+V_{BB})/R_{LOAD}$ where V_{BEMF} is proportional to the motor's speed. If the internal slow current-decay control circuitry is used, then the maximum load current generated can be approximated by $I_{LOAD} = V_{BEMF}/R_{LOAD}$. For both cases care must be taken to ensure the maximum ratings of the device are not exceeded. If the internal fast current-decay control circuitry is used, then the load current will regulate to a value given by:

$$I_{LOAD} = V_{REF}/R_S.$$

CAUTION: In fast current-decay mode, when the direction of the motor is changed abruptly, the kinetic energy stored in the motor and load inertia will be converted into current that charges the V_{BB} supply bulk capacitance (power supply output and decoupling capacitance). Care must be taken to ensure the capacitance is sufficient to absorb the energy without exceeding the voltage rating of any devices connected to the motor supply.

See also "Brake Operation" above.

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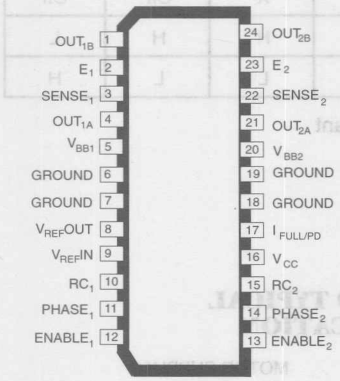
DUAL FULL-BRIDGE PWM MOTOR DRIVER



Note the A3961SB (DIP) and the A3961SLB (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} . . . . **45 V**

Output Current, I_{OUT} . . . . **±800 mA***

Logic Supply Voltage, V_{CC} . . . . **7.0 V**

Logic Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{CC} + 0.3 V**

Sense Voltage, V_{SENSE} . . . . **1.0 V**

Reference Output Current,
$I_{REF\ OUT}$ . . . . **1.0 mA**

Package Power Dissipation,
P_D . . . . **See Graph**

Operating Temperature Range,
T_A . . . . **-20°C to +85°C**

Junction Temperature, T_J . . . . **+150°C†**

Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed for pulse-width modulated (PWM) current control of bipolar stepper motors, the A3961S— is capable of continuous output currents to ±800 mA and operating voltages to 45 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. An internal precision voltage reference is provided to improve motor peak current control accuracy. The peak load current limit is set by the user's selection of an external resistor divider and current-sensing resistors.

The fixed off-time pulse duration is set by user-selected external RC timing networks. The capacitor in the RC timing network also determines a user-selectable blanking window that prevents false triggering of the PWM current control circuitry during switching transitions. This eliminates the need for two external RC filter networks on the current-sensing comparator inputs.

For each bridge the PHASE input controls load current polarity by selecting the appropriate source and sink driver pair. For each bridge the ENABLE input, when held high, disables the output drivers. Special power-up sequencing is not required. Internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover-current protection.

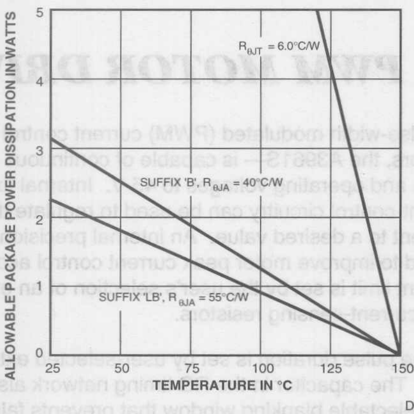
The A3961S— is supplied in a choice of two power packages: 24-pin dual-in-line plastic package with copper heat-sink tabs and 24-lead plastic SOIC with copper heat-sink tabs. In both packages the power tab is at ground potential and needs no electrical isolation.

FEATURES

- ±800 mA Continuous Output Current Rating
- 45 V Output Voltage Rating
- Internal PWM Current Control, Saturated Sink Drivers
- Internally Generated Precision 2.5 V Reference
- Internal Transient-Suppression Diodes
- Internal Thermal-Shutdown Circuitry
- Crossover-Current Protection, UVLO Protection

Always order by complete part number:

PART NUMBER	PACKAGE	$R_{\theta JA}$	$R_{\theta JT}$
A3961SB	24-Pin DIP	40°C/W	6°C/W
A3961SLB	24-Lead SOIC	55°C/W	6°C/W

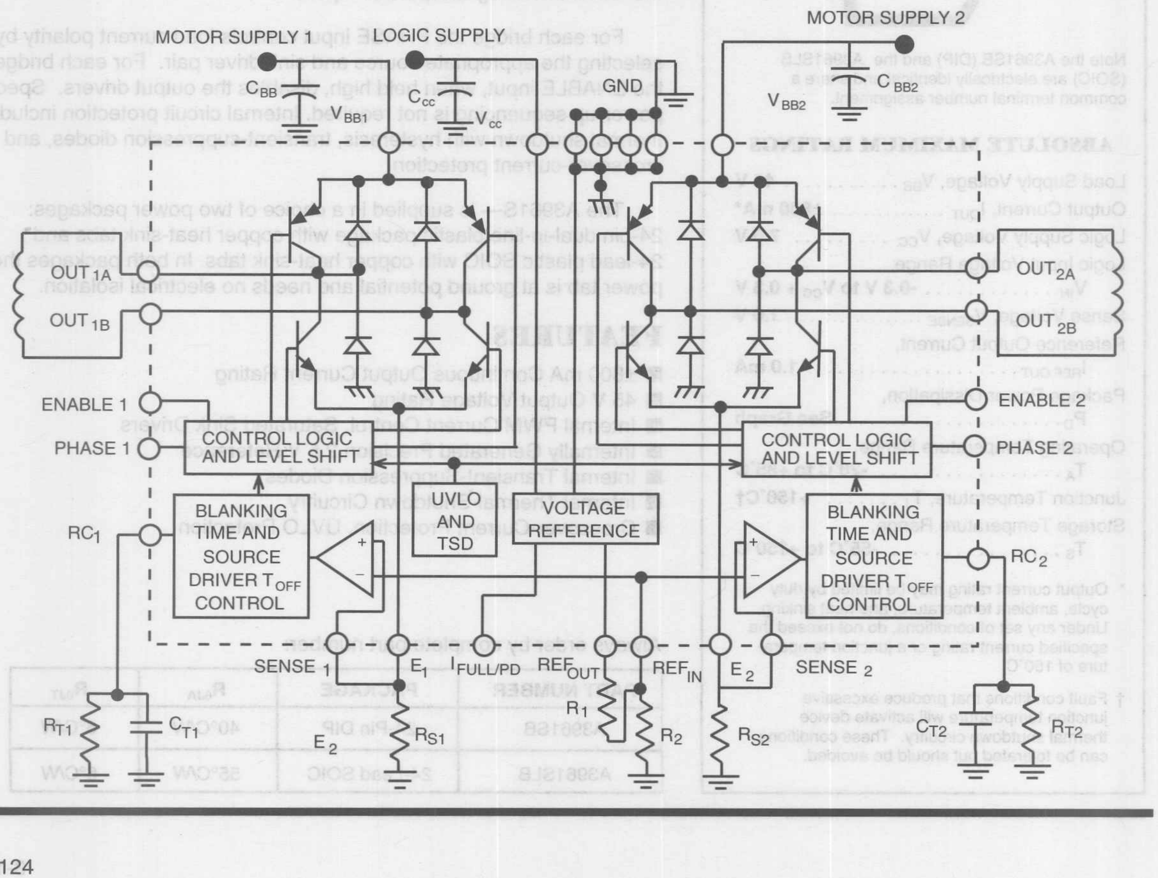


TRUTH TABLE

ENABLE	PHASE	OUT_A	OUT_B
H	X	Off	Off
L	H	H	L
L	L	L	H

X = Irrelevant

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL BIPOLAR STEPPER MOTOR APPLICATION



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{SENSE} = 0 V, 30 kΩ & 1000 pF RC to Ground (unless noted otherwise)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±800 mA, L = 3 mH	5.0	—	45	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<-1.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -500 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -750 mA	—	1.1	1.3	V
		Source Driver, I_{OUT} = -800 mA	—	—	1.4	V
		Sink Driver, I_{OUT} = +500 mA	—	0.3	0.6	V
		Sink Driver, I_{OUT} = +750 mA	—	0.5	0.9	V
		Sink Driver, I_{OUT} = +800 mA	—	—	1.0	V
Clamp Diode Forward Voltage (Sink or Source)	V_F	I_F = 500 mA	—	1.1	1.4	V
		I_F = 750 mA	—	1.3	1.6	V
		I_F = 800 mA	—	—	1.7	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V	—	5.0	7.0	mA
(No Load)	$I_{BB(OFF)}$	V_{ENABLE} = 2.4 V	—	5.0	7.0	mA
Control Logic						
Logic Supply Voltage Range	V_{CC}	Operating	4.75	—	5.25	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-200	µA
Reference Output Voltage	$V_{REF\ OUT}$	V_{CC} = 5.0 V, $I_{REF\ OUT}$ = 90 to 900 µA:				
		$I_{FULL/PD}$ = LOW	2.45	2.50	2.55	V
		$I_{FULL/PD}$ = HIGH	1.49	1.67	1.84	V

Continued next page…

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{SENSE} = 0 V, 30 kΩ & 1000 pF RC to Ground (unless noted otherwise) (cont.)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Control Logic (Continued)						
Reference Output Current	$I_{REF\,OUT}$	3 kΩ ≤ $R_D = R_1 + R_2$ ≤ 15 kΩ	90	—	900	µA
Ref. Input Offset Current	I_{OS}	$V_{REF\,IN}$ = 1 V	-2.5	0	1.0	µA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V	-5.0	0	5.0	mV
Comparator Input Volt. Range	V_{REF}	Operating	-0.3		1.0	V
PWM RC Fixed Off-time	$t_{OFF\,RC}$	C_T = 1000 pF, R_T = 30 kΩ	27	30	33	µs
PWM Propagation Delay Time	t_{PWM}	Comparator Trip to Source OFF	—	1.2	2.0	µs
PWM Minimum On Time	$t_{ON(min)}$	C_T = 1000 pF ± 5%, R_T ≥ 15 kΩ, V_{CC} = 5 V	—	2.5	3.6	µs
Propagation Delay Times	t_{pd}	I_{OUT} = ±800 mA, 50% to 90%:				
		ENABLE ON to Source ON	—	3.2	—	µs
		ENABLE OFF to Source OFF	—	1.2	—	µs
		ENABLE ON to Sink ON	—	3.2	—	µs
		ENABLE OFF to Sink OFF	—	0.7	—	µs
		PHASE Change to Sink ON	—	3.2	—	µs
		PHASE Change to Source ON	—	3.2	—	µs
		PHASE Change to Sink OFF	—	0.7	—	µs
		PHASE Change to Source OFF	—	1.2	—	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Disable Threshold			2.5	2.7	2.9	V
UVLO Hysteresis			0.7	0.9	1.1	V
Logic Supply Current	$I_{CC(ON)}$	$V_{ENABLE1} = V_{ENABLE2}$ = 0.8 V	—	65	85	mA
	$I_{CC(OFF)}$	$V_{ENABLE1} = V_{ENABLE2}$ = 2.4 V	—	11	15	
Logic Supply Current Temperature Coefficient	$\Delta I_{CC(ON)}$	$V_{ENABLE1} = V_{ENABLE2}$ = 0.8 V	—	0.18	—	mA/°C

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Internal PWM Current Control. The A3961S— contains a fixed off-time pulse-width modulated (PWM) current-control circuit that can be used to limit the load current to a desired value. The peak value of the current limiting (I_{TRIP}) is set by the selection of an external current-sensing resistor (R_{SENSE}) and reference input voltage ($V_{REF\ IN}$). The internal circuitry compares the voltage across the external sense resistor to the voltage on the reference input terminal ($V_{REF\ IN}$), resulting in a transconductance function approximated by:

$$I_{TRIP} \approx \frac{V_{REF\ IN}}{R_{SENSE}}$$

The reference input voltage is typically set with a resistor divider from $V_{REF\ OUT}$. The value of $V_{REF\ OUT}$ can be switched from a nominal value of 2.5 V to 1.67 V by applying a low or high logic signal respectively to the $I_{FULL/PD}$ terminal. To ensure proper operation of the voltage reference, the resistor divider ($R_D = R_1+R_2$) should have an impedance of 3 kΩ to 15 kΩ. Within this range, a low impedance will minimize the effect of the REF IN input offset current.

The current-control circuitry limits the load current as follows: when the load current reaches I_{TRIP}, the comparator resets a latch that turns off the selected source driver. The load inductance causes the current to recirculate through the sink driver and flyback diode.

For each bridge, the user selects an external resistor (R_T) and capacitor (C_T) to determine the time period ($t_{OFF} = R_T \bullet C_T$) during which the source driver remains disabled (see “RC Fixed Off-time” below). The range of recommended values for C_T and R_T are 1000 pF to 1500 pF and 15 kΩ to 100 kΩ respectively. For optimal load current regulation, C_T is normally set to 1000 pF (see “Load Current Regulation” below). At the end of the RC interval, the source driver is enabled allowing the load current to increase again. The PWM cycle repeats, maintaining the peak load current at the desired value.

RC BLANKING. In addition to determining the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the comparator when the outputs are switched by the internal current-control circuitry (or by the PHASE or ENABLE inputs). The comparator output is blanked to prevent false over-current detections due to reverse-recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{OFF} time, the comparator's output is blanked and C_T begins to be charged from approximately 1.1 volts by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

When a transition of the PHASE input occurs, C_T is discharged to near ground during the crossover delay time (The crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

When the device is disabled, via the ENABLE input, C_T is discharged to near ground. When the device is re-enabled, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

The minimum recommended value for C_T is 1000 pF. This value ensures that the blanking time is sufficient to avoid false trips of the comparator under normal operating conditions. For optimal regulation of the load current, the above value for C_T is recommended and the value of R_T can be sized to determine t_{OFF}. For more information regarding load current regulation, see below.

Load Current Regulation. Because the device operates in a slow decay mode (2-quadrant PWM mode), there is a limit to the lowest level that the PWM current control circuitry can regulate load current. The limitation is due to the minimum PWM duty cycle, which is a function of the user-selected value of t_{OFF} and the minimum on-time pulse $t_{ON(min)}$max that occurs each time the PWM latch is reset. If the motor is not rotating, as in the case of a stepper motor in hold/detent mode, a brush dc motor when stalled or at startup, the worst case value of current regulation can be approximated by:

$$I_{AVE} \approx \frac{[(V_{BB}-V_{SAT(SOURCE+SINK)}) \bullet t_{ON(min)}max] - (1.05 \bullet (V_{SAT(SINK)} + V_F) \bullet t_{OFF})}{1.05 \bullet (t_{ON(min)}max + t_{OFF}) \bullet R_{LOAD}}$$

where $t_{OFF} = R_TC_T$, R_{LOAD} is the series resistance of the load, V_{BB} is the motor supply voltage and $t_{ON(min)}$max is specified in the electrical characteristics table. When the motor is rotating, the back EMF generated will influence the above relationship. For brush dc motor applications, the current regulation is improved. For stepper motor applications when the motor is rotating, the effect is dependent on the polarity and magnitude of the motor's back EMF.

The following procedure can be used to evaluate the worst-case internal PWM load current regulation in the system:

Set V_{REF} to 0 volts. With the load connected and the PWM current control operating in slow decay mode, use an oscilloscope to measure the time the output is low (sink ON) for the output that is chopping. This is the typical minimum on time ($t_{ON(min)}$typ) for the device. The C_T then should be increased until the measured value of $t_{ON(min)}$ is equal to $t_{ON(min)}$max as specified in the electrical characteristics table. When the new value of C_T has been set, the value of R_T should be decreased so the value for $_{OFF} = R_T \bullet C_T$ (with the artificially increased value of C_T) is equal to the nominal design value. The worst-case load-current regulation then can be measured in the system under operating conditions.

PWM of the Phase and Enable Inputs. The PHASE and ENABLE inputs can be pulse width modulated to regulate load current. Typical propagation delays from the PHASE and ENABLE inputs to transitions of the power outputs are specified in the electrical characteristics table. If the internal PWM current control is used, the comparator blanking function is active during phase and enable transitions. This eliminates false tripping of the over-current comparator caused by switching transients (see "RC Blanking" above).

Enable PWM. Toggling the ENABLE input turns ON and OFF the selected source and sink drivers. The corresponding pair of flyback and ground clamp diodes conduct after the drivers are disabled, resulting in fast current decay. When the device is enabled the internal current-control circuitry will be active and can be used to limit the load current in a slow decay mode.

Phase PWM. Toggling the PHASE terminal selects which sink/source pair is enabled, producing a load current that varies with the duty cycle and remains continuous at all times. This can have added benefits in bidirectional brush dc servo motor applications as the transfer function between the duty cycle on the PHASE input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low current levels).

Miscellaneous Information. An internally generated dead time prevents crossover currents that can occur when switching phase.

Thermal protection circuitry turns OFF all drivers should the junction temperature reach 165°C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The hysteresis of the thermal shutdown circuit is approximately 15°C.

APPLICATION NOTES

Current Sensing. The actual peak load current (I_{PEAK}) will be above the calculated value of I_{TRIP} due to delays in the turn off of the drivers. The amount of overshoot can be approximated by:

$$I_{OS} \approx \frac{(V_{BB} - ((I_{TRIP} \bullet R_{LOAD}) + V_{BEMF})) \bullet t_{PWM}}{L_{LOAD}}$$

where V_{BB} is the motor supply voltage, V_{BEMF} is the back-EMF voltage of the load, R_{LOAD} and L_{LOAD} are the resistance and inductance of the load respectively, and t_{PWM} is specified in the electrical characteristics table.

To minimize current sensing inaccuracies caused by ground trace I•R drops, each current-sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the I•R drops in the PCB can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_{SENSE}.

Generally, larger values of R_{SENSE} reduce the aforementioned effects but can result in excessive heating and power loss in the sense resistor. The selected value of R_{SENSE} should not cause the absolute maximum voltage rating of 1.0 V, for the SENSE terminal, to be exceeded. The recommended value of R_{SENSE} is in the range of:

$$R_{SENSE} \approx \frac{0.5}{I_{TRIP}\text{max}} \pm 50\%$$

If desired, the reference input voltage can be filtered by placing a capacitor from REF_{IN} to ground. The ground return for this capacitor as well as R_2 should be independent from the high-current power-ground trace to avoid changes in REF_{IN} due to I•R drops.

Thermal Considerations. For reliable operation it is recommended that the maximum junction temperature be kept below 110 to 125°C. The junction temperature can be measured best by attaching a thermocouple to the power tab/batwing of the device and measuring the tab temperature, T_{TAB}. The junction temperature can then be approximated by using the formula:

$$T_J \approx T_{TAB} + (I_{LOAD} \bullet 2 \bullet V_F \bullet R_{\theta JT})$$

where V_F can be chosen from the electrical specification table for the given level of I_{LOAD}. The value for $R_{\theta JT}$ is given in the package thermal resistance table for the appropriate package.

The power dissipation of the batwing packages can be improved by 20 to 30% by adding a section of printed circuit board copper (typically 6 to 18 square centimeters) connected to the batwing terminals of the device.

The thermal performance in applications that run at high load currents and/or high duty cycles can be improved by adding external diodes from each output to ground in parallel with the internal diodes. Fast recovery (≤ 200 ns) diodes should be used to minimize switching losses.

The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (≥ 47 µF is recommended) placed as close to the device as is physically practical. To minimize the effect of system ground I•R drops on the logic and reference input signals the system ground should have a low-resistance return to the motor supply voltage.

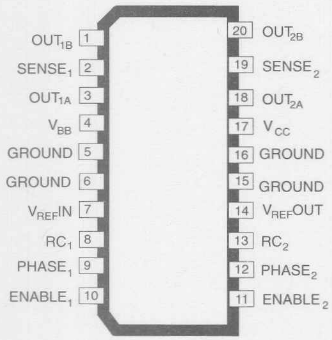
See also "Current Sensing" and "Thermal Considerations" above.

Fixed Off-Time Selection. With increasing values of t_{OFF}, switching losses will decrease, low-level load current regulation will improve, EMI will be reduced, the PWM frequency will decrease, and ripple current will increase. The value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} are chosen to be in the range of 15 to 35 µs.

3962

29319.27

DUAL FULL-BRIDGE PWM MOTOR DRIVER



Designed for pulse-width modulated (PWM) current control of bipolar stepper motors, the A3962SLB is capable of continuous output currents to ±800 mA and operating voltages to 30 V. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. An internal precision voltage reference is provided to improve motor peak-current control accuracy. The peak load current limit is set by the user's selection of an external resistor divider and current-sensing resistors.

The fixed off-time pulse duration is set by user-selected external RC timing networks. The capacitor in the RC timing network also determines a user-selectable blanking window that prevents false triggering of the PWM current control circuitry during switching transitions. This eliminates the need for two external RC filter networks on the current-sensing comparator inputs.

For each bridge the PHASE input controls load current polarity by selecting the appropriate source and sink driver pair. For each bridge the ENABLE input, when held high, disables the output drivers. Special power-up sequencing is not required. Internal circuit protection includes thermal shutdown with hysteresis, transient-suppression diodes, and crossover-current protection.

The A3962SLB is supplied in a 20-lead plastic SOIC with copper heat sink tabs. The power tab is at ground potential and needs no electrical isolation.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} .... **30 V**
Output Current, I_{OUT} .... **±800 mA***
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to V_{CC} + 0.3 V**
Sense Voltage, V_{SENSE} .... **1.0 V**
Reference Output Current,
$I_{REF\ OUT}$ .... **1.0 mA**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Junction Temperature, T_J .... **+150°C†**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

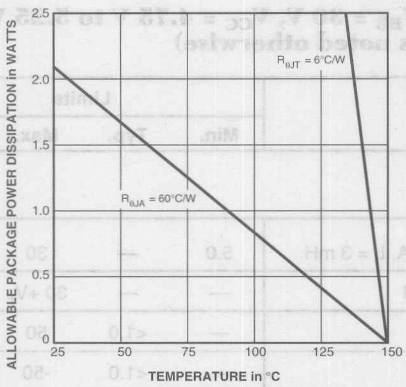
* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction tempera ture of 150°C.

† Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

FEATURES

- ±800 mA Continuous Output Current Rating
- 30 V Output Voltage Rating
- Internal PWM Current Control, Saturated Sink Drivers
- Internally Generated Precision 2.5 V Reference
- Internal Transient-Suppression Diodes
- Internal Thermal-Shutdown Circuitry
- Crossover-Current Protection, UVLO Protection
- Automotive Capable

Always order by complete part number: A3962SLB.



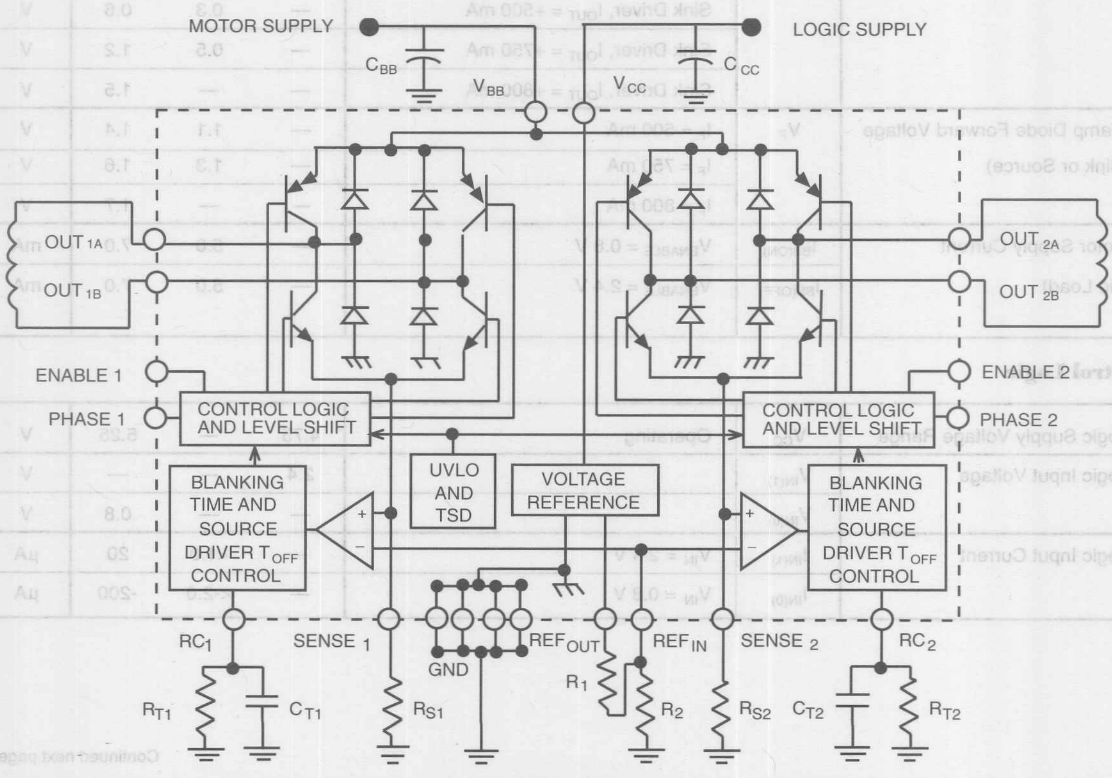
Dwg. GP-019-1

TRUTH TABLE

ENABLE	PHASE	OUT_A	OUT_B
H	X	Off	Off
L	H	H	L
L	L	L	H

X = Irrelevant

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL BIPOLAR STEPPER MOTOR APPLICATION



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 4.75 V to 5.25 V, V_{SENSE} = 0 V, 30 kΩ & 1000 pF RC to Ground (unless noted otherwise)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating, I_{OUT} = ±800 mA, L = 3 mH	5.0	—	30	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±800 mA, L = 3 mH	—	—	30 +V_F	V
Output Leakage Current	I_{CEX}	V_{OUT} = V_{BB}	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<1.0	-50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Driver, I_{OUT} = -500 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -750 mA	—	1.1	1.5	V
		Source Driver, I_{OUT} = -800 mA	—	—	1.7	V
		Sink Driver, I_{OUT} = +500 mA	—	0.3	0.6	V
		Sink Driver, I_{OUT} = +750 mA	—	0.5	1.2	V
		Sink Driver, I_{OUT} = +800 mA	—	—	1.5	V
Clamp Diode Forward Voltage (Sink or Source)	V_F	I_F = 500 mA	—	1.1	1.4	V
		I_F = 750 mA	—	1.3	1.6	V
		I_F = 800 mA	—	—	1.7	V
Motor Supply Current (No Load)	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V	—	5.0	7.0	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 2.4 V	—	5.0	7.0	mA
Control Logic						
Logic Supply Voltage Range	V_{CC}	Operating	4.75	—	5.25	V
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	<-2.0	-200	µA

Continued next page…

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 4.75 V to 5.25 V, V_{SENSE} = 0 V, 30 kΩ & 1000 pF RC to Ground (unless noted otherwise) (cont.)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Control Logic (Continued)						
Reference Output Voltage	$V_{REF\ OUT}$	V_{CC} = 5.0 V, $I_{REF\ OUT}$ = 90 to 900 μA	2.45	2.50	2.55	V
Reference Output Current	$I_{REF\ OUT}$	3 kΩ ≤ R_D = R_1 + R_2 ≤ 15 kΩ	150	—	900	μA
Ref. Input Offset Current	I_{OS}	$V_{REF\ IN}$ = 1 V	-2.5	0	1.0	μA
Comparator Input Offset Volt.	V_{IO}	V_{REF} = 0 V	-6.0	0	6.0	mV
Comparator Input Volt. Range	V_{REF}	Operating	-0.3	—	1.0	V
PWM RC Fixed Off-time	$t_{OFF\ RC}$	C_T = 1000 pF, R_T = 30 kΩ	27	30	33	μs
PWM Propagation Delay Time	t_{PWM}	Comparator Trip to Source OFF	—	1.2	2.0	μs
PWM Minimum On Time	$t_{ON\ (min)}$	C_T = 1000 pF ± 5%, R_T ≥ 15 kΩ, V_{CC} = 5 V	—	2.5	3.6	μs
Propagation Delay Times	t_{pd}	I_{OUT} = ±800 mA, 50% to 90%:				
		ENABLE ON to Source ON	—	3.2	—	μs
		ENABLE OFF to Source OFF	—	1.2	—	μs
		ENABLE ON to Sink ON	—	3.2	—	μs
		ENABLE OFF to Sink OFF	—	0.7	—	μs
		PHASE Change to Sink ON	—	3.2	—	μs
		PHASE Change to Source ON	—	3.2	—	μs
		PHASE Change to Sink OFF	—	0.7	—	μs
		PHASE Change to Source OFF	—	1.2	—	μs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
UVLO Disable Threshold			2.5	2.7	2.9	V
UVLO Hysteresis			0.7	0.9	1.1	V
Logic Supply Current	$I_{CC(ON)}$	$V_{ENABLE1}$ = $V_{ENABLE2}$ = 0.8 V	—	60	85	mA
	$I_{CC(OFF)}$	$V_{ENABLE1}$ = $V_{ENABLE2}$ = 2.4 V	—	11	17	mA
Logic Supply Current Temperature Coefficient	$\Delta I_{CC(ON)}$	$V_{ENABLE\ 1}$ = $V_{ENABLE\ 2}$ = 0.8 V	—	0.18	—	mA/°C

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

FUNCTIONAL DESCRIPTION

Internal PWM Current Control. The A3962SLB contains a fixed off-time pulse-width modulated (PWM) current-control circuit that can be used to limit the load current to a desired value. The peak value of the current limiting (I_{TRIP}) is set by the selection of an external current-sensing resistor (R_{SENSE}) and reference input voltage ($V_{REF\ IN}$). The internal circuitry compares the voltage across the external sense resistor to the voltage on the reference input terminal ($V_{REF\ IN}$) resulting in a transconductance function approximated by:

$$I_{TRIP} \approx \frac{V_{REF\ IN}}{R_{SENSE}}$$

The reference input voltage is typically set with a resistor divider from $V_{REF\ OUT}$. To ensure proper operation of the voltage reference, the resistor divider ($R_D = R_1+R_2$) should have an impedance of 3 kΩ to 15 kΩ. Within this range, a low impedance will minimize the effect of the REF IN input offset current.

The current-control circuitry limits the load current as follows: when the load current reaches I_{TRIP}, the comparator resets a latch that turns off the selected source driver. The load inductance causes the current to recirculate through the sink driver and flyback diode.

For each bridge, the user selects an external resistor (R_T) and capacitor (C_T) to determine the time period ($t_{OFF} = R_T \bullet C_T$) during which the source driver remains disabled (see "RC Fixed Off-time" below). The range of recommended values for C_T and R_T are 1000 pF to 1500 pF and 15 kΩ to 100 kΩ respectively. For optimal load current regulation, C_T is normally set to 1000 pF (see "Load Current Regulation" below). At the end of the RC interval, the source driver is enabled allowing the load current to increase again. The PWM cycle repeats, maintaining the peak load current at the desired value.

RC Blanking. In addition to determining the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the comparator when the outputs are switched by the internal current-control circuitry (or by the PHASE or ENABLE inputs). The comparator output is blanked to prevent false over-current detections due to reverse-recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{OFF} time, the comparator's output is blanked and C_T begins to be charged from approximately 1.1 volts by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

When a transition of the PHASE input occurs, C_T is discharged to near ground during the crossover delay time (The crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

When the device is disabled, via the ENABLE input, C_T is discharged to near ground. When the device is re-enabled, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately 3.0 volts.

The minimum recommended value for C_T is 1000 pF. This value ensures that the blanking time is sufficient to avoid false trips of the comparator under normal operating conditions. For optimal regulation of the load current, the above value for C_T is recommended and the value of R_T can be sized to determine t_{OFF}. For more information regarding load current regulation, see below.

Load Current Regulation. Because the device operates in a slow decay mode (2-quadrant PWM mode), there is a limit to the lowest level that the PWM current control circuitry can regulate load current. The limitation is due to the minimum PWM duty cycle, which is a function of the user-selected value of t_{OFF} and the minimum on-time pulse $t_{ON(min)}$max that occurs each time the PWM latch is reset. If the motor is not rotating, as in the case of a stepper motor in hold/detent mode, a brush dc motor when stalled or at startup, the worst case value of current regulation can be approximated by:

$$I_{AVE} \approx \frac{[(V_{BB} - V_{SAT(SOURCE+SINK)}) \bullet t_{ON(min)}\text{max}] - (1.05 \bullet (V_{SAT(SINK)} + V_F) \bullet t_{OFF})}{1.05 \bullet (t_{ON(min)}\text{max} + t_{OFF}) \bullet R_{LOAD}}$$

where $t_{OFF} = R_T C_T$, R_{LOAD} is the series resistance of the load, V_{BB} is the motor supply voltage and $t_{ON(min)}$max is specified in the electrical characteristics table. When the motor is rotating, the back EMF generated will influence the above relationship. For brush dc motor applications, the current regulation is improved. For stepper motor applications when the motor is rotating, the effect is dependent on the polarity and magnitude of the motor's back EMF.

The following procedure can be used to evaluate the worst case internal PWM load current regulation in the system:

Set V_{REF} to 0 volts. With the load connected and the PWM current control operating in slow decay mode, use an oscilloscope to measure the time the output is low (sink ON) for the output that is chopping. This is the typical minimum on time ($t_{ON(min)}$typ) for the device. The C_T then should be increased until the measured value of $t_{ON(min)}$ is equal to $t_{ON(min)}$max as specified in the electrical characteristics table. When the new value of C_T has been set, the value of R_T should be decreased so the value for $t_{OFF} = R_T \bullet C_T$ (with the artificially increased value of C_T) is equal to the nominal design value. The worst-case load-current regulation then can be measured in the system under operating conditions.

PWM of the Phase and Enable Inputs. The PHASE and ENABLE inputs can be pulse width modulated to regulate load current. Typical propagation delays from the PHASE and ENABLE inputs to transitions of the power outputs are specified in the electrical characteristics table. If the internal PWM current control is used, the comparator blanking function is active during phase and enable transitions. This eliminates false tripping of the over-current comparator caused by switching transients (see "RC Blanking" above).

Enable PWM. Toggling the ENABLE input turns ON and OFF the selected source and sink drivers. The corresponding pair of flyback and ground clamp diodes conduct after the drivers are disabled, resulting in fast current decay. When the device is enabled the internal current control circuitry will be active and can be used to limit the load current in a slow decay mode.

Phase PWM. Toggling the PHASE terminal selects which sink/source pair is enabled, producing a load current that varies with the duty cycle and remains continuous at all times. This can have added benefits in bidirectional brush dc servo motor applications as the transfer function between the duty cycle on the PHASE input and the average voltage applied to the motor is more linear than in the case of ENABLE PWM control (which produces a discontinuous current at low current levels).

Miscellaneous Information. An internally generated dead time prevents crossover currents that can occur when switching phase.

Thermal protection circuitry turns OFF all drivers should the junction temperature reach 165°C (typical). This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The hysteresis of the thermal shutdown circuit is approximately 15°C.

APPLICATION NOTES

Current Sensing. The actual peak load current (I_{PEAK}) will be above the calculated value of I_{TRIP} due to delays in the turn off of the drivers. The amount of overshoot can be approximated by:

$$I_{OS} \approx \frac{(V_{BB} - ((I_{TRIP} \bullet R_{LOAD}) + V_{BEMF})) \bullet t_{PWM}}{L_{LOAD}}$$

where V_{BB} is the motor supply voltage, V_{BEMF} is the back-EMF voltage of the load, R_{LOAD} and L_{LOAD} are the resistance and inductance of the load respectively, and t_{PWM} is specified in the electrical characteristics table.

To minimize current sensing inaccuracies caused by ground trace I•R drops, each current sensing resistor should have a separate return to the ground terminal of the device. For low-value sense resistors, the I•R drops in the PCB can be significant and should be taken into account. The use of sockets should be avoided as their contact resistance can cause variations in the effective value of R_{SENSE}.

Generally, larger values of R_{SENSE} reduce the aforementioned effects but can result in excessive heating and power loss in the sense resistor. The selected value of R_{SENSE} should not cause the absolute maximum voltage rating of 1.0 V, for the SENSE terminal, to be exceeded. The recommended value of R_{SENSE} is in the range of:

$$R_{SENSE} \approx \frac{0.5}{I_{TRIP}max} \pm 50\%$$

If desired, the reference input voltage can be filtered by placing a capacitor from REF_{IN} to ground. The ground return for this capacitor as well as R_2 should be independent from the high-current power-ground trace to avoid changes in REF_{IN} due to I•R drops.

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where V_F can be chosen from the electrical specification table for the given level of I_{LOAD}. The value for $R_{\theta JT}$ is given in the package thermal resistance table for the appropriate package.

The power dissipation of the batwing packages can be improved by 20 to 30% by adding a section of printed circuit board copper (typically 6 to 18 square centimeters) connected to the batwing terminals of the device.

The thermal performance in applications that run at high load currents and/or high duty cycles can be improved by adding external diodes from each output to ground in parallel with the internal diodes. Fast recovery (≤ 200 ns) diodes should be used to minimize switching losses.

The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (≥ 47 µF is recommended) placed as close to the device as is physically practical. To minimize the effect of system ground I•R drops on the logic and reference input signals the system ground should have a low-resistance return to the motor supply voltage.

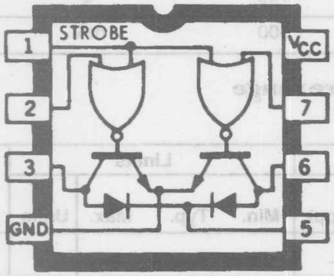
See also "Current Sensing" and "Thermal Considerations" above.

Fixed Off-Time Selection. With increasing values of t_{OFF}, switching losses will decrease, low-level load current regulation will improve, EMI will be reduced, the PWM frequency will decrease, and ripple current will increase. The value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} are chosen to be in the range of 15 to 35 µs.

5713

29307B

DUAL PERIPHERAL AND POWER DRIVER — TRANSIENT PROTECTED OUTPUTS



Dwg. No. A-9789

This "mini-DIP" dual peripheral and power driver is a bipolar monolithic integrated circuit incorporating NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, this driver will withstand at least 80 V.

The UDN5713M dual driver is ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to 600 mA.

The integral transient suppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. Similar devices with four drivers per package are the 5703 and 5706.

FEATURES

- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Stand-off Voltage of 80 V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage, V_{IN} . . . . **30 V**
Output Off-State Voltage,
V_{OFF} . . . . **80 V**
Output On-State Sink Current,
I_{ON} . . . . **600 mA**
Suppression Diode Off-State Voltage,
V_{OFF} . . . . **80 V**
Suppression Diode On-State Current,
I_{ON} . . . . **600 mA**
Power Dissipation at T_A = 25°C, P_D
Package . . . . **1.5 W***
Each Driver . . . . **0.8 W**
Operating Free-Air Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

*Derate at the rate of 12.5 mW/°C above T_A = 25°C.

Always order by complete part number, e.g., **UDN5713M**.

5713
DUAL PERIPHERAL AND POWER DRIVER

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{IN(1)}$	—	MIN	—	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	—	MIN	—	—	—	—	—	0.8	V	—
"0" Input Current at all Inputs except Strobe	$I_{IN(0)}$	—	MAX	0.4 V	30 V	—	—	-50	-100	µA	2
"0" Input Current at Strobe	$I_{IN(0)}$	—	MAX	0.4 V	30 V	—	—	-100	-200	µA	—
"1" Input Current at all Inputs except Strobe	$I_{IN(1)}$	—	MAX	30 V	0 V	—	—	—	10	µA	2
"1" Input Current at Strobe	$I_{IN(1)}$	—	MAX	30 V	0 V	—	—	—	20	µA	—
Input Clamp Voltage	V_{IK}	—	MIN	-12 mA	—	—	—	—	-1.5	V	—

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

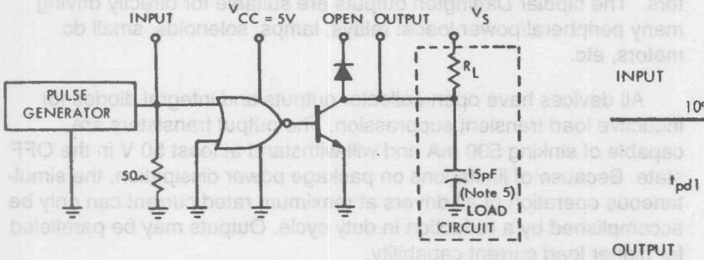
INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	t_f = 7 ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

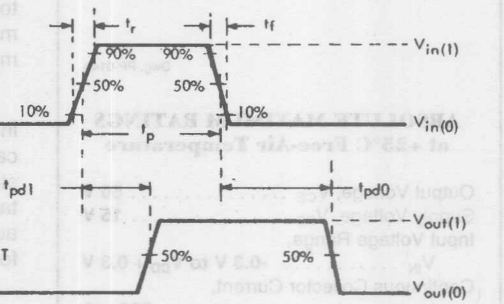
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions: Temp.	V_{CC}	Driven Input	Other Input	Output	Limits: Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	0 V	80 V	—	—	100	µA	—
			OPEN	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	0.8 V	150 mA	—	0.35	0.5	V	—
			MIN	0.8 V	0.8 V	300 mA	—	0.5	0.7	V	—
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	36	50	mA	1, 2

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_F = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-9123A

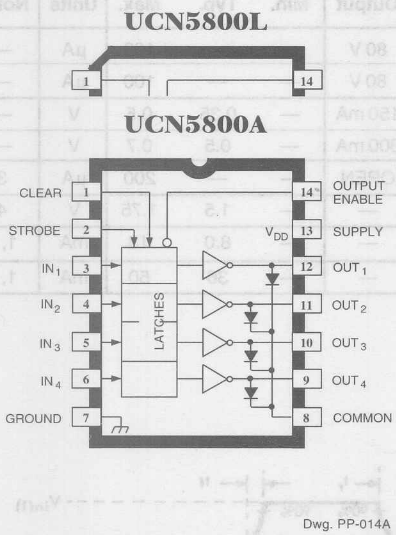


Dwg. No. A-7628C

5800 AND 5801

26180.10A*

BiMOS II LATCHED DRIVERS



Dwg. PP-014A

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . **50 V**
Supply Voltage, V_{DD} . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Collector Current,
I_C . . . . **500 mA**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Note that the UCN5800A (dual in-line package) and UCN5800L (small-outline IC package) are electrically identical and share a common pin number assignment.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5800A/L and UCN5801A/EP latched-input BiMOS ICs merge high-current, high-voltage outputs with CMOS logic. The CMOS input section consists of 4 or 8 data ('D' type) latches with associated common CLEAR, STROBE, and OUTPUT ENABLE circuitry. The power outputs are bipolar npn Darlingtons. This merged technology provides versatile, flexible interface. These BiMOS power interface ICs greatly benefit the simplification of computer or microprocessor I/O. The UCN5800A and UCN5800L each contain four latched drivers; the UCN5801A and UCN5801EP contain eight latched drivers.

The UCN5800A/L and UCN5801A/EP supersede the original BiMOS latched-input driver ICs (UCN4400A and UCN4801A). These second-generation devices are capable of much higher data input rates and will typically operate at better than 5 MHz with a 5 V logic supply. Circuit operation at 12 V affords substantial improvement over the 5 MHz figure.

The CMOS inputs are compatible with standard CMOS and NMOS circuits. TTL circuits may mandate the addition of input pull-up resistors. The bipolar Darlington outputs are suitable for directly driving many peripheral/power loads: relays, lamps, solenoids, small dc motors, etc.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

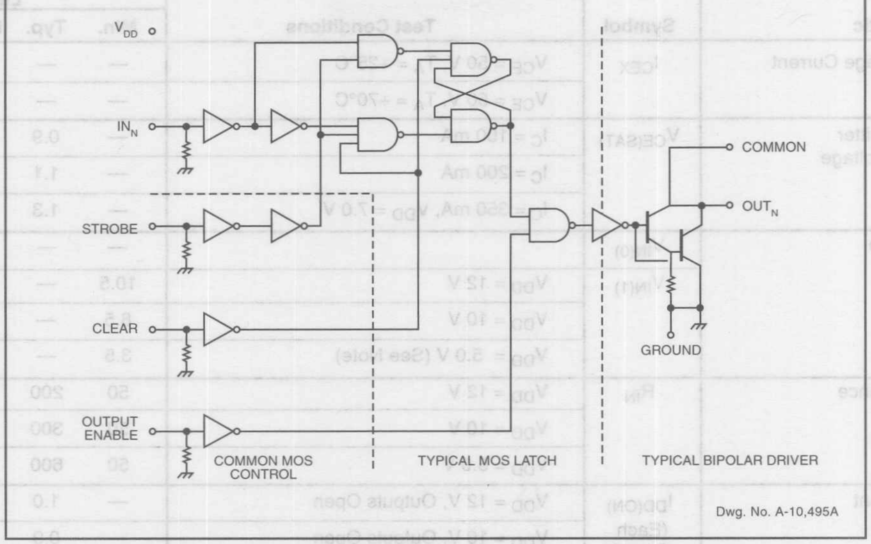
The UCN5800A is furnished in a standard 14-pin DIP; the UCN5800L in a surface-mountable SOIC; the UCN5801A in a 22-pin DIP with 0.400" (10.16 mm) row centers; the UCN5801EP in a 28-lead PLCC.

FEATURES

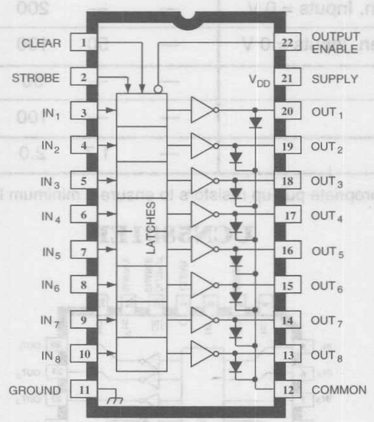
- To 4.4 MHz Data Input Rate
- High-Voltage, High-Current Outputs
- CMOS, NMOS, TTL Compatible Inputs
- Output Transient Protection
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Automotive Capable

Always order by complete part number, e.g., **UCN5801EP** .

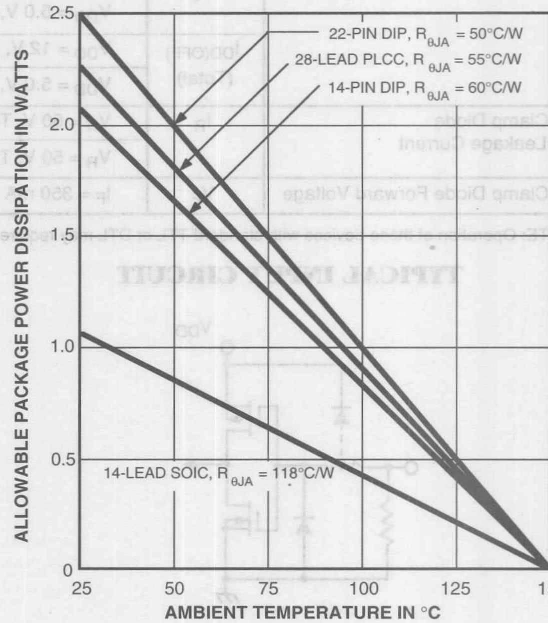
FUNCTIONAL BLOCK DIAGRAM



UCN5801A



Dwg. PP-015



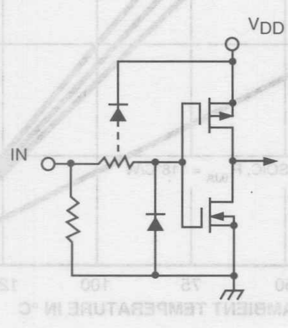
Dwg. GP-023

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	µA
		V_{CE} = 50 V, T_A = +70°C	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	µA
		V_R = 50 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

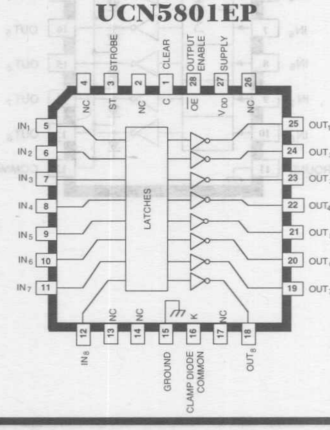
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic "1".

TYPICAL INPUT CIRCUIT

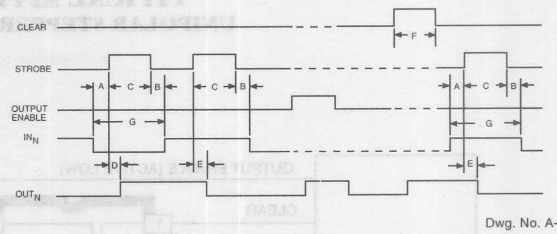


Dwg. EP-010-4A

UCN5801EP



Dwg. PP-037



Dwg. No. A-10,895A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) .... **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) .... **50 ns**

C. Minimum Strobe Pulse Width .... **125 ns**

D. Typical Time Between Strobe Activation and Output On to Off Transition .... **500 ns**

E. Minimum Time Between Strobe Activation and Output Off to On Transition .... **500 ns**

F. Minimum Clear Pulse Width .... **300 ns**

G. Minimum Data Pulse Width .... **225 ns**

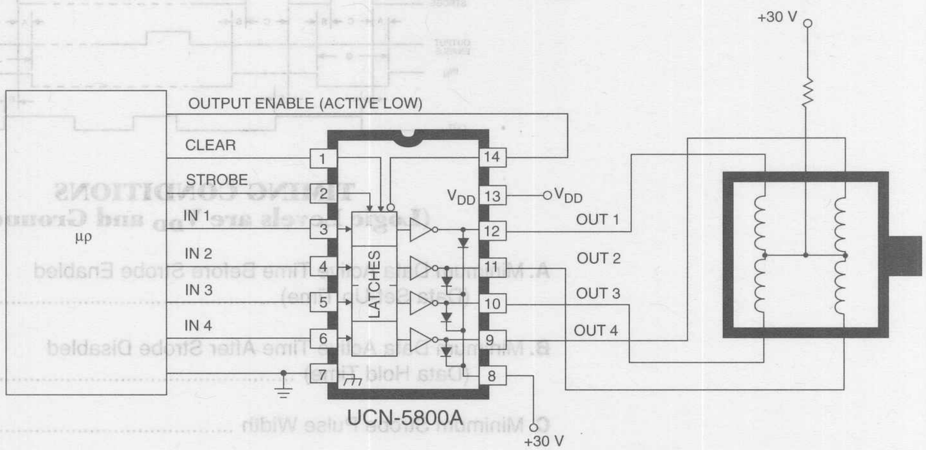
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_{IN} t-1	OUT_{IN} t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

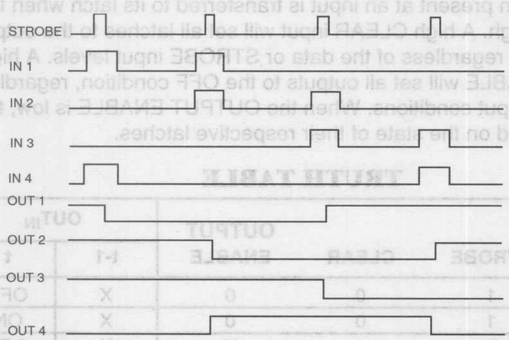
X = irrelevant.
t-1 = previous output state.
t = present output state.

TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



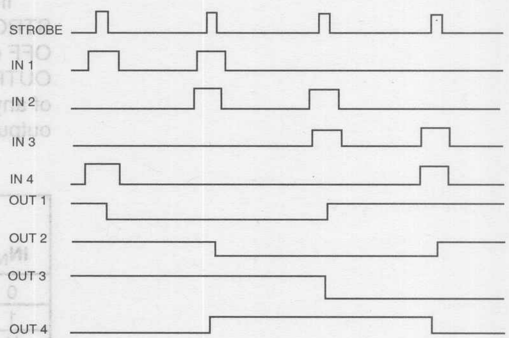
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE

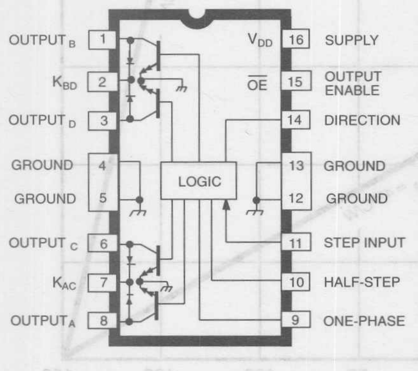


Dwg. No. A-11,447

5804

26184.12A

BiMOS II UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVER



Dwg. W-194

Combining low-power CMOS logic with high-current and high-voltage bipolar outputs, the UCN5804B BiMOS II translator/driver provides complete control and drive for a four-phase unipolar stepper-motor with continuous output current ratings to 1.25 A per phase (1.5 A startup) and 35 V.

The CMOS logic section provides the sequencing logic, DIRECTION and OUTPUT ENABLE control, and a power-ON reset function. Three stepper-motor drive formats, wave-drive (one-phase), two-phase, and half-step are externally selectable. The inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high.

The wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding inbalance in the motor. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.

The bipolar outputs are capable of sinking up to 1.5 A and withstanding 50 V in the OFF state (sustaining voltages up to 35 V). Ground clamp and flyback diodes provide protection against inductive transients. Thermal protection circuitry disables the outputs when the chip temperature is excessive.

The UCN5804B is rated for operation over the temperature range of -20°C to +85°C. It is supplied in a 16-pin dual in-line plastic batwing package with a copper lead frame and heat-sinkable tabs for improved power dissipation capabilities.

ABSOLUTE MAXIMUM RATINGS

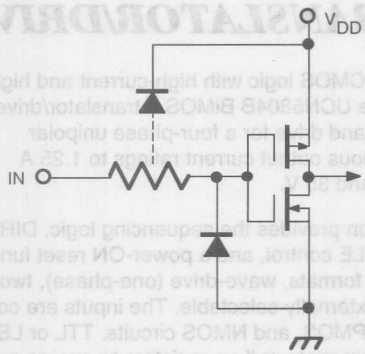
Output Voltage, V_{CE} .... **50 V**
Output Sustaining Voltage,
$V_{CE\ (sus)}$ .... **35 V**
Output Sink Current, I_{OUT} .... **1.5 A**
Logic Supply Voltage, V_{DD} .... **7.0 V**
Input Voltage, V_{IN} .... **7.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

FEATURES

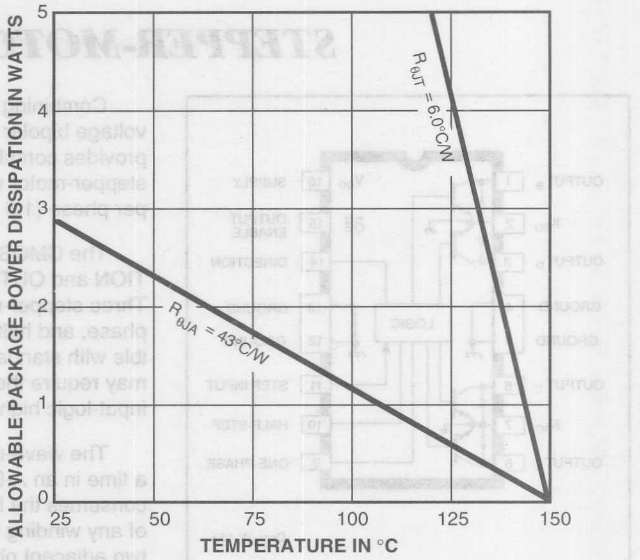
- 1.5 A Maximum Output Current
- 35 V Output Sustaining Voltage
- Wave-Drive, Two-Phase, and Half-Step Drive Formats
- Internal Clamp Diodes
- Output Enable and Direction Control
- Power-ON Reset
- Internal Thermal Shutdown Circuitry

Always order by complete part number: **UCN5804B**

TYPICAL INPUT CIRCUIT

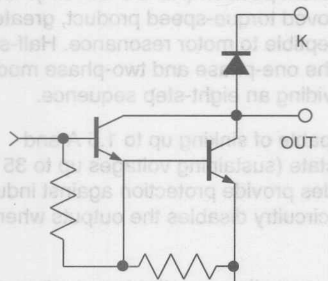


Dwg. EP-010-5



Dwg. GP-010B

TYPICAL OUTPUT DRIVER



Dwg. EP-021-4

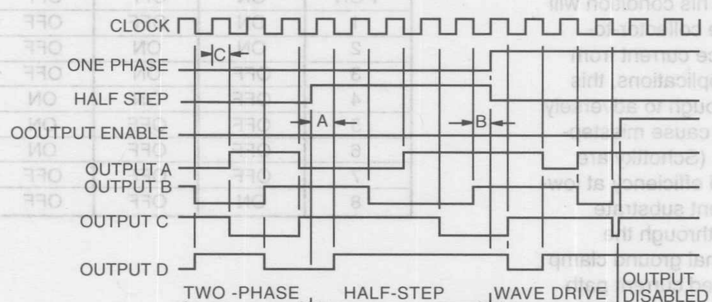
TRUTH TABLE

Drive Format	Pin 9	Pin 10
Two-Phase	L	L
One-Phase	H	L
Half-Step	L	H
Step-Inhibit	H	H

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $T_J \le$ 150°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	10	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 1.25 A, L = 3 mH	35	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 700 mA	—	1.0	1.2	V
		I_{OUT} = 1 A	—	1.1	1.4	V
		I_{OUT} = 1.25 A	—	1.2	1.5	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	10	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.25 A	—	1.5	3.0	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.5	5.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.5	-5.0	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5 V	3.5	—	5.3	V
	$V_{IN(0)}$		-0.3	—	0.8	V
Supply Current	I_{DD}	2 Outputs ON	—	20	30	mA
Turn-Off Delay	t_{ON}	50% Step Inputs to 50% Output	—	—	10	µs
Turn-On Delay	t_{OFF}	50% Step Inputs to 50% Output	—	—	10	µs
Thermal Shutdown Temperature	T_J		—	165	—	°C

TIMING CONDITIONS



Dwg. W-110A

A. Minimum Data Set Up Time .... **100 ns**
B. Minimum Data Hold Time .... **100 ns**
C. Minimum Step Input Pulse Width .... **500 ns**

APPLICATIONS INFORMATION

Internal power-ON reset (POR) circuitry resets $OUTPUT_A$ (and $OUTPUT_D$ in the two-phase drive format) to the ON state with initial application of the logic supply voltage. After reset, the circuit then steps according to the tables.

The outputs will advance one sequence position on the high-to-low transition of the STEP INPUT pulse. Logic levels on the HALF-STEP and ONE-PHASE inputs will determine the drive format (one-phase, two-phase, or half-step). The DIRECTION pin determines the rotation sequence of the outputs. Note that the STEP INPUT must be in the low state when changing the state of ONE-PHASE, HALF-STEP, or DIRECTION to prevent erroneous stepping.

All outputs are disabled (OFF) when OUTPUT ENABLE is at a logic high. If the function is not required, OUTPUT ENABLE should be tied low. In that condition, all outputs depend only on the state of the step logic.

During normal commutation of a unipolar stepper motor, mutual coupling between the motor windings can force the outputs of the UCN5804B below ground. This condition will cause forward biasing of the collector-to-substrate junction and source current from the output. For many L/R applications, this substrate current is high enough to adversely affect the logic circuitry and cause misstepping. External series diodes (Schottky are recommended for increased efficiency at low-voltage operation) will prevent substrate current from being sourced through the outputs. Alternatively, external ground clamp diodes will provide a preferred current path from ground when the outputs are pulled below ground.

Internal thermal protection circuitry disables all outputs when the junction temperature reaches approximately 165°C. The outputs are enabled again when the junction cools down to approximately 145°C.

WAVE-DRIVE SEQUENCE

Half Step = L, One Phase = H				
Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	OFF	OFF	ON	OFF
4	OFF	OFF	OFF	ON

TWO-PHASE DRIVE SEQUENCE

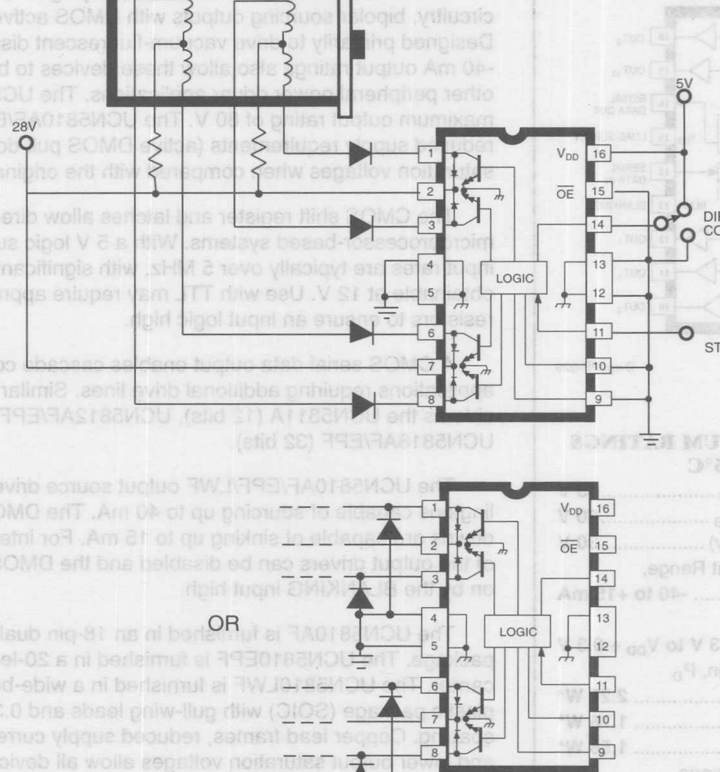
Half Step = L, One Phase = L				
Step	A	B	C	D
POR	ON	OFF	OFF	ON
1	ON	OFF	OFF	ON
2	ON	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	ON

HALF-STEP DRIVE SEQUENCE

Half Step = H, One Phase = L				
Step	A	B	C	D
POR	ON	OFF	OFF	OFF
1	ON	OFF	OFF	OFF
2	ON	ON	OFF	OFF
3	OFF	ON	OFF	OFF
4	OFF	ON	ON	OFF
5	OFF	OFF	ON	OFF
6	OFF	OFF	ON	ON
7	OFF	OFF	OFF	ON
8	ON	OFF	OFF	ON

5804
BiMOS II UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVER

TYPICAL APPLICATION
L/R Stepper-Motor Drive



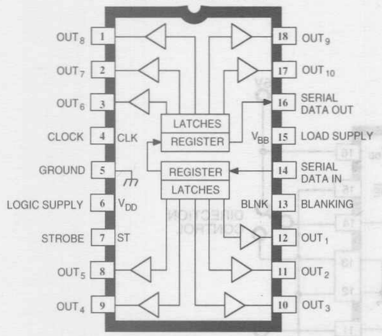
Dwg. EP-029A

5810-F

26182.24A*

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5810AF



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**

Driver Supply Voltage, V_{BB} .... **60 V**

(UCN5810LWF-1 only) .... **80 V**

Continuous Output Current Range,

I_{OUT} .... **-40 to +15 mA**

Input Voltage Range,

V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Package Power Dissipation, P_D

(UCN5810AF) .... **2.27 W***

(UCN5810EPF) .... **1.78 W***

(UCN5810LWF) .... **1.56 W***

Operating Temperature Range,

T_A .... **-20°C to +85°C**

Storage Temperature Range,

T_S .... **-55°C to +150°C**

*Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5810AF (dual in-line package) and UCN5810LWF (small-outline IC package) are electrically identical and share a common pin number assignment.

The UCN5810AF, UCN5810EPF, and UCN5810LWF combine a 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The UCN5810LWF-1 has a maximum output rating of 80 V. The UCN5810AF/EPF/LWF feature reduced supply requirements (active DMOS pull-downs) and lower saturation voltages when compared with the original UCN5810A.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, serial-data input rates are typically over 5 MHz, with significantly higher speeds obtainable at 12 V. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5811A (12 bits), UCN5812AF/EPF (20 bits) and UCN5818AF/EPF (32 bits).

The UCN5810AF/EPF/LWF output source drivers are NPN Darlingtons capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned on by the BLANKING input high.

The UCN5810AF is furnished in an 18-pin dual in-line plastic package. The UCN5810EPF is furnished in a 20-lead plastic chip carrier. The UCN5810LWF is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads and 0.300" lead row spacing. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow all devices to source 25 mA from all outputs continuously, over the entire operating temperature range. All 60 V devices (without the '-1' suffix) are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

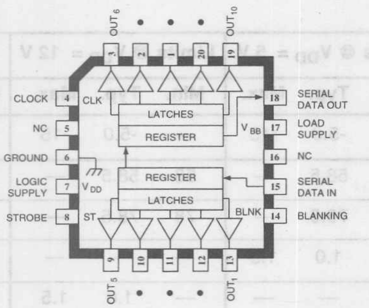
FEATURES

- High-Speed Source Drivers
- 60 V or 80 V Minimum Output Breakdown
- Improved Replacements for TL4810B
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- To 3.3 MHz Data Input Rate
- Active DMOS Pull-Downs

Always order by complete part number, e.g., **UCN5810AF**.

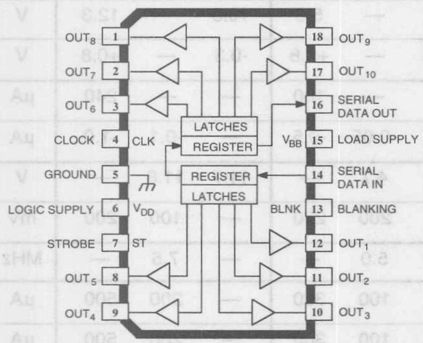
5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5810EP

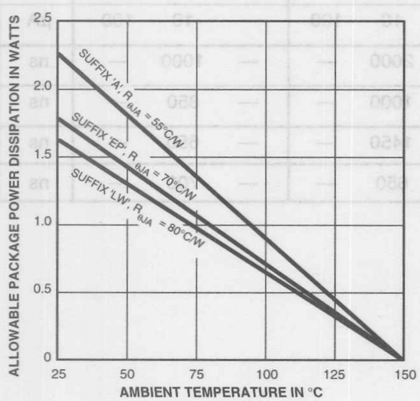


Dwg. PP-059

UCN5810LWF

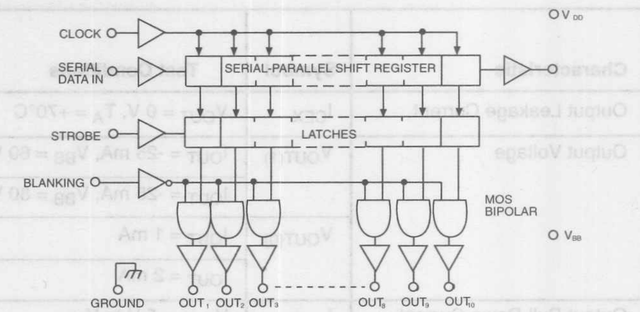


Dwg. PP-029-1

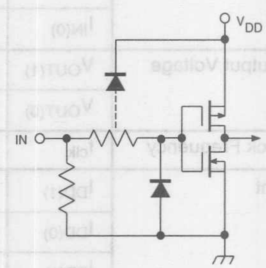


Dwg. GP-024A

FUNCTIONAL BLOCK DIAGRAM

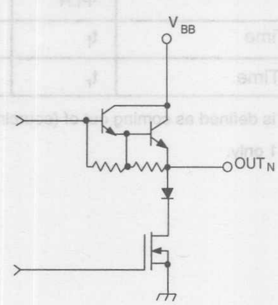


TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

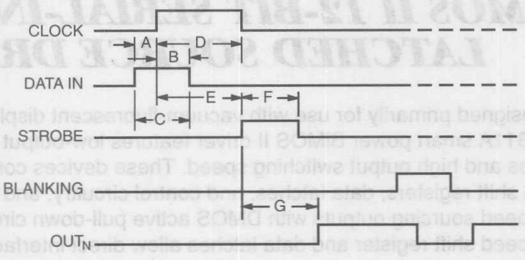
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (UCN5810AF/EPF/LWF) or 80 V (UCN5810LWF-1) unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V Min.	Typ.	Max.	Limits @ V_{DD} = 12 V Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	—	100	—	—	240	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	0.7	2.0	—	0.7	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.

* UCN5810LWF-1 only.

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. A-12,649A

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) **75ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) **75ns**

C. Minimum Data Pulse Width **150ns**

D. Minimum Clock Pulse Width **150ns**

E. Minimum Time Between Clock Activation and Strobe **300ns**

F. Minimum Strobe Pulse Width **100ns**

G. Typical Time Between Strobe Activation and Output Transition **500ns**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Blanking	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5811

26182.20A

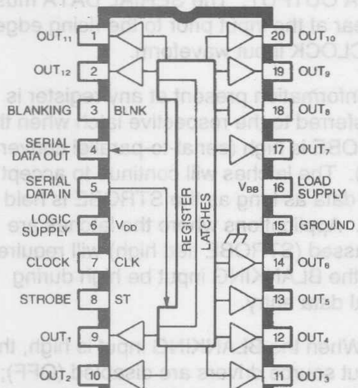
BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

Designed primarily for use with vacuum-fluorescent displays, the UCN5811A smart power BiMOS II driver features low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCN5811A features 60 V and -40 mA output ratings, allowing it to be used in many other peripheral power driver applications. It can be used as an improved replacement tor the SN75512B. The Allegro devices do not require special power-up sequencing.

The UCN5811A has been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, it will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of this device with TTL may require the use of appropriate pull-up resistors to ensure a proper input logic high.

This device is supplied in a 20-pin plastic dual in-line package. It can be operated over the ambient temperature range of -20°C to + 85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 76°C .



Dwg. W-180

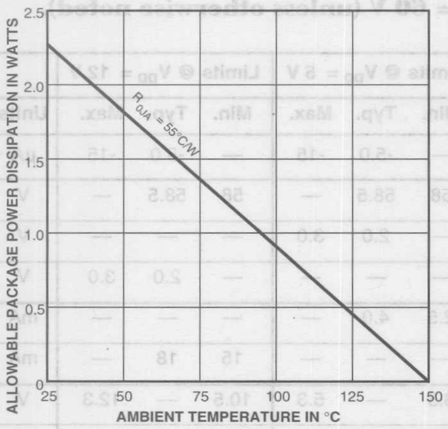
FEATURES

- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

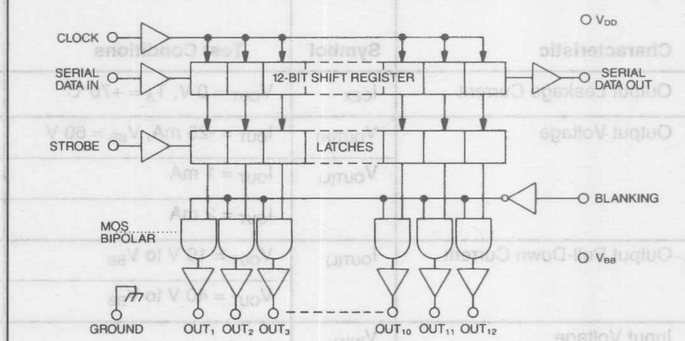
Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current,
I_{OUT} .... **-40 to +25 mA**
Input Voltage Range,
V_{IN} .... **0.3 V to V_{DD} +0.3 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Always order by complete part number: **UCN5811A**



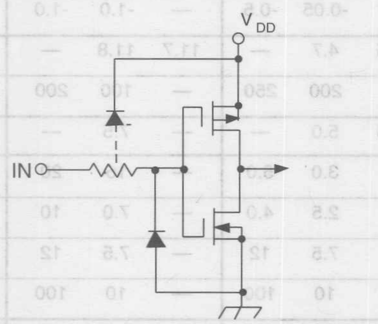
Dwg. GS-004-1

FUNCTIONAL BLOCK DIAGRAM



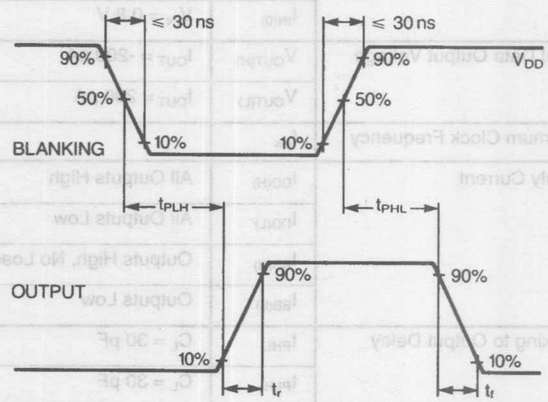
Dwg. W-181

TYPICAL INPUT CIRCUIT



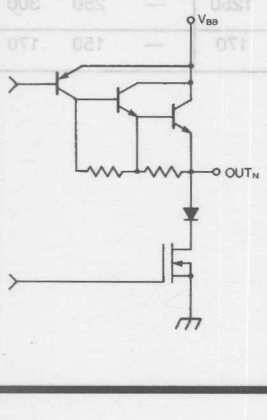
Dwg. No. A-13,035

TIMING WAVESHAPES



Dwg. W-184

TYPICAL OUTPUT DRIVER

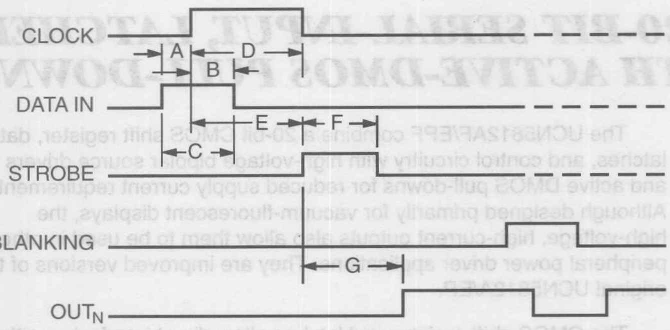


Dwg. W-182

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V Min.	Typ.	Max.	Limits @ V_{DD} = 12 V Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(H)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
	$V_{OUT(L)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(L)}$	V_{OUT} = 10 V to V_{BB}	2.5	4.0	—	—	—	—	mA
		V_{OUT} = 40 V to V_{BB}	—	—	—	15	18	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-1.0	-1.0	µA
Serial Data Output Voltage	$V_{OUT(H)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(L)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(H)}$	All Outputs High	—	3.0	5.0	—	15	20	mA
	$I_{DD(L)}$	All Outputs Low	—	2.5	4.0	—	7.0	10	mA
	$I_{BB(H)}$	Outputs High, No Load	—	7.5	12	—	7.5	12	mA
	$I_{BB(L)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF	—	300	550	—	125	150	ns
	t_{PLH}	C_L = 30 pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	C_L = 30 pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	C_L = 30 pF	—	150	170	—	150	170	ns

Negative current is defined as coming out of (sourcing) the specified device pin.



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse
(Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse
(Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and
Output Transistion .... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

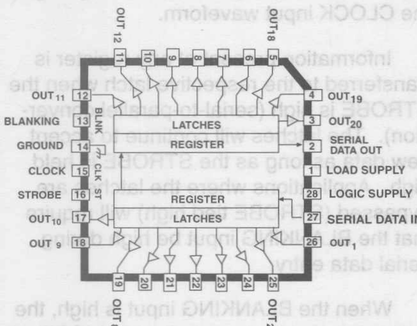
Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Blanking	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	
P_N										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

5812-F

BiMOS II 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5812EPF



Dwg. No. A-14,356

ABSOLUTE MAXIMUM RATINGS at $T_A = 25°C$

Logic Supply Voltage, V_{DD} .... **15 V**

Driver Supply Voltage, V_{BB} .... **60 V**

Continuous Output Current Range,
I_{OUT} .... **-40 to +15 mA**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Package Power Dissipation, P_D
(UCN5812AF) .... **3.12 W***
(UCN5812EPF) .... **1.92 W=**

Operating Temperature Range,
T_A .... **-20°C to +85°C**

Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Derate at rate of 25 mW/°C above T_A = +25°C

= Derate at rate of 15 mW/°C above T_A = +25°C

Caution: Allegro CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5812AF (dual in-line package) and UCN5812EPF (PLCC package) are electrically identical and share a common pin number assignment.

The UCN5812AF/EPF combine a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements. Although designed primarily for vacuum-fluorescent displays, the high-voltage, high-current outputs also allow them to be used in other peripheral power driver applications. They are improved versions of the original UCN5812A/EP.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Data input rates are typically over 5 MHz with a 5 V logic supply, and over 7.5 MHz at 12 V. Especially useful for inter-digit blanking, the BLANKING input disables the output source drives and turns on the DMOS sink drivers. Use with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5818AF/EPF (32 bits).

The output source drivers are high-voltage PNP-NPN Darlingtons with a minimum breakdown of 60 V and are capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA.

The UCN5812AF is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. For surface-mounting, the UCN5812EPF is furnished in 28-lead plastic chip carrier (quad pack) with 0.050"(1.22 mm) centers. Copper lead-frames, reduced supply current requirements and lower output saturation voltages, allow continuous operation, with all outputs sourcing 25 mA, of the UCN5812AF over the operating temperature range, and the UCN5812EPF up to +75°C. All devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

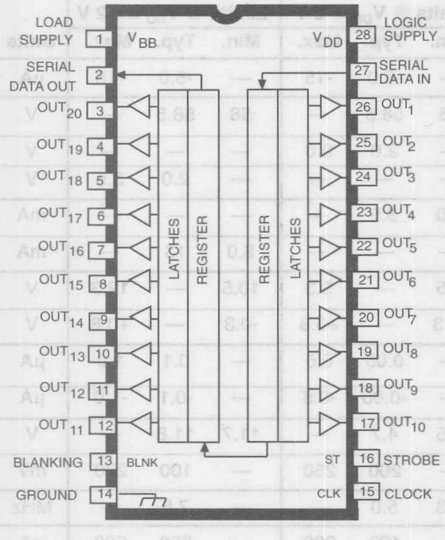
FEATURES

- High-Speed Source Drivers
- 60 V Source Outputs
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- Active DMOS Pull-Downs
- Reduced Supply Current Requirements
- Improved Replacement for TL5812

Always order by complete part number, e.g., UCN5812AF

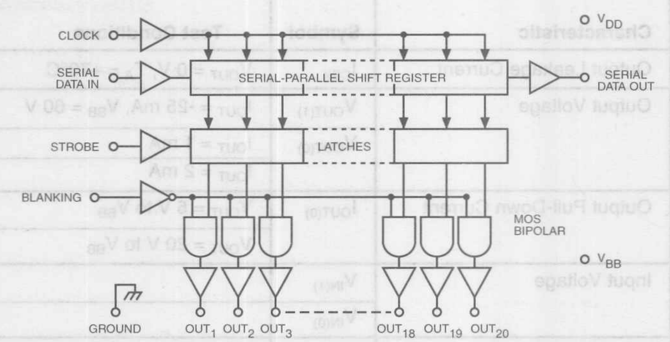
5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5812AF

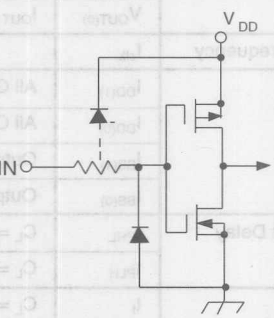


Dwg. No. A-12,270

FUNCTIONAL BLOCK DIAGRAM

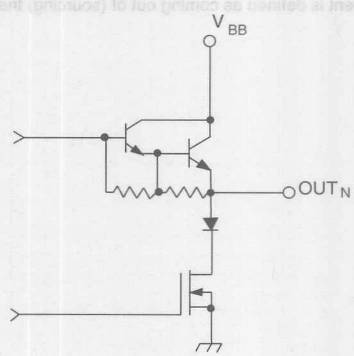


TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



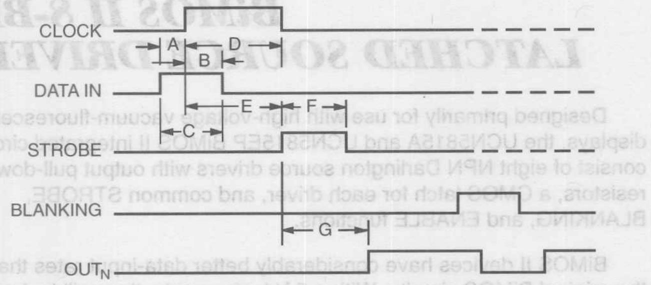
Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	4.0	—	1.5	4.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.

5812-F
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

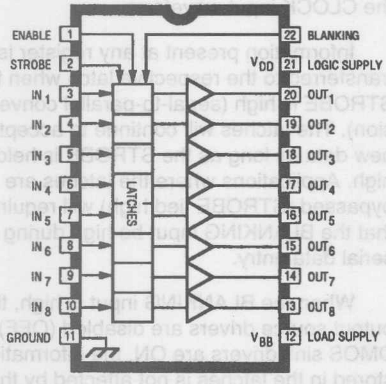
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Blanking	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

BiMOS II 8-BIT LATCHED SOURCE DRIVERS

UCN5815A



Dwg. No. A-10,987

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} .... **60 V**

Logic Supply Voltage Range,
V_{DD} .... **4.5 V to 15 V**

Load Supply Voltage Range,
V_{BB} .... **5.0 V to 60 V**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
I_{OUT} .... **-40 mA**

Package Power Dissipation, P_D
(UCN5815A) .... **2.5 W***
(UCN5815EP) .... **2.27 W***

Operating Temperature Range,
T_A .... **-20°C to +85°C**

Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with high-voltage vacuum-fluorescent displays, the UCN5815A and UCN5815EP BiMOS II integrated circuits consist of eight NPN Darlington source drivers with output pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

BiMOS II devices have considerably better data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs cause minimum loading and are compatible with standard CMOS and NMOS logic commonly found in microprocessor designs. TTL circuits may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures in excess of 75°C. To simplify printed wiring board layout, output connections are opposite the inputs. A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN5815A/EP with the UCN5810AF/EPF/LWF, UCN5812AF/EPF, or UCN5818AF/EPF serial-to-parallel latched drivers.

Suffix 'A' devices are furnished in a standard 22-pin plastic DIP; suffix 'EP' indicates a 28-lead PLCC.

FEATURES

- 4.4 MHz Minimum Date-Input Rate
- High-Voltage Source Outputs
- CMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range

Always order by complete part number:

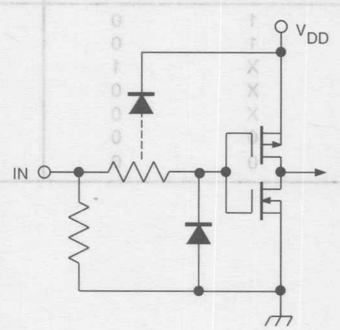
Part Number	Package
UCN5815A	22-Pin DIP
UCN5815EP	28-Lead PLCC

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V and 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		Units
			Min.	Max.	
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = -25 mA, V_{BB} = 60 V	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

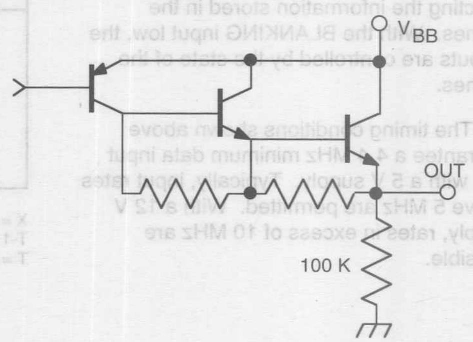
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT



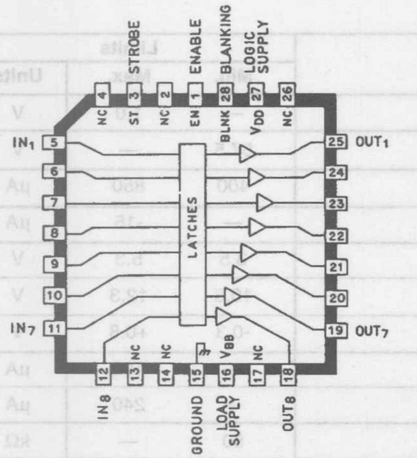
Dwg. No. EP-010-4A

TYPICAL OUTPUT DRIVER

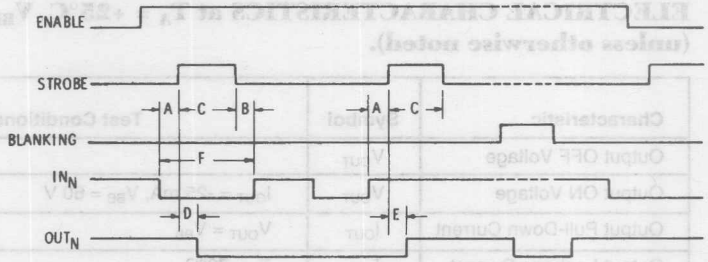


Dwg. No. EP-021-3

UCN5815EP



Dwg. No. A-14,357



Dwg. No. A-10,991

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz minimum data input rate with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output ON to OFF Transition . . . . . **5.0 μs**

E. Typical Time Between Strobe Activation and Output OFF to ON Transition . . . . . **500 ns**

F. Minimum Data Pulse Width . . . . . **225 ns**

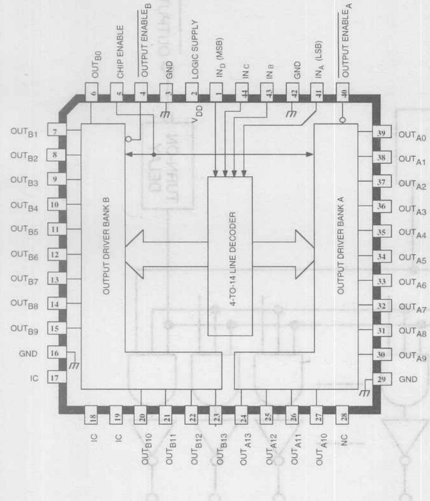
TRUTH TABLE

INPUTS				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

5817

ADDRESSABLE 28-LINE DECODER/DRIVER



Dwg. PP-050

Intended for use in ink-jet printer applications, the A5817SEP addressable 28-line decoder/driver combines low-power CMOS inputs and logic with 28 high-current, high-voltage bipolar outputs. A 4-to-14 line decoder determines the selected output driver (n) in each 14-driver bank. Two independent output enable inputs (active low) then provide the final decoding to activate 1- or 2-of-28 outputs (OUT_{An} and/or OUT_{Bn}). Special internal circuitry is programmed at the time of manufacture to adjust the output pulse timing and thereby the energy the device delivers to the ink-jet print head.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic. Use with TTL or DTL circuits may require appropriate pull-up resistors to ensure an input logic high. The internal CMOS logic operates from a 5 V supply. A CHIP ENABLE function is provided to lock out the drivers during system power up. The 28 bipolar power outputs are open-collector 30 V Darlington drivers capable of sinking 500 mA at ambient temperatures up to 85°C.

The A5817SEP is furnished in a 44-lead plastic chip carrier (quad pack) for minimum-area, surface-mount applications.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{CE} .... **30 V**
Logic Supply Voltage, V_{DD} .... **7.0 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Output Current, I_C .... **600 mA**
Package Power Dissipation, P_D ..... **2.50 W***
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Derate linearly to 0 W at T_J = 150°C.

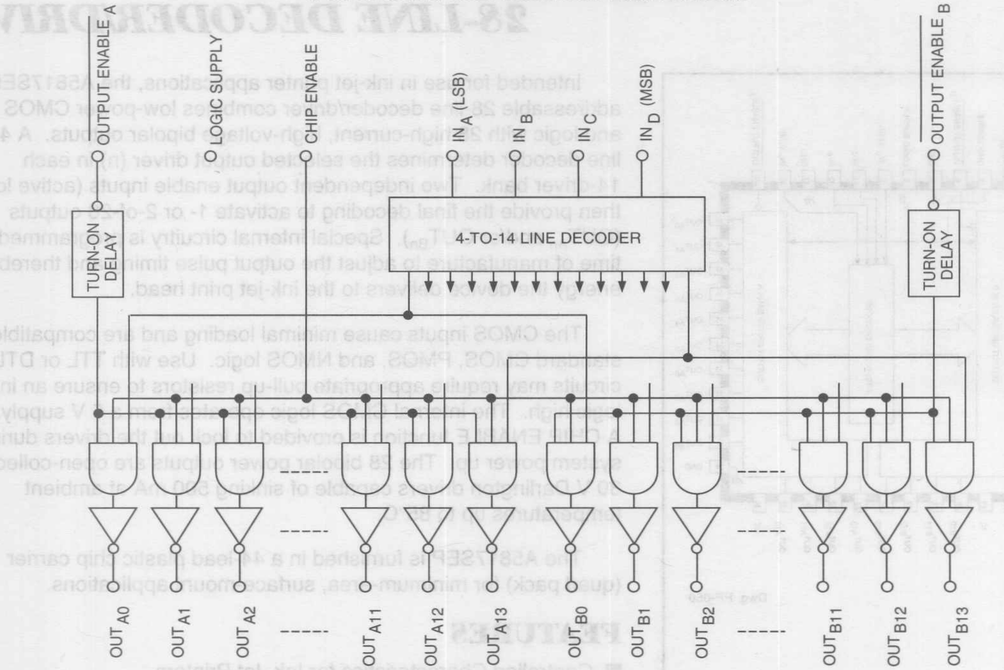
Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FEATURES

- Controlled Characteristics for Ink-Jet Printers
- Addressable Data Entry
- 30 V Minimum $V_{(BR)CEX}$
- CMOS, PMOS, NMOS Compatible Inputs
- Low-Power CMOS Logic

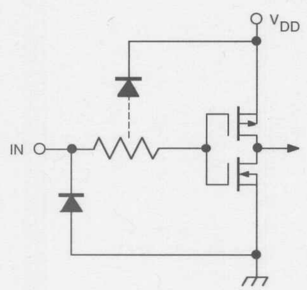
Always order by complete part number: **A5817SEP**.

FUNCTIONAL BLOCK DIAGRAM



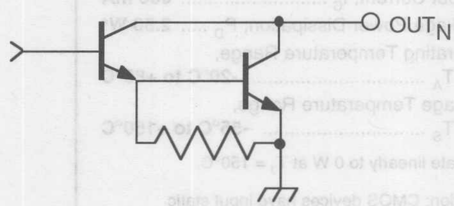
Dwg. FP-032

TYPICAL INPUT CIRCUIT



Dwg. EP-010-1

TYPICAL OUTPUT DRIVER

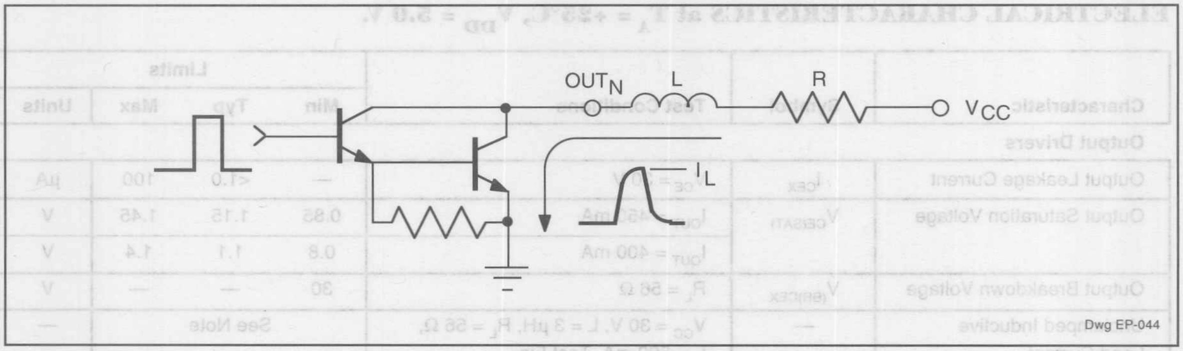


Dwg. EP-021-7

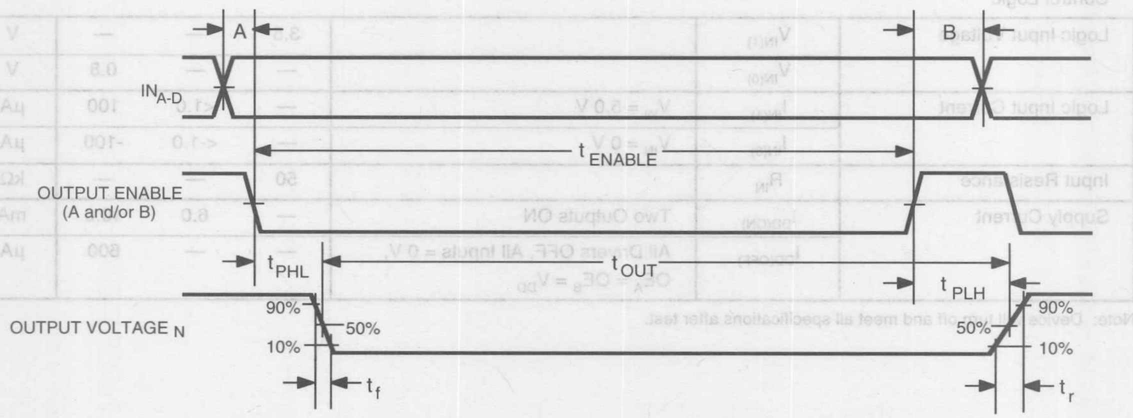
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V.

Characteristic	Symbol	Test Conditions	Limits Min	Limits Typ	Limits Max	Units
Output Drivers						
Output Leakage Current	I_{CEX}	V_{CE} = 30 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 450 mA	0.85	1.15	1.45	V
		I_{OUT} = 400 mA	0.8	1.1	1.4	V
Output Breakdown Voltage	$V_{(BR)CEX}$	R_L = 56 Ω	30	—	—	V
Unclamped Inductive Load Current	—	V_{CC} = 30 V, L = 3 µH, R_L = 56 Ω, I_L = 500 mA, Test Fig.		See Note		—
Turn-On Time	t_{PHL}	V_{CC} = 21 V, R_L = 39 Ω	125	225	475	ns
Fall Time	t_f	V_{CC} = 21 V, R_L = 39 Ω	—	20	—	ns
Turn-Off Time	t_{PLH}	V_{CC} = 21 V, R_L = 39 Ω	175	250	400	ns
Rise Time	t_r	V_{CC} = 21 V, R_L = 39 Ω	—	50	—	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		3.5	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	<1.0	100	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-1.0	-100	µA
Input Resistance	R_{IN}		50	—	—	kΩ
Supply Current	$I_{DD(ON)}$	Two Outputs ON	—	6.0	10.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, $OE_A = OE_B = V_{DD}$	—	—	600	µA

Note: Device will turn off and meet all specifications after test.



UNCLAMPED INDUCTIVE LOAD CURRENT TEST FIGURE



Dwg. WP-017

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Output Enable (Data Set-Up Time) .... 150 ns
B. Minimum Data Hold Time After Output Enable (Data Hold Time) .... 250 ns

5817
ADDRESSABLE 28-LINE DECODER/DRIVER

APPLICATIONS INFORMATION

This device is intended specifically for, although certainly not limited to, driving ink-jet print heads. In this application, a certain minimum energy (a function of load voltage and output pulse duration) is required for proper operation, while excessive energy will degrade the life of the print head. The output pulse duration (t_{OUT}) is equal to $t_{ENABLE} + t_{PLH} - t_{PHL}$, where t_{PHL} is adjusted during manufacture to compensate for variations in the output saturation voltage ($V_{CE(SAT)}$).

For the A5817SEP, the relationship between t_{OUT} and t_{ENABLE} at $T_A = 25°C$ is:

$$t_{OUT} = t_{ENABLE} + ([V_{CE(SAT)}\ (act) - V_{CE(SAT)}\ (typ)] \times 330\ ns) + 25\ ns \pm 110\ ns.$$

For most applications, this will result in a driver contribution to energy error of less than ±4%.

A logic low on the CHIP ENABLE input will prevent the drivers from turning ON, regardless of the state of other inputs or the logic supply voltage. The CHIP ENABLE input has a slow response time and should not be used as a high-speed control line. For proper operation, all ground terminals should be connected to a common ground on the printed wiring board. The IC (Internal Connection) terminals are used to program the turn-on time of the device and **MUST** be left electrically unconnected (floating) for proper operation.

DECODER TRUTH TABLE

IN_D (MSB)	INC	INB	IN_A (LSB)	N
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	ALL OFF
1	1	1	1	ALL OFF

Depending on the four address inputs, the 4-to-14 line decoder selects one driver from each of the 14 output A and B banks of sink drivers according to the Decoder Truth Table. The state of the selected outputs is determined by the OUTPUT ENABLE inputs as shown in the Enable Truth Table.

ENABLE TRUTH TABLE

CHIP ENABLE	OUTPUT $ENABLE_A$	OUTPUT $ENABLE_B$	OUTPUTS (OFF unless otherwise specified. For the value of N see the Decoder Truth Table)
0	X	X	ALL OFF
1	1	1	ALL OFF
1	0	1	OUT_{AN} ON
1	1	0	OUT_{BN} ON
1	0	0	OUT_{AN} ON, OUT_{BN} ON

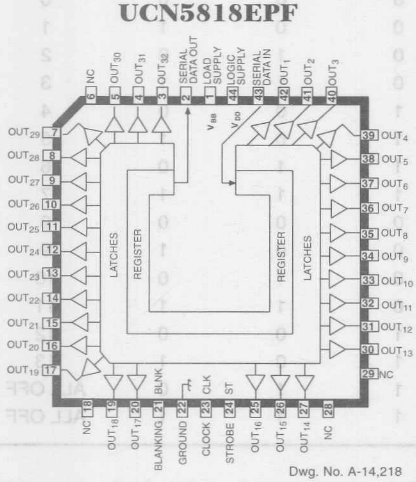
X = Irrelevant

5818-F

26182.28B

BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5818EPF



Dwg. No. A-14,218

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current,
I_{OUT} .... **-40 to +15 mA**
Input Voltage Range,
V_{IN} .... **-30 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCN5818AF) .... **3.5 W***
(UCN5818EPF) .... **2.5 W†**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Derate at rate of 28 mW/°C above T_A = +25°C
† Derate at rate of 20 mW/°C above T_A = +25°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with vacuum-fluorescent displays, the UCN5818AF and UCN5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interfacing with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and -40 mA output ratings, allowing them to be used in many other peripheral power driver applications.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of -20°C to +85°C. The UCN5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirement, and low output saturation voltage permits operation with minimum junction temperature rise. The 'A' package allows all 32 outputs to be operated at -25 mA continuously over the operating temperature range.

For high-density packaging applications, the UCN5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface mounting on solder lands with 0.050" (1.27 mm) centers. The PLCC allows -25 mA continuous operation of all outputs simultaneously at ambient temperatures to 60°C. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5812AF/EPF (20 bits).

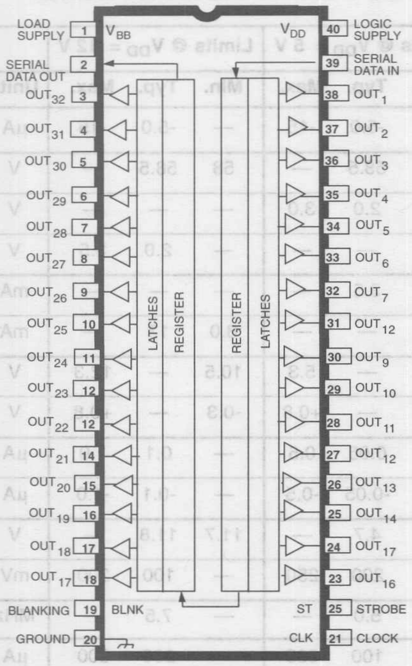
FEATURES

- 60 V Source Outputs
- High-Speed Source Drivers
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Active DMOS Pull-Downs
- Low-Power CMOS Logic and Latches
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

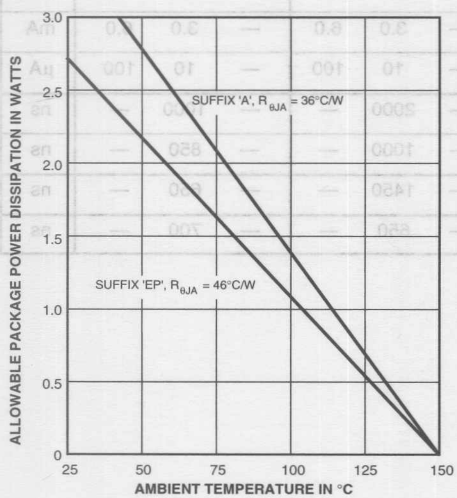
Always order by complete part number, e.g., UCN5818EPF.

5818-F
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCN5818AF

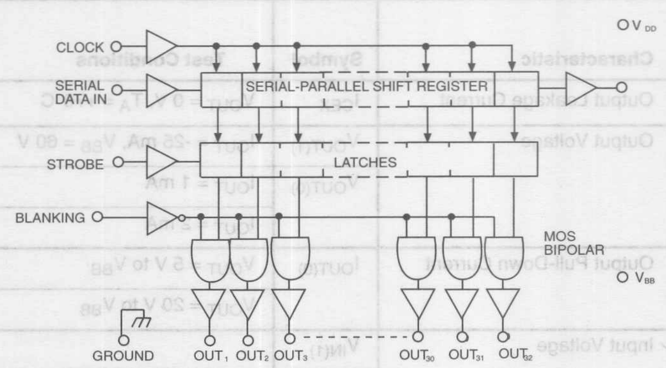


Dwg. No. A-12,269A

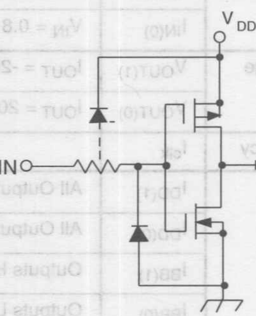


Dwg. GP-025A

FUNCTIONAL BLOCK DIAGRAM

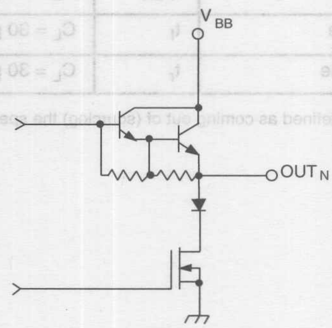


TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



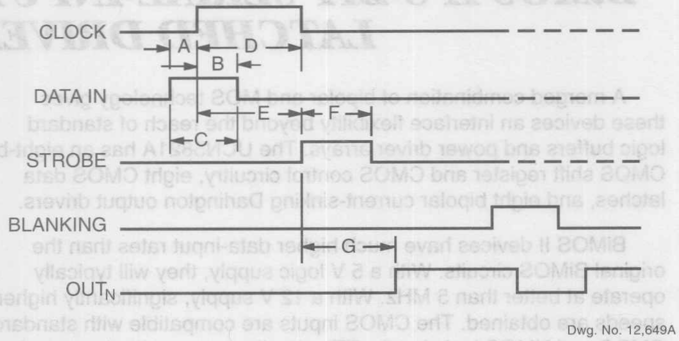
Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{BB} = 60 V unless otherwise noted.

			Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.

5818-F
32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. No. 12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**
C. Minimum Data Pulse Width .... **150 ns**
D. Minimum Clock Pulse Width .... **150 ns**
E. Minimum Time Between Clock Activation and Strobe .... **300 ns**
F. Minimum Strobe Pulse Width .... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

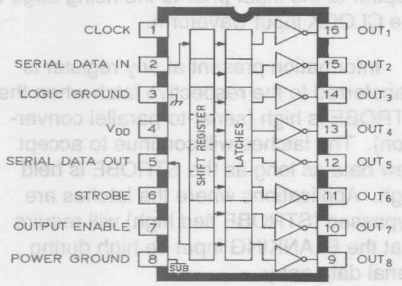
Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5821

26185.12A

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVER



Dwg. No. PP-026

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The UCN5821A has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

FEATURES

- To 3.3 MHz Data Input Rate
- CMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- Automotive Capable

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT} .... **50 V**

Logic Supply Voltage, V_{DD} .... **15 V**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
I_{OUT} .... **500 mA**

Package Power Dissipation,
P_D .... **2.08 W***

Operating Temperature Range,
T_A .... **-20°C to +85°C**

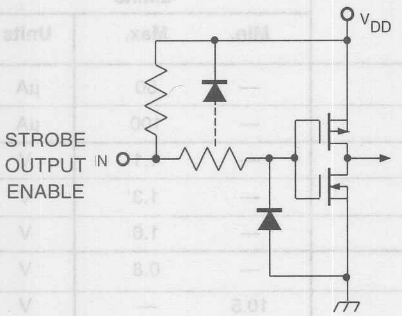
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

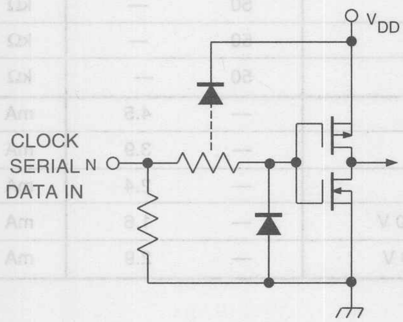
Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number: **UCN5821A**.

TYPICAL INPUT CIRCUITS

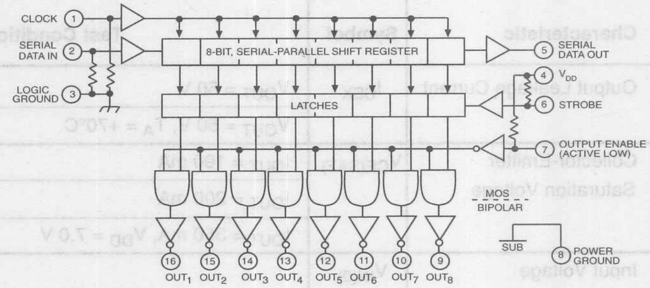


Dwg. No. EP-010-3



Dwg. No. EP-010-4

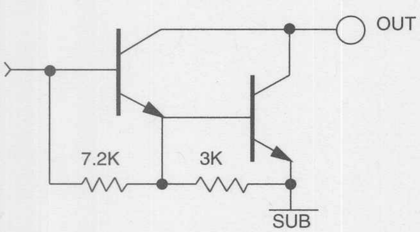
FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FP-013

Number of Outputs ON (I_{OUT} = 200 mA, V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of 25°C	40°C	50°C	60°C	70°C
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

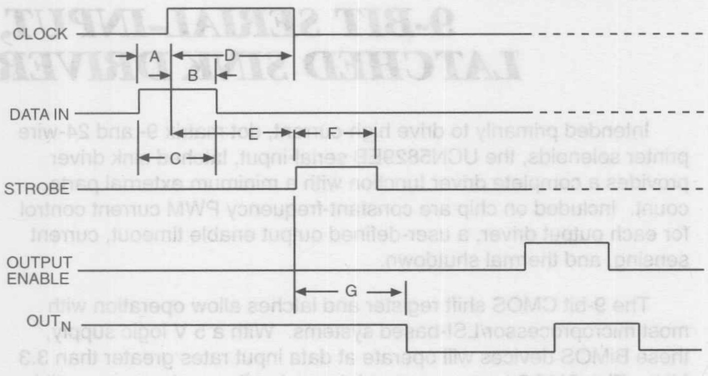
TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	50	µA
		V_{OUT} = 50 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	—	1.1	V
		I_{OUT} = 200 mA	—	1.3	V
		I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12 V	—	4.5	mA
		One Driver ON, V_{DD} = 10 V	—	3.9	mA
		One Driver ON, V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{DD} = 5.0 V, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
		V_{DD} = 12 V, All Drivers OFF, All Inputs = 0 V	—	2.9	mA



Dwg. No. A-12,627

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

TIMING CONDITIONS

(V_{DD} = 5.0 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **30 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

TRUTH TABLE

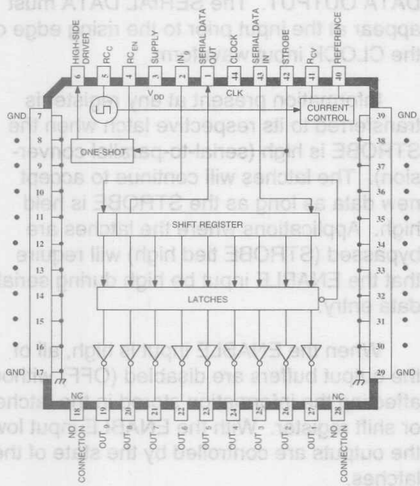
Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_8	Output Enable	Output Contents I_1	I_2	I_3	...	I_8
H	↑	H	R_1	R_2	....	R_7	R_7												
L	↑	L	R_1	R_2	....	R_7	R_7												
X	↓	R_1	R_2	R_3	....	R_8	R_8												
		X	X	X	....	X	X	L	R_1	R_2	R_3	....	R_8						
		P_1	P_2	P_3	....	P_8	P_8	H	P_1	P_2	P_3	....	P_8	L	P_1	P_2	P_3	....	P_8
									X	X	X	....	X	H	H	H	H	....	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5829

26185.50

9-BIT SERIAL-INPUT, LATCHED SINK DRIVER



Dwg. PP-028A

ABSOLUTE MAXIMUM RATINGS

Output Current Voltage, V_{OUT} .... **50 V**

Output Current, $I_{OUT(S)}$

(Continuous) .... **1.6 A**

(Peak) .... **1.8 A**

Logic Supply Voltage, V_{DD} .... **7.0 V**

Input Voltage Range,

V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Package Power Dissipation,

P_D .... **See Graph**

Operating Temperature Range,

T_A .... **-20°C to +85°C**

Junction Temperature, T_J .... **+150°C***

Storage Temperature Range,

T_S .... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Caution: This CMOS device has input static protection but is susceptible to damage when exposed to extremely high static electrical charges.

Intended primarily to drive high-current, dot matrix 9- and 24-wire printer solenoids, the UCN5829EB serial-input, latched sink driver provides a complete driver function with a minimum external parts count. Included on chip are constant-frequency PWM current control for each output driver, a user-defined output enable timeout, current sensing, and thermal shutdown.

The 9-bit CMOS shift register and latches allow operation with most microprocessor/LSI-based systems. With a 5 V logic supply, these BiMOS devices will operate at data input rates greater than 3.3 MHz. The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, NMOS, and TTL circuits. A CMOS serial data output allows cascade connections in applications requiring additional drive lines as required for 24-wire printheads.

The device features nine open-collector Darlington drivers, each rated at 50 V and 1.6 A. Current-control for each output is provided by an internal current-sensing resistor and a constant-frequency chopper circuit. An external high-side driver can be used to optimize print head performance. It is enabled by an on-chip driver during the output enable timeout. Internal logic sequencing prevents false output operation during power up. Other high-current devices for driving dot matrix printheads are the UDN2961B/W and UDN2962W.

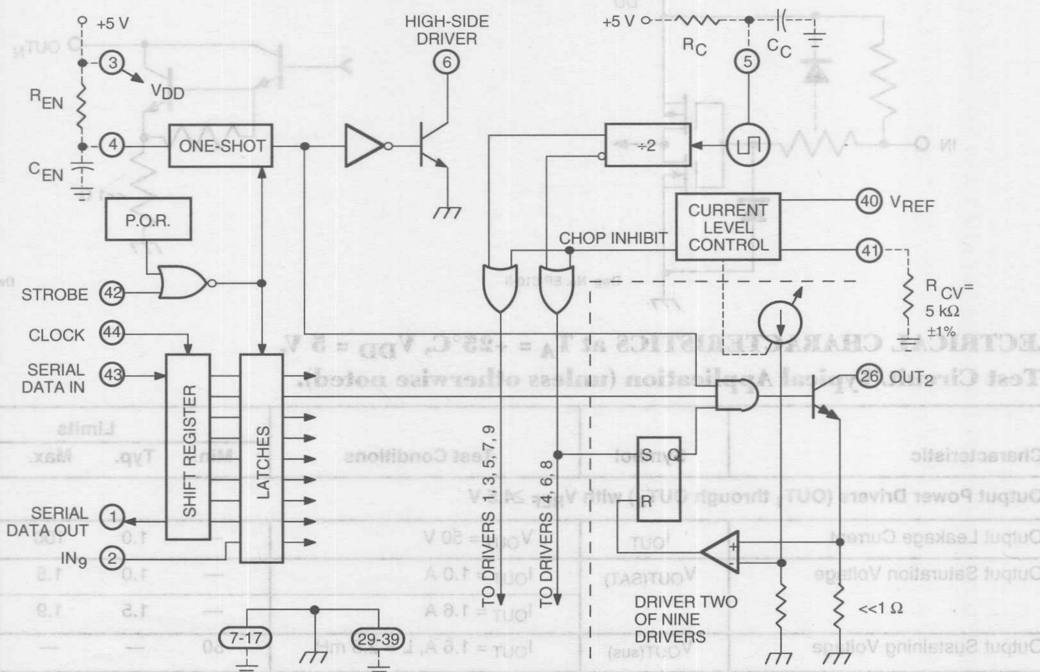
The UCN5829EB is supplied in a 44-lead power PLCC. Its batwing construction provides for maximum package power dissipation in a minimum-area, surface-mountable package.

FEATURES

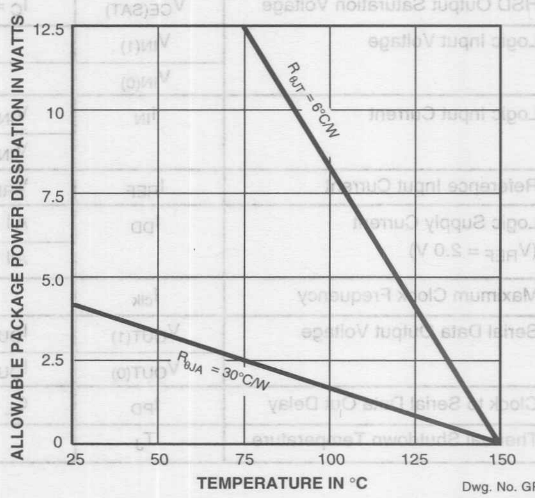
- 1.6 A Continuous Output Current
- 50 V Minimum Sustaining Voltage
- Internal Current Sensing
- Constant-Frequency PWM Current Control
- Control for External High-Side Driver
- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic & Latches
- Internal Pull-Ups for TTL Compatibility
- User-Defined Output Enable Timeout
- Internal Thermal Shutdown Circuitry

Always order by complete part number: UCN5829EB .

FUNCTIONAL BLOCK DIAGRAM

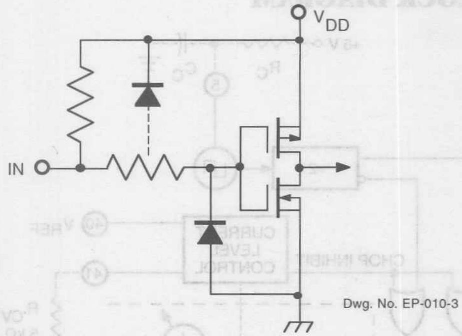


Dwg. No. FP-015A

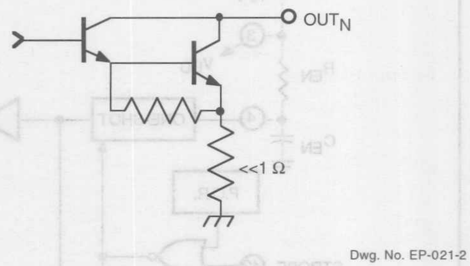


Dwg. No. GP-020B

TYPICAL INPUT CIRCUITS



TYPICAL OUTPUT DRIVER



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Power Drivers (OUT_1 through OUT_9) with V_{REF} ≥4.5 V						
Output Leakage Current	I_{OUT}	V_{OUT} = 50 V	—	1.0	100	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 1.0 A	—	1.0	1.5	V
		I_{OUT} = 1.6 A	—	1.5	1.9	V
Output Sustaining Voltage	$V_{OUT(sus)}$	I_{OUT} = 1.6 A, L = 2.5 mH	50	—	—	V
Control Logic						
HSD Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 mA	—	0.5	1.0	V
Logic Input Voltage	$V_{IN(1)}$		3.5	—	5.3	V
	$V_{IN(0)}$		-0.3	—	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 5.0 V	—	—	1.0	µA
		V_{IN} = 0.8 V	—	-90	-180	µA
Reference Input Current	I_{REF}	V_{REF} = 3.0 V	—	500	900	µA
Logic Supply Current (V_{REF} = 2.0 V)	I_{DD}	All Drivers OFF	—	15	25	mA
		All Drivers ON, No Load	—	55	75	mA
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	MHz
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	250	—	mV
Clock to Serial Data Out Delay	t_{PD}	C_L = 30 pF	—	—	300	ns
Thermal Shutdown Temperature	T_J		—	165	—	°C

Continued next page...

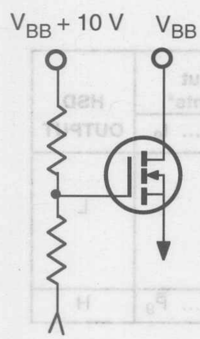
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V, in Test Circuit/Typical Application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Chopping Characteristics ($T_J = +25°C$ to $+150°C$) with Fast Clamp Diodes						
Enable Timeout	t_{EN}	$R_{EN} = 20\ k\Omega$, $C_{EN} = 0.01\ \mu F$	190	200	210	µs
Chopping Frequency	f_{ch}	$R_C = 20\ k\Omega$, $C_C = 250$ pF	90	100	110	kHz
Duty Cycle Range	dc	$t_{on} / t_{on} + t_{off}$	15	—	< 50	%
Chop Current Level	I_{TRIP}	$V_{REF} = 2.0$ V, $f_{ch} < 100$ kHz	0.9	1.0	1.1	A
		$V_{REF} = 2.8$ V, $f_{ch} < 100$ kHz	1.26	1.4	1.54	A
Output Current Control Range	V_{REF}		1.0	—	3.2	V
	I_{TRIP}		0.5	—	1.6	A
Delay	t_d	I_{TRIP} to $I_{OUT(P)}$, $T_A = +25°C$	—	300	500	ns
Chop Inhibit Voltage Range	V_{REF}		4.5	—	$V_{DD} + 0.3$	V

Negative current is defined as coming out of (sourcing) the specified device terminal.

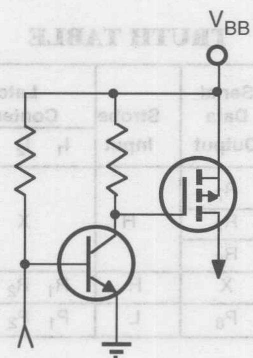
EXTERNAL HIGH-SIDE DRIVERS

NMOS



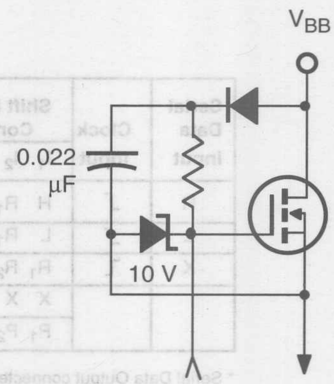
Dwg. No. EP-027

PMOS



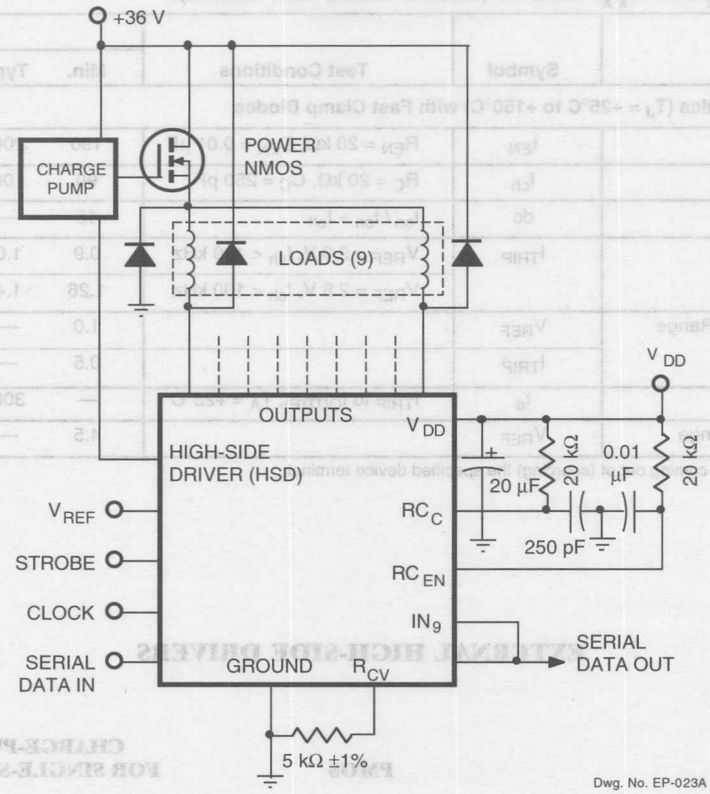
Dwg. No. EP-028

CHARGE-PUMP CIRCUITRY FOR SINGLE-SUPPLY OPERATION



Dwg. No. EP-026

TEST CIRCUIT AND TYPICAL APPLICATION



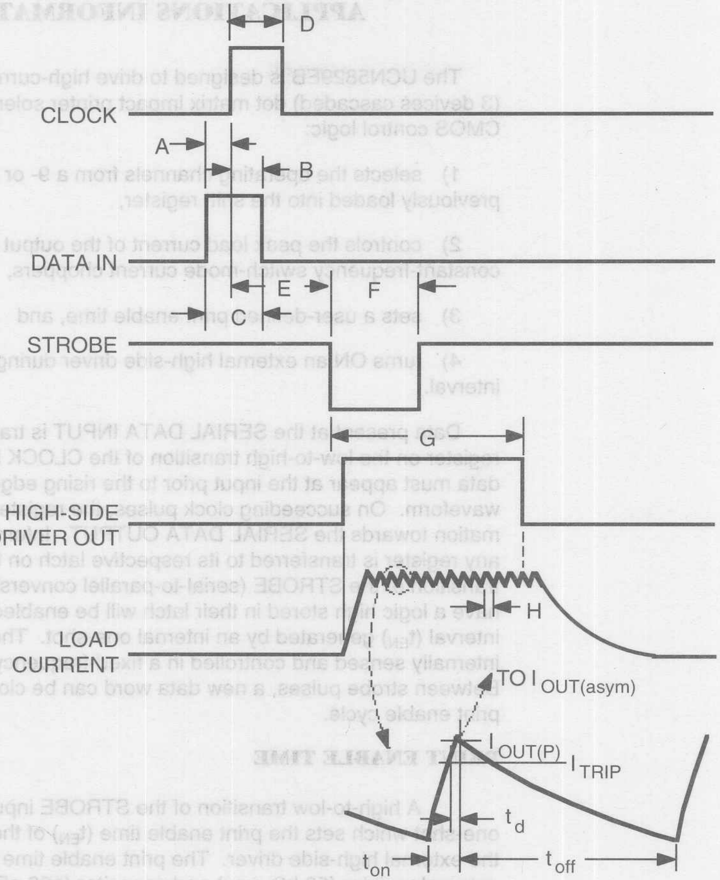
Dwg. No. EP-023A

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents* I_1 I_2 … I_9	Serial Data Output	Strobe Input	Latch Contents* I_1 I_2 … I_9	Output Contents* I_1 I_2 … I_9	HSD OUTPUT
H	$\uparrow$	H R_1 … R_8	R_7				
L	$\uparrow$	L R_1 … R_8	R_7	H	X	H	L
X	$\downarrow$	R_1 R_2 … R_9	R_8				
		X X … X	X	H	R_1 R_2 … R_9		
		P_1 P_2 … P_9	P_8	L	P_1 P_2 … P_9	$\bar{P}_1$ $\bar{P}_2$ … $\bar{P}_9$	H

* Serial Data Output connected to Input$_9$.

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State



Dwg. No. WP-011A

TIMING CONDITIONS

T_A = +25°C, Logic Levels are V_{DD} and Ground

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . **75 ns**

C. Minimum Data Pulse Width . . . . **250 ns**

D. Minimum Clock Pulse Width . . . . **250 ns**

E. Minimum Time Between Clock Activation and Strobe . . . . **500 ns**

F. Minimum Strobe Pulse Width . . . . **500 ns**

G. Enable Timeout, t_{EN} . . . . **R_{EN} C_{EN}**

H. Chop Period*, t_{on} + t_{off} . . . . **2 R_C C_C**

* Chopping is disabled if V_{REF} is greater than 4.5 V.

APPLICATIONS INFORMATION

The UCN5829EB is designed to drive high-current, 9- or 24-wire (3 devices cascaded) dot matrix impact printer solenoids. The internal CMOS control logic:

1) selects the operating channels from a 9- or 24-bit word previously loaded into the shift register,

2) controls the peak load current of the output drivers via nine constant-frequency switch-mode current choppers,

3) sets a user-defined print enable time, and

4) turns ON an external high-side driver during the print enable interval.

Data present at the SERIAL DATA INPUT is transferred to the shift register on the low-to-high transition of the CLOCK input pulse. The data must appear at the input prior to the rising edge of the clock input waveform. On succeeding clock pulses, the registers shift data information towards the SERIAL DATA OUTPUT. Information present at any register is transferred to its respective latch on the high-to-low transition of the STROBE (serial-to-parallel conversion). Drivers that have a logic high stored in their latch will be enabled for a set time interval (t_{EN}) generated by an internal one-shot. The output current is internally sensed and controlled in a fixed-frequency chopper format. Between strobe pulses, a new data word can be clocked in for the next print enable cycle.

PRINT ENABLE TIME

A high-to-low transition of the STROBE input starts an internal one-shot which sets the print enable time (t_{EN}) of the output drivers and the external high-side driver. The print enable time is determined by an external resistor (50 kΩ max) and capacitor (100 pF min) at RC_{EN} as

$$t_{EN} = R_{EN} C_{EN}$$

The print enable time can also be controlled from a microprocessor. In this mode, the internal one-shot is operated as an output disable function. In this mode, R_{EN} and C_{EN} are not used; instead a 10 kΩ series resistor is connected between RC_{EN} and an externally generated output disable pulse. As before, on the high-to-low STROBE transition, the outputs will be enabled. They will remain enabled until a low-to-high logic (≥3.3 V) DISABLE transition at RC_{EN}.

When operating in a continuous chopping mode, and neither print enable timeout nor output disable are desired, RC_{EN} should be grounded.

HIGH-SIDE DRIVER

To reduce the current decay time at the end of a print enable cycle, an external high-side driver can be used and controlled by the HIGH-SIDE DRIVER (HSD) output. The HSD is designed to drive an external N-channel MOSFET (with accompanying charge pump circuitry). During the print enable time (t_{EN}), the internal high-side driver is OFF, allowing the external high-side driver to be ON. If the external high-side driver is a P-channel device (eliminating the need for charge-pump circuitry), the HSD signal must be inverted for correct operation.

If an external high-side driver is used, an external ground clamp diode is also required.

OUTPUT CURRENT CONTROL

Each of the nine channels consists of a power Darlington sink driver, internal low-value current-sensing resistor, comparator, and an R/S flip-flop. The output current is sensed and controlled independently in each channel by means of a fixed-frequency chopper which sets the flip-flop and allows the output to turn ON. As the current increases in the load it is sensed by the internal sense resistor until the sense voltage equals the trip voltage of the comparator. At this time, the flip-flop is reset and the output is turned OFF. Over the range of V_{REF} = 1.0 V to 3.2 V, the output current trip point is a linear function of the reference voltage:

$$I_{TRIP} = V_{REF}/2$$

To ensure an accurate chop current level, an external 5 kΩ resistor (R_{CV}) is used. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays (typically 300 ns). After turn-off, the load current decays, circulating through the load and an external clamp diode. The output driver will stay OFF until the next chop pulse sets the flip-flop, turning ON the output, and allowing load current to rise again. The cycle repeats, maintaining the average printhead current at the desired level.

The chop pulse frequency is determined by an external resistor and capacitor at RC_C:

$$f_{ch} = \frac{1}{2\, R_C\, C_C}$$

To reduce the power supply and ground noise developed when operating nine channels synchronously, the outputs are split into two groups (OUTPUTS 2, 4, 6, 8 and OUTPUTS 1, 3, 5, 7, 9) for chopping pulses.

The chopping function is disabled when $V_{REF} > 4.5$ V. To prevent operation at higher than allowable current levels, V_{REF} should not exceed 3.2 V, except to disable the chopping function.

DUTY CYCLE LIMITS

For correct operation of the UCN5829EB, the duty cycle must be between 15% and 50% with 20% to 40% recommended. The lower limit is due to internal lockout circuitry while the upper limit guarantees synchronous operation. The duty cycle (dc) can be calculated as

$$dc = \frac{t_{on}}{t_{on} + t_{off}} \approx \frac{I_{OUT(P)} / I_{OUT(asym)} + v_d / v_c}{1 + v_d / v_c}$$

where $I_{OUT(asym)}$ = the asymptotic current value = v_c/R_L

v_d = discharge voltage across the load = $V_{HSD} + V_{DIODE}$

v_c = charge voltage across the load = $V_{BB} - V_{OUT(SAT)} - V_{HSD}$

For most practical cases, correct operation can be achieved if

$I_{OUT(asym)} / I_{OUT(P)} > 2.5$.

GENERAL

For applications with 9-wire printheads, SERIAL DATA OUT should be connected to IN_9. For 24-wire printhead applications, three devices (eight channels per device) are cascaded by connecting SERIAL DATA OUT to the next SERIAL DATA IN.

Each of the CMOS logic inputs have internal pull-up resistors for TTL compatibility.

An external transient-protection flyback diode is required at each output. Fast recovery diodes are recommended to reduce power dissipation in the UCN5829EB. Internal filtering prevents false triggering of the current sense comparator which can be caused by the recovery current spike of the diodes when the outputs turn ON.

The SUPPLY terminal should be well decoupled with a capacitor placed as close as possible to the device. Internal power-ON reset circuitry prevents false output triggering during power up.

Thermal protection circuitry is activated and turns OFF all drivers at a junction temperature of typically +165°C. The thermal shutdown is independent of all other functions. It should not be used as another control input but is intended only to protect the chip from catastrophic failures due to excessive junction temperatures. The output drivers are re-enabled when the junction temperature cools down to approximately +145°C.

TYPICAL APPLICATION

Shown is a typical application with the UCN5829EB controlling a chop current of 1 A through a 3 mH, 9 Ω load. To check the duty cycle and $I_{OUT(asym)}/I_{OUT(P)}$ restrictions

where $v_d = V_{HSD} + V_{DIODE} \approx 1.5 + 1.5 = 3$

$v_c = V_{BB} - V_{OUT(SAT)} - V_{HSD} = 36 - 1.5 - 1.5 = 33$

$I_{OUT(asym)} = v_c / R_L = 33 / 9 = 3.67$

then $I_{OUT(asym)} / I_{OUT(P)} = 3.67 / 1 = 3.67$

The condition of $I_{OUT(asym)} / I_{OUT(P)} > 2.5$ is met and the duty cycle will be within the proscribed limits. The actual duty cycle is

$$dc = \frac{I_{OUT(P)}/I_{OUT(asym)} + v_d/v_c}{1 + v_d/v_c} = \frac{1.0/3.67 + 2.5/33}{1 + 2.5/33} = 32\%$$

For a 50 kHz chopping frequency and a 250 µs print enable time, the remaining component values are

with $C_C = 250$ pF and $C_{EN} = 0.01$ µF

then $R_C = 1/(2\ f_{ch}\ C_C) = 1/(2 \times 50 \times 10^3 \times 250 \times 10^{-12}) = 40\ k\Omega$

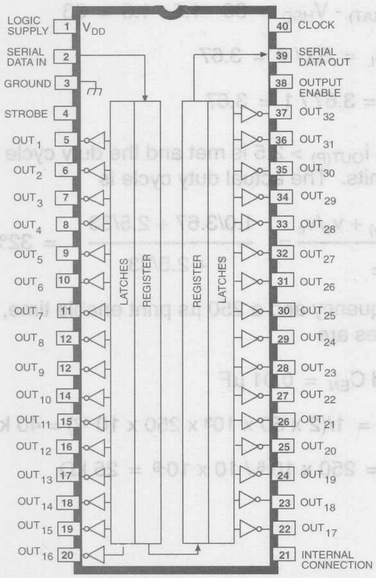
and $R_{EN} = t_{EN} / C_{EN} = 250 \times 10^{-6} / 10 \times 10^{-9} = 25\ k\Omega$

5832

26185.10A*

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5832A



Dwg. No. A-12,377A

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} .... **40 V**
Logic Supply Voltage, V_{DD} .... **15 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} .... **150 mA**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Caution: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Intended originally to drive thermal printheads, Types UCN5832A and UCN5832EP have been optimized for low output-saturation voltage, high-speed operation, and pin configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. The combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar NPN open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The UCN5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, this device will allow all outputs to sustain 100 mA continuously without derating. The UCN5832EP is supplied in a 44-lead plastic leaded chip carrier for minimum area, surface-mount applications. Both devices are also available for operation from -40°C to +85°C. To order, change the prefix from ‘UCN’ to ‘UCQ’.

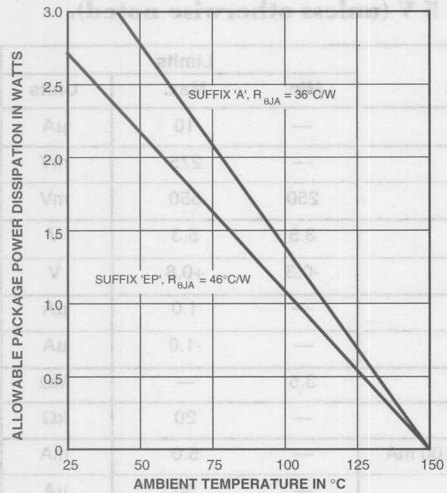
Similar 32-bit serial-input latched source drivers are available as UCN5818AF/EPF. High-voltage, high-current 8-bit devices are available in Series UCN5820A and UCN5840A/EP/LW.

FEATURES

- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage
- Automotive Capable

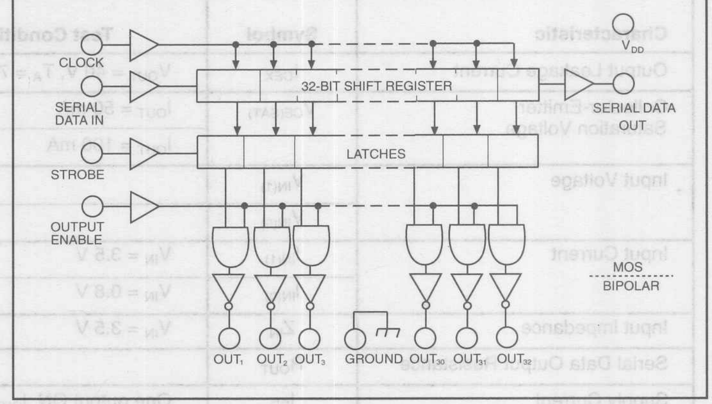
Always order by complete part number:

Part Number	Package
UCN5832A	40-Pin DIP
UCN5832EP	44-Lead PLCC

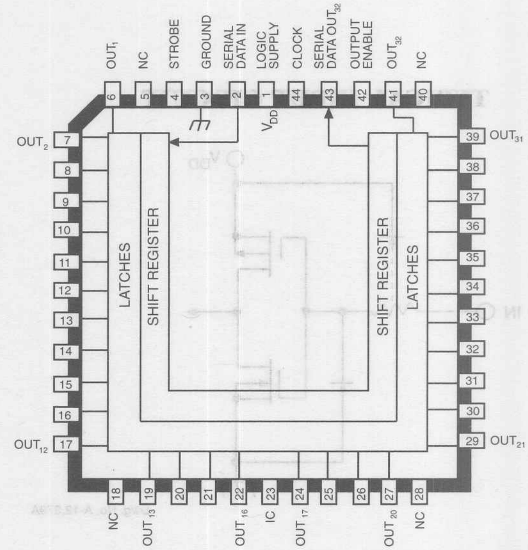


Dwg. No. GP-025

FUNCTIONAL BLOCK DIAGRAM



UCN5832EP



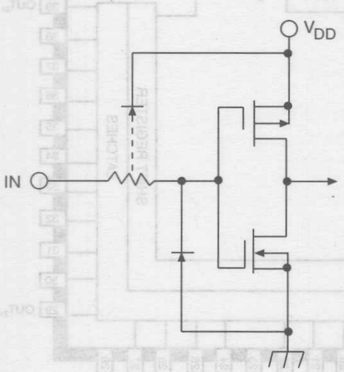
Dwg. No. A-14,360

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 40 V, T_A = 70°C	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	275	mV
		I_{OUT} = 100 mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 3.5 V	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-1.0	µA
Input Impedance	Z_{IN}	V_{IN} = 3.5 V	3.5	—	MΩ
Serial Data Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	1.0	µs

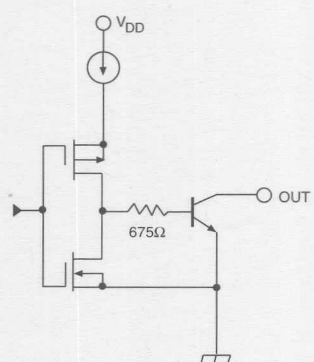
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT

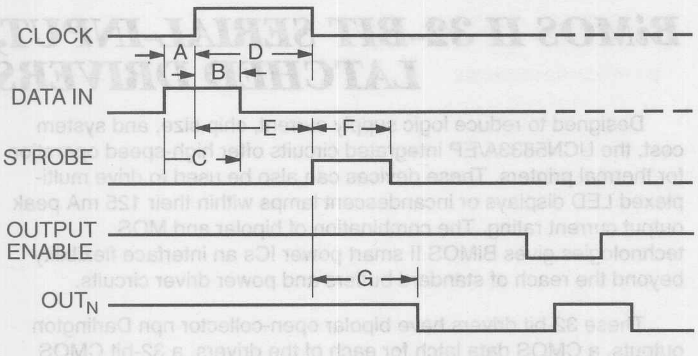


Dwg. No. A-12,379A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,380A



Dwg. No. A-12,276A

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**
C. Minimum Data Pulse Width .... **150 ns**
D. Minimum Clock Pulse Width .... **150 ns**
E. Minimum Time Between Clock Activation and Strobe .... **300 ns**
F. Minimum Strobe Pulse Width .... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	L	H	H	H	...	H	H

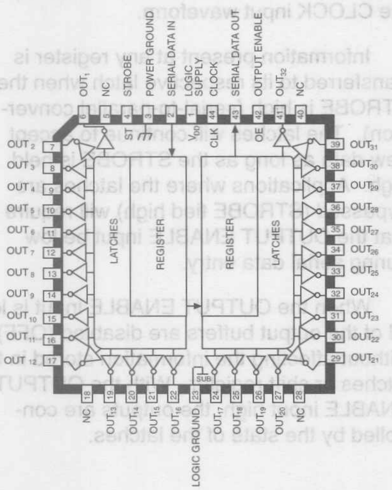
L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5833

26185.16A

BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5833EP



Dwg. No. A-13,049

Designed to reduce logic supply current, chip size, and system cost, the UCN5833A/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits.

These 32-bit drivers have bipolar open-collector npn Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN5833A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. At an ambient temperature of +75°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. For high-density applications, the UCN5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050" (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FEATURES

- To 3.3 MHz Data Input Rate
- 30 V Minimum Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . **30 V**

Logic Supply Voltage, V_{DD} . . . . **7.0 V**

Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{DD} + 0.3 V**

Continuous Output Current,
I_{OUT} (each output) . . . . **125 mA**

Package Power Dissipation, P_D
(UCN5833A) . . . . **3.5 W***
(UCN5833EP) . . . . **2.5 W***

Operating Temperature Range,
T_A . . . . **-20°C to +85°C**

Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

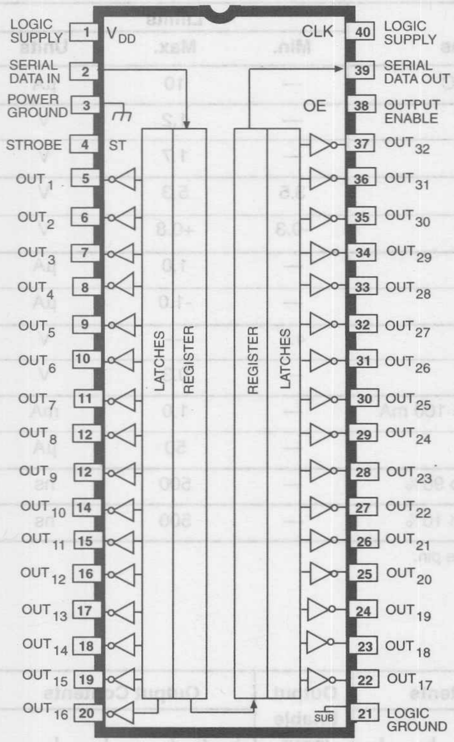
* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number:

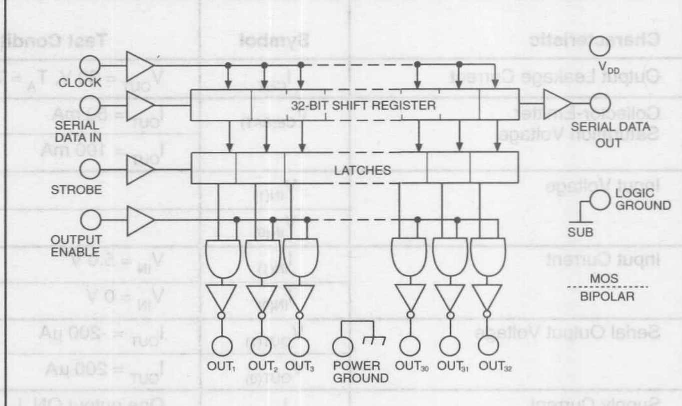
Part Number	Package
UCN5833A	**40-Pin DIP**
UCN5833EP	**44-Lead PLCC**

UCN5833A



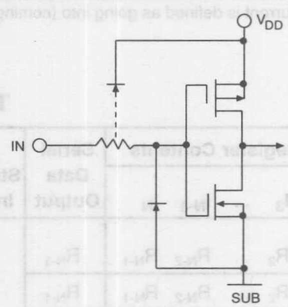
Dwg. No. A-13,048

FUNCTIONAL BLOCK DIAGRAM



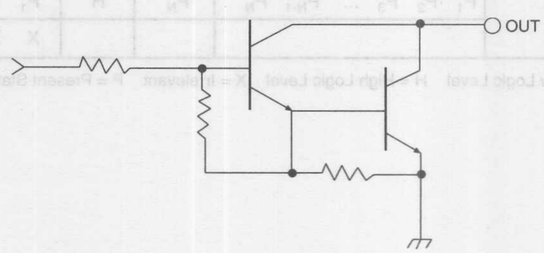
Dwg. No. A-13,057

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER



Dwg. No. A-13,051

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

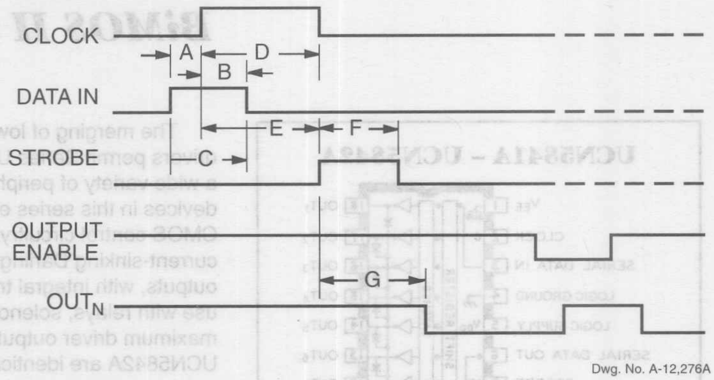
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V, T_A = 70°C	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	1.2	V
		I_{OUT} = 100 mA	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	-1.0	µA
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	0.3	V
Supply Current	I_{DD}	One output ON, I_{OUT} = 100 mA	—	1.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	500	ns
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	500	ns

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Output Enable Input	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

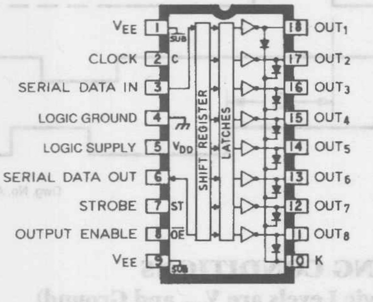
Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5841A – UCN5842A



Dwg. No. A-12,659

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{CE}
(UCN5841A/LW) . . . . **50 V**
(UCN5842A) . . . . **80 V**
Output Voltage, $V_{CE(sus)}$
(UCN5841A/LW) . . . . **35 V†**
(UCN5842A) . . . . **50 V†**
Logic Supply Voltage Range,
V_{DD} . . . . **4.5 V to 15 V**
V_{DD} with Reference to V_{EE} . . . . . . **25 V**
Emitter Supply Voltage, V_{EE} . . . . **-20 V**
Input Voltage Range,
V_{IN} . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . **500 mA**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

†For inductive load applications.

Note that the UCN5841A (dual in-line package) and UCN5841LW (small-outline IC package) are electrically identical and share a common pin number assignment.

The merging of low-power CMOS logic and bipolar output power drivers permit Series UCN5840A/LW integrated circuits to be used in a wide variety of peripheral power driver applications. The three basic devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The 500 mA NPN Darlington outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads. Except for the maximum driver output voltage ratings, the UCN5841A/LW and UCN5842A are identical. The UCN5842A offers premium performance with a minimum output-breakdown voltage rating of 80 V (50 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

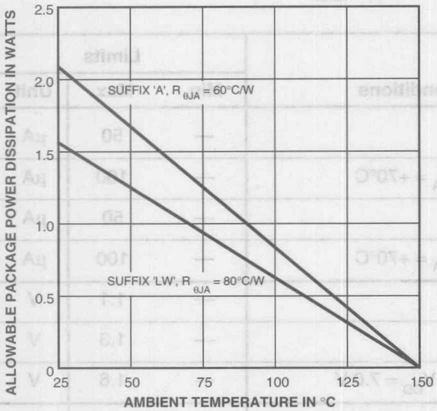
BiMOS II devices have higher data-input rates than the earlier BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

Suffix 'A' devices are furnished in a standard 18-pin plastic DIP; suffix 'LW' indicates an 18-lead wide-body SOIC.

FEATURES

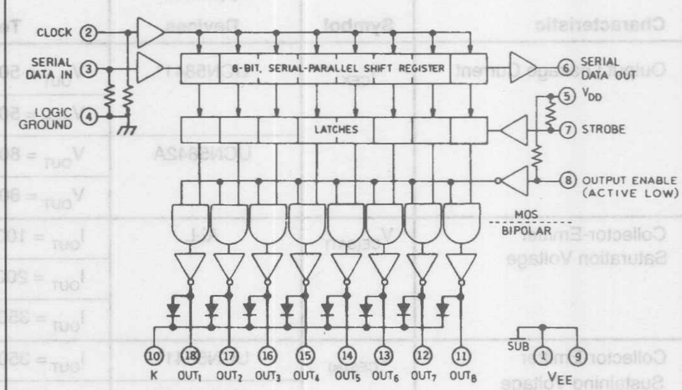
- To 3.3 MHz Data-Input Rate
- CMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches,
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- DIP or SOIC Packaging

Always order by complete part number, e.g., UCN5841LW.



Dwg. No. GP-018B

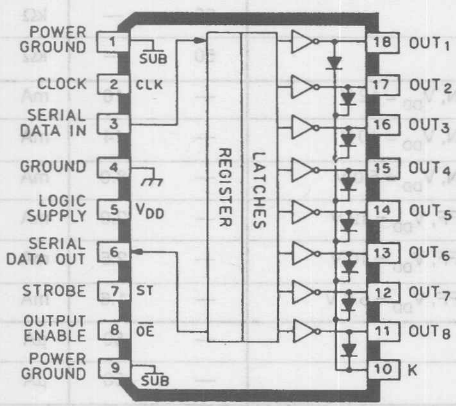
FUNCTIONAL BLOCK DIAGRAM
('A' & 'LW' Package Shown)



Dwg. No. A-12,661A

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN5841LW



Dwg. No. A-14,438

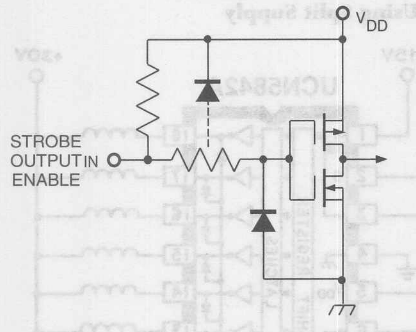
Note that the UCN5841A (dual in-line package) and UCN5841LW (small-outline IC package) are electrically identical and share a common pin number assignment.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{EE} = 0 V (unless otherwise specified).

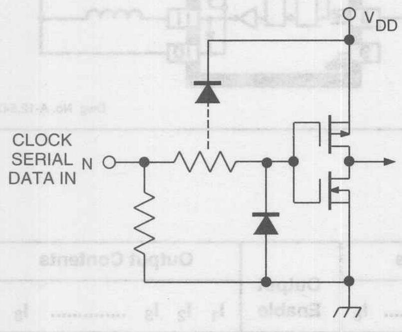
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	UCN5841*	V_{OUT} = 50 V	—	50	µA
			V_{OUT} = 50 V, T_A = +70°C	—	100	µA
		UCN5842A	V_{OUT} = 80 V	—	50	µA
			V_{OUT} = 80 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	UCN5841*	I_{OUT} = 350 mA, L = 2 mH	35	—	V
		UCN5842A	I_{OUT} = 350 mA, L = 2 mH	50	—	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 12 V	10.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 12 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, V_{DD} = 12 V	—	16	mA
			All Drivers ON, V_{DD} = 10 V	—	14	mA
			All Drivers ON, V_{DD} = 5.0 V	—	8.0	mA
	$I_{DD(OFF)}$	ALL	All Drivers OFF, V_{DD} = 12 V	—	2.9	mA
			All Drivers OFF, V_{DD} = 10 V	—	2.5	mA
			All Drivers OFF, V_{DD} = 5.0 V	—	1.6	mA
Clamp Diode Leakage Current	I_R	UCN5841*	V_R = 50 V	—	50	µA
		UCN5842A	V_R = 80 V	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	—	2.0	V

* Complete part number includes a suffix to identify package style: A = DIP, LW = SOIC.

TYPICAL INPUT CIRCUITS

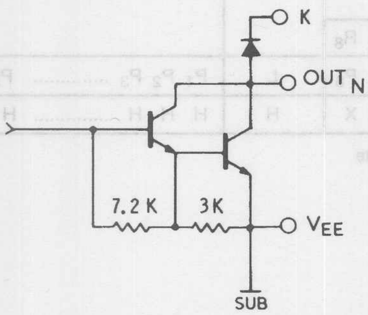


Dwg. No. EP-010-3

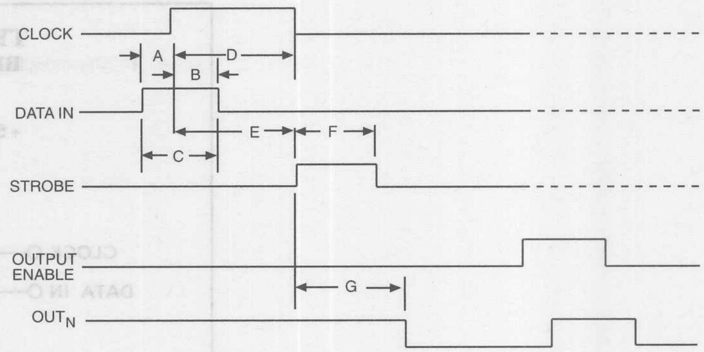


Dwg. No. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,660



Dwg. No. A-12,627

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

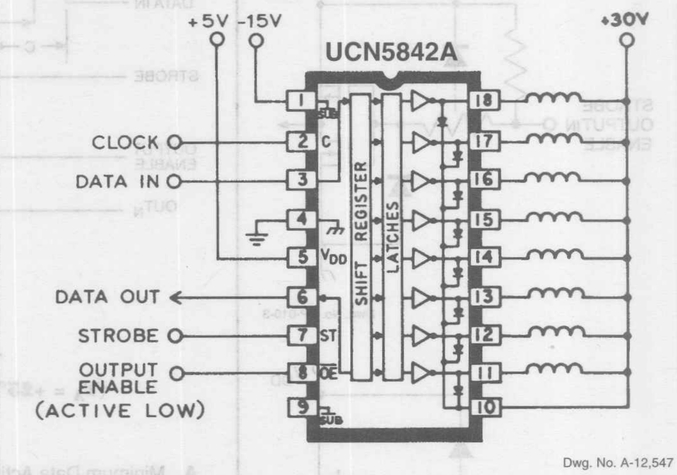
G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

TYPICAL APPLICATION
RELAY/SOLENOID DRIVER
Using Split Supply



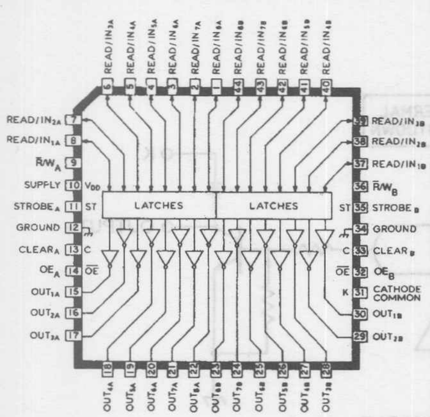
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	....	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	....	I_8	Output Enable	Output Contents I_1	I_2	I_3	....	I_8
H	↑	H	R_1	R_2	....	R_7	R_7												
L	↑	L	R_1	R_2	....	R_7	R_7												
X	↓	R_1	R_2	R_3	....	R_8	R_8												
		X	X	X	....	X	X	L	R_1	R_2	R_3	....	R_8						
		P_1	P_2	P_3	....	P_8	P_8	H	P_1	P_2	P_3	....	P_8	L	P_1	P_2	P_3	....	P_8
									X	X	X	....	X	H	H	H	H	....	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

26180.16

BiMOS II DUAL 8-BIT LATCHED DRIVER WITH READ BACK



Dwg. No. A-14,225

With 16 CMOS data latches (two sets of eight), CMOS control circuitry for each set of latches, and a bipolar saturated driver for each latch, the UCN5881EP provides low-power interface with maximum flexibility. The driver includes thermal shutdown circuitry to protect against damage from high junction temperatures and clamp diodes for inductive load transient suppression.

The CMOS inputs cause minimal circuit loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull up resistors. When reading back, each data input will sink 8 mA (if its corresponding latch is low) or source 400 μA (if its corresponding latch is high). The read back feature is for error checking. It allows the system to verify that data has been received and latched.

The bipolar outputs are suitable for use with low-power relays, solenoids, and stepping motors. The very-low output saturation voltage makes this device well-suited for driving LED arrays. The output transistors are capable of sinking 50 mA and will maintain at least 20 V in the OFF state. Outputs may be paralleled for higher current capability.

The UCN5881EP dual 8-bit latched sink driver is rated for operation over the temperature range of -20°C to +85°C and is supplied in a plastic 44-lead chip carrier conforming to the JEDEC MS-007AB outline.

FEATURES

- 4.4 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic
- 20 V, 50 mA (Max.) Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier

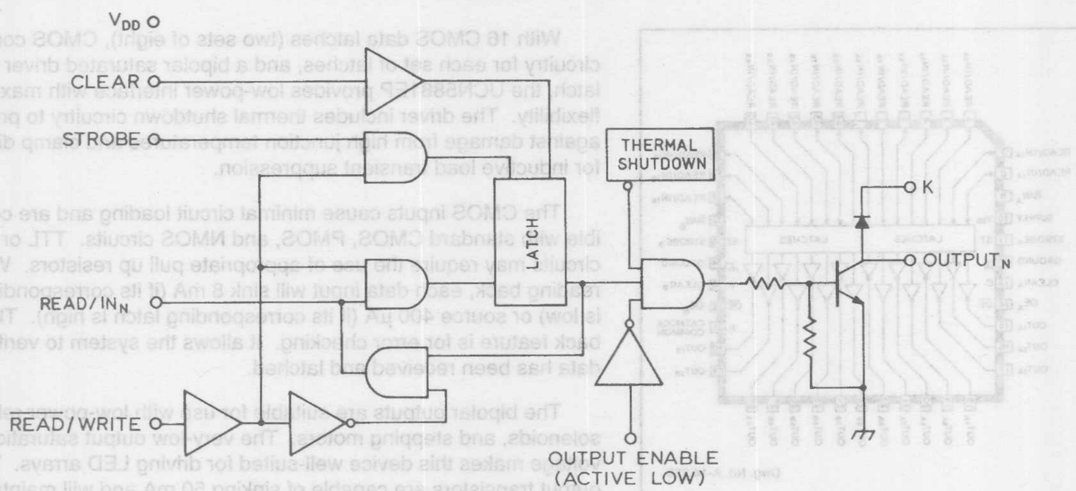
ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} .... **20 V**
Output Sustaining Voltage, $V_{CE(sus)}$ ... **15 V**
Output Current, I_{OUT} .... **50 mA**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Logic Supply Voltage, V_{DD} .... **15 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

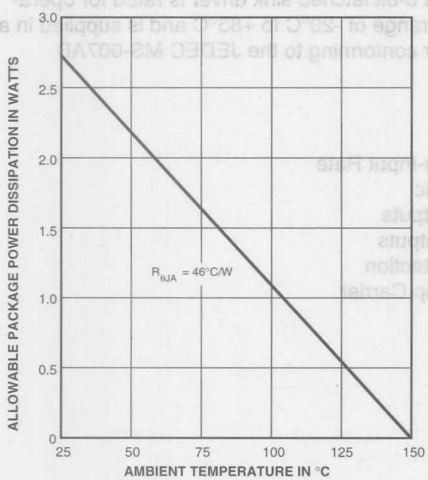
Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number: **UCN5881EP**

FUNCTIONAL BLOCK DIAGRAM
(1 of 16 Channels)



Dwg. No. A-14,227



Dwg. No. GP-025-1A

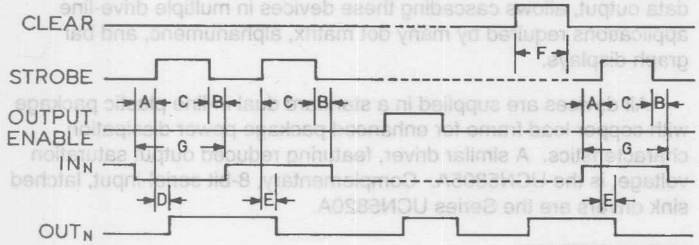
TRUTH TABLE

Read/In	Strobe	Clear	Output Enable	$\overline{\text{Read/Write}}$	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

n = Present Latch Contents
n-1 = Previous Latch Contents
X = Irrelevant

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{DD} = 5$ V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 20$ V	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 10$ mA	—	0.1	V
		$I_{OUT} = 25$ mA	—	0.5	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = 25$ mA, L = 2 mH	15	—	V
Input Voltage	$V_{IN(0)}$		-0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	-10	µA
	$I_{IN(1)}$	$V_{IN} = 5$ V	—	10	µA
Readback Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -400$ µA	3.5	—	V
	$V_{OUT(0)}$	$I_{OUT} = 5.0$ mA	—	0.8	V
Logic Supply Current	I_{DD}	All Drivers ON	—	14	mA
		All Drivers OFF	—	3.0	mA
Clamp Diode Leakage Current	I_R	$V_R = 20$ V	—	50	µA
Clamp Diode Forward Voltage	V_F	$I_F = 50$ mA	—	1.5	V



Dwg. No. A-14,228

TIMING CONDITIONS
($V_{DD} = 5.0$ V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output ON to OFF Transition . . . . **5 µs**

E. Typical Time Between Strobe Activation and Output OFF to ON Transition . . . . **500 ns**

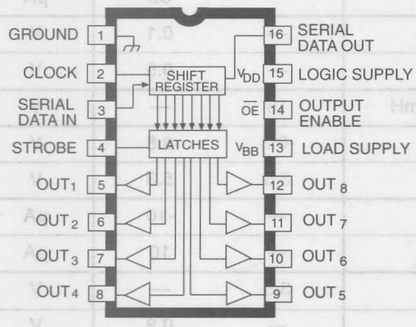
F. Minimum Clear Pulse Width . . . . **225 ns**

G. Minimum Data Pulse Width . . . . **225 ns**

A high on the READ/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

A low on the READ/WRITE input will allow the latched data to be read back on the data input lines. Allow a minimum of 750 ns delay (will increase with capacitive loading) before reading back the state of the latches. The read back feature is for error checking applications and allows the system to verify that data has been received and latched.

BIMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg. No. A-12,639

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{OUT}
(UCN5890A) .... **80 V**
(UCN5891A) .... **50 V**
Logic Supply Voltage Range,
V_{DD} .... **4.5 V to 15 V**
Driver Supply Voltage Range, V_{BB}
(UCN5890A) .... **20 V to 80 V**
(UCN5891A) .... **5.0 V to 50 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} .... **-500 mA**
Allowable Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Frequently applied in non-impact printer systems, the UCN5890A and UCN5891A are BiMOS II serial-input, latched source (high-side) drivers. The octal, high-current smart-power ICs merge an 8-bit CMOS shift register, associated CMOS latches, and CMOS control logic (strobe and output enable) with sourcing power Darlington outputs. Typical applications include multiplexed LED and incandescent displays, relays, solenoids, and similar peripheral loads to a maximum of -500 mA per output.

Except for output voltage ratings, these smart high-side driver ICs are equivalent. The UCN5890A is rated for operation with load supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. The UCN5891A is optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining).

BiMOS II devices have higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output, allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

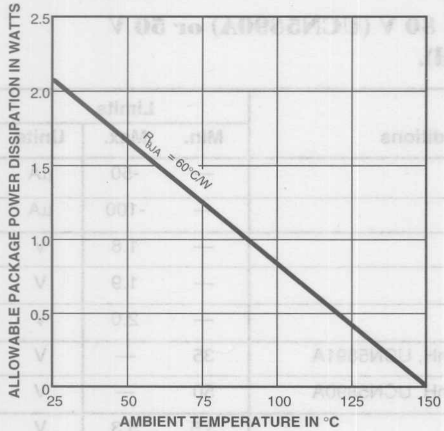
All devices are supplied in a standard dual in-line plastic package with copper lead frame for enhanced package power dissipation characteristics. A similar driver, featuring reduced output saturation voltage, is the UCN5895A. Complementary, 8-bit serial-input, latched sink drivers are the Series UCN5820A.

FEATURES

- 50 V or 80 V Source Outputs
- Output Current to -500 mA
- Output Transient-Suppression Diodes
- To 3.3 MHz Data-Input Rate
- Low-Power CMOS Logic and Latches

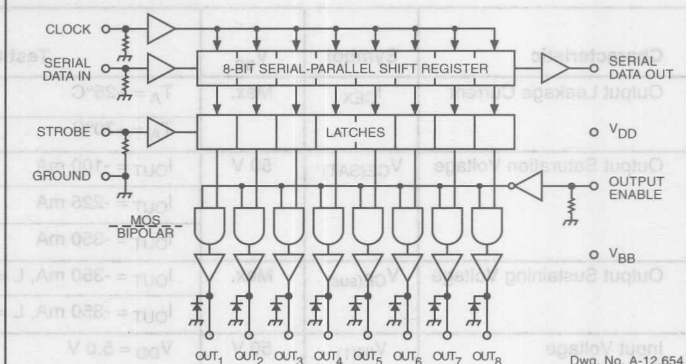
Always order by complete part number:

Part Number	Max. V_{OUT}
UCN5890A	**80 V**
UCN5891A	**50 V**



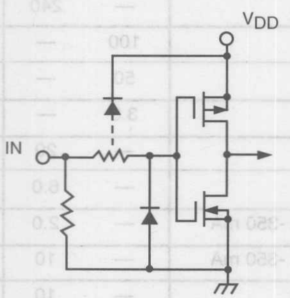
Dwg. GP-016

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,654

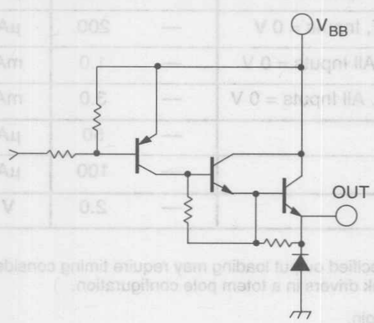
TYPICAL INPUT CIRCUIT



Dwg. EP-010-YA

Number of Outputs ON at I_{OUT} = -200 mA	Max. Allowable Duty Cycle at T_A of 50°C	60°C	70°C
8	53%	47%	41%
7	60%	54%	48%
6	70%	64%	56%
5	83%	75%	67%
4	100%	94%	84%
3	100%	100%	100%
2	100%	100%	100%
1	100%	100%	100%

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,648

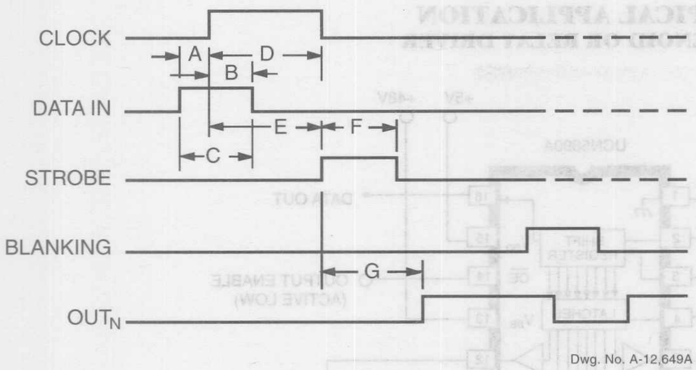
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 80 V (UCN5890A) or 50 V (UCN5891A), V_{DD} = 5 V and 12 V (unless otherwise noted).

Characteristic	Symbol	V_{BB}	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	Max.	T_A = +25°C	—	-50	µA
			T_A = +70°C	—	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	I_{OUT} = -100 mA	—	1.8	V
			I_{OUT} = -225 mA	—	1.9	V
			I_{OUT} = -350 mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	I_{OUT} = -350 mA, L = 2 mH, UCN5891A	35	—	V
			I_{OUT} = -350 mA, L = 2 mH, UCN5890A	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	50 V	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	V_{DD} = V_{IN} = 5.0 V	—	50	µA
			V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	50 V	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Max. Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, I_{OUT} = -350 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, I_{OUT} = -350 mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
			V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
			V_{DD} = 5 V, One output ON, All Inputs = 0 V	—	1.0	mA
			V_{DD} = 12 V, One output ON, All Inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	T_A = +25°C	—	50	µA
			T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	Open	I_F = 350 mA	—	2.0	V

NOTES: Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing considerations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

Positive (negative) current is defined as going into (coming out of) the specified device pin.

5890 AND 5891
BiMOS II 8-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

TIMING CONDITIONS
(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse
(Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse
(Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe**300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

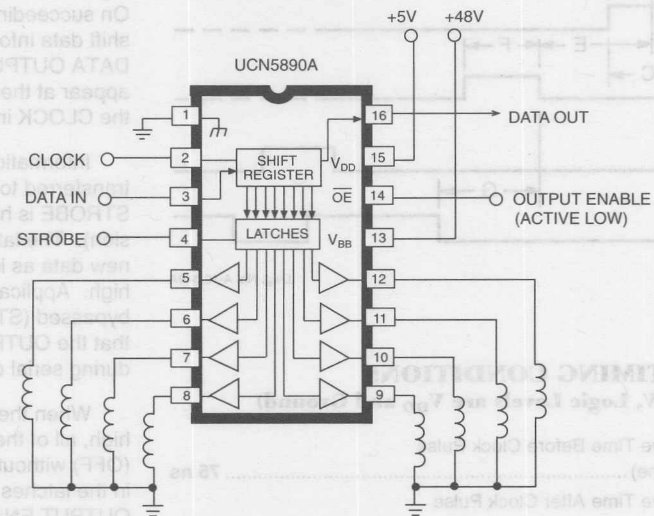
G. Typical Time Between Strobe Activation and
Output Transition .... **1.0 μs**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
							X	X	X	...	X	X	H	L	L	L	...	L	L			

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

TYPICAL APPLICATION
SOLENOID OR RELAY DRIVER



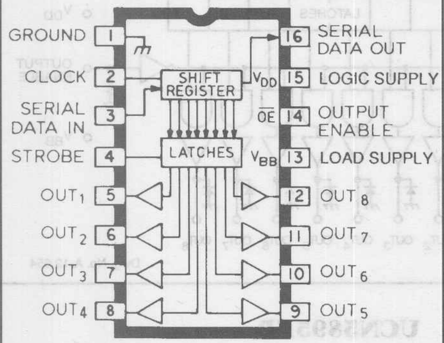
Dwg. No. A-12,548

5895

26182.14A

BiMOS II 8-BIT SERIAL INPUT, LATCHED SOURCE DRIVERS

UCN5895A



Dwg. No. A-12,639

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{OUT} .... **50 V**
Logic Supply Voltage Range,
V_{DD} .... **4.5 V to 12 V**
Driver Supply Voltage Range,
V_{BB} .... **5.0 V to 50 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} .... **-250 mA**
Allowable Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5895A and UCN5895EP BiMOS II serial-input, latched source drivers are designed for applications emphasizing low output saturation voltages and currents to -250 mA per output. These smart high-side octal, driver ICs merge an 8-bit CMOS shift register, associated CMOS latches, and CMOS control logic (strobe and output enable) with medium current emitter-follower (sourcing) outputs. Typical applications include incandescent or LED displays (both directly driven and multiplexed), non-impact (i.e., thermal) printers, relays, and solenoids.

The UCN5895A and UCN5895EP are suitable for high-side applications to -250 mA per channel. The maximum supply voltage is 50 V and a minimum output sustaining voltage rating of 35 V for inductive load applications. Under normal operating conditions, the UCN5895A is capable of providing -120 mA (8 outputs continuous and simultaneous) at +65°C with a logic supply of 5 V. Similar devices, with higher output current ratings, are the UCN5890A and UCN5891A.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

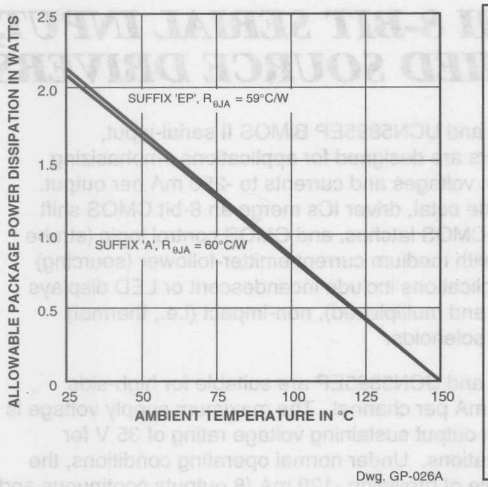
The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of -20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN5895A is supplied in a standard 16-pin dual in-line plastic package with a copper lead frame for increased allowable package power dissipation. The UCN5895EP is supplied in a 20-lead plastic leaded chip carrier for minimum area, surface-mount applications.

FEATURES

- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to -250 mA
- To 3.3 MHz Data-Input Rate
- Low-Power CMOS Logic & Latches

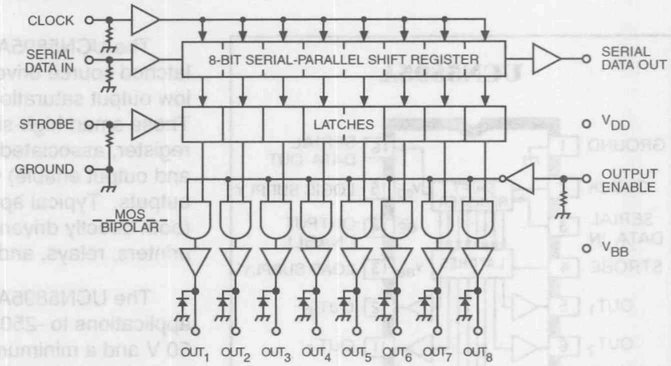
Always order by complete part number, e.g., **UCN5895A**



Dwg. GP-026A

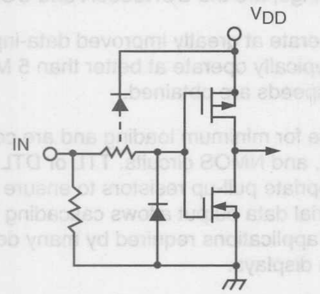
FUNCTIONAL BLOCK DIAGRAM

('A' Package pin numbers shown)



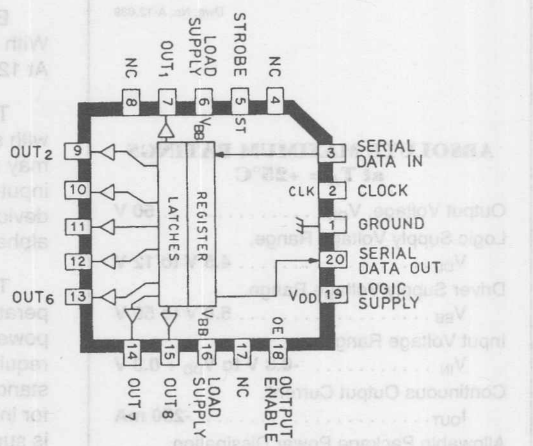
Dwg. No. A-12,654

TYPICAL INPUT CIRCUIT



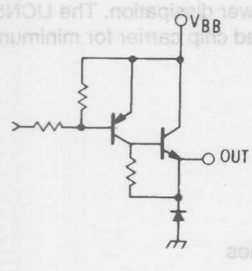
Dwg. EP-010-4A

UCN5895EP



Dwg. No. A-14,368

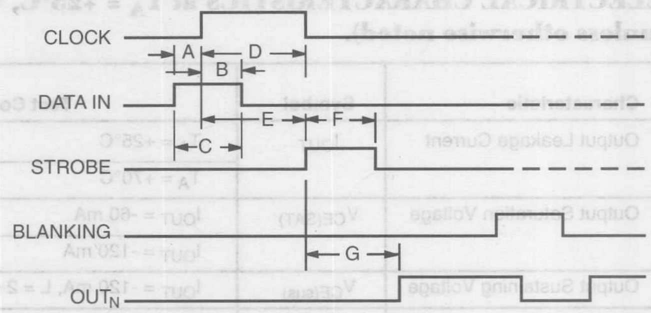
TYPICAL OUTPUT DRIVER



Dwg. No. A-12,655

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5 V and 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{OUT}	T_A = +25°C	—	-50	µA
		T_A = +70°C	—	-100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = -60 mA	—	1.1	V
		I_{OUT} = -120 mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = -120 mA, L = 2 mH	35	—	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	50	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	100	—	kΩ
		V_{DD} = 12 V	50	—	kΩ
Max. Clock Frequency	f_{CLK}		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, I_{OUT} = -120 mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, I_{OUT} = -120 mA	—	10	µs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	µA
	I_{DD}	V_{DD} = 5 V, All outputs OFF, Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
		V_{DD} = 5 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	V_R = 25 V, T_A = +25°C	—	50	µA
		V_R = 25 V, T_A = +70°C	—	100	µA
Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V



Dwg. No. A-12,649A

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

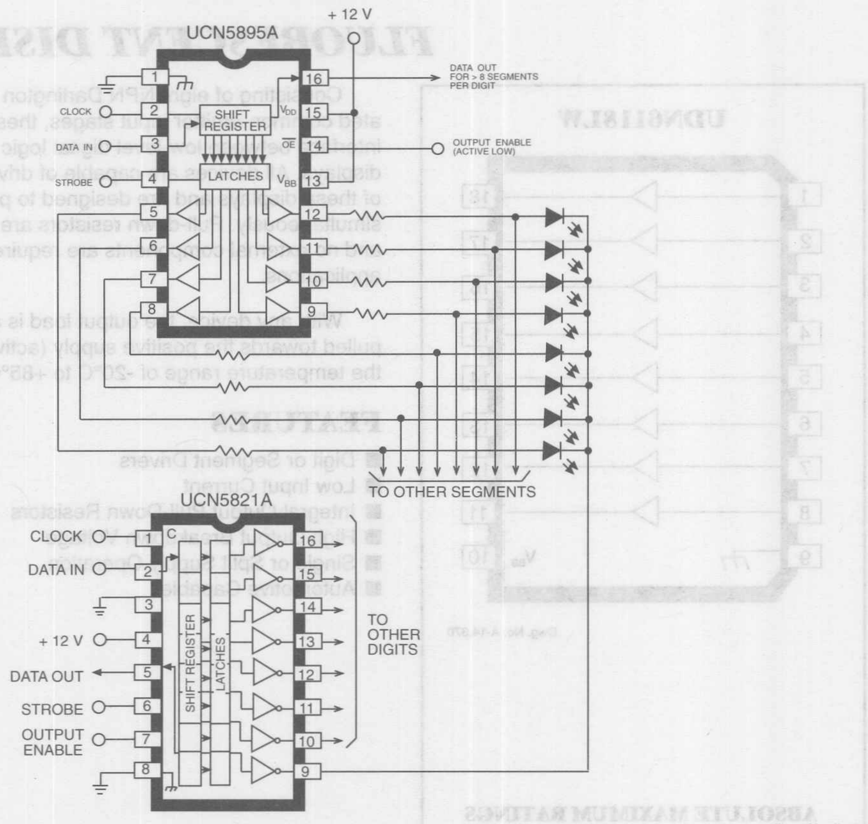
G. Typical Time Between Strobe Activation and Output Transition .... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

TYPICAL APPLICATION



Dwg. No. B-1541

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	...	I_{N-1}	I_N	Output Enable	Output Contents I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

6118

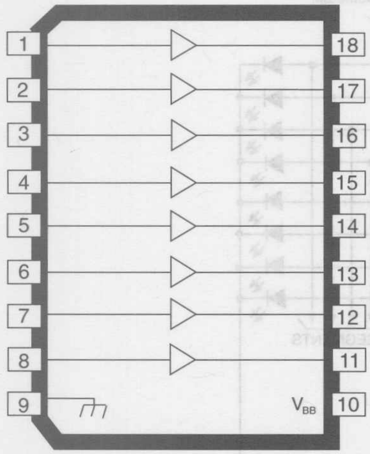
29313C

FLUORESCENT DISPLAY DRIVERS

Consisting of eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. All devices are capable of driving the digits and/or segments of these displays and are designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications.

With any device, the output load is activated when the input is pulled towards the positive supply (active 'high'). All units operate over the temperature range of -20°C to +85°C.

UDN6118LW



Dwg. No. A-14,370

FEATURES

- Digit or Segment Drivers
- Low Input Current
- Integral Output Pull-Down Resistors
- High Output Breakdown Voltage
- Single or Split Supply Operation
- Automotive Capable

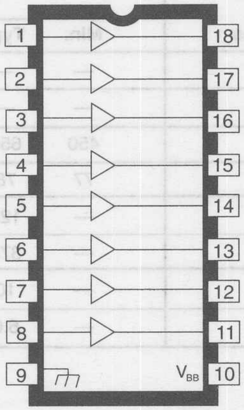
ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

Supply Voltage, V_{BB} . . . . **85 V**
Input Voltage, V_{IN} . . . . **20 V**
Output Current, I_{OUT} . . . . **-40 mA**
Allowable Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Caution: The high input impedance of these devices makes them susceptible to static discharge damage associated with handling and testing. Techniques similar to those used for handling MOS devices should be employed.

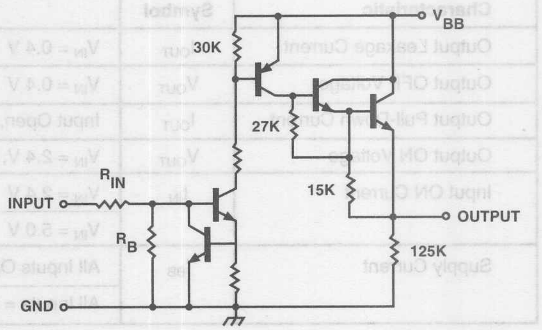
Always order by complete part number, e.g., **UDN6118A**.

UDN6118A



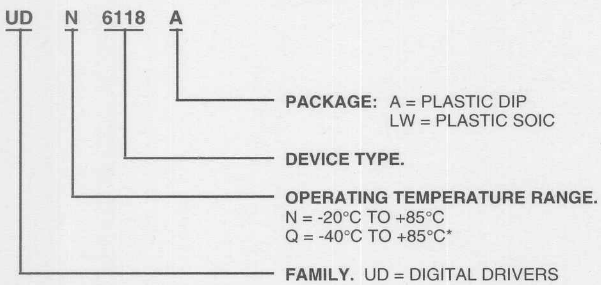
Dwg. No. A-9641A

PARTIAL SCHEMATIC
ONE DRIVER (ALL TYPES)

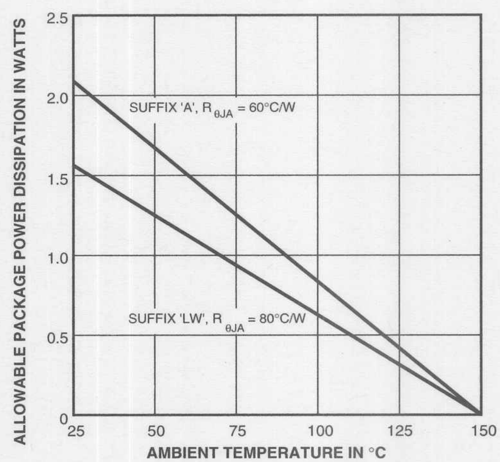


Dwg. No. A-10,592C

R_{IN}	R_B
10 kΩ	30 kΩ



* Devices are also available for operation between -40°C and +85°C. To order, change the prefix from 'UDN' to 'UDQ'.



Dwg. No. GP-018B

ELECTRICAL CHARACTERISTICS (over operating temperature range) at V_{BB} = 80 V.

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{OUT}	V_{IN} = 0.4 V	—	—	15	µA
Output OFF Voltage	V_{OUT}	V_{IN} = 0.4 V	—	—	1.0	V
Output Pull-Down Current	I_{OUT}	Input Open, $V_{OUT} = V_{BB}$	450	650	1100	µA
Output ON Voltage	V_{OUT}	V_{IN} = 2.4 V, I_{OUT} = -25 mA	77	78	—	V
Input ON Current	I_{IN}	V_{IN} = 2.4 V	—	120	225	µA
		V_{IN} = 5.0 V	—	375	650	µA
Supply Current	I_{BB}	All Inputs Open	—	10	100	µA
		All Inputs = 2.4 V	—	6.0	9.0	mA

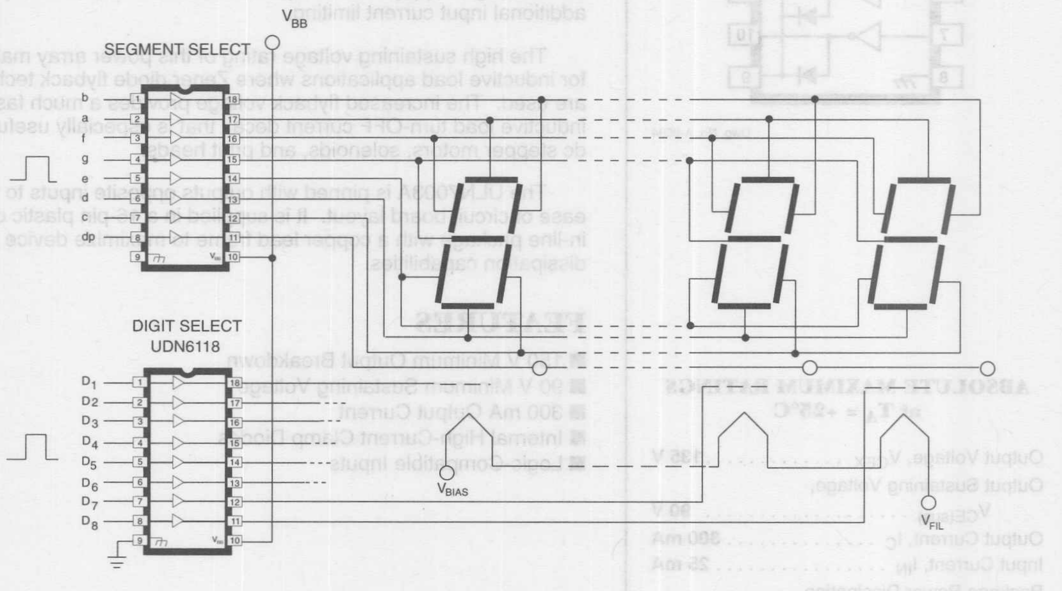
6118
FLUORESCENT DISPLAY DRIVERS

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage	V_{BB}		5.0	—	70	V
Input ON Voltage	V_{IN}		2.4	—	15	V
Output ON Current	I_{OUT}		—	—	-25	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL MULTIPLEXED FLUORESCENT DISPLAY

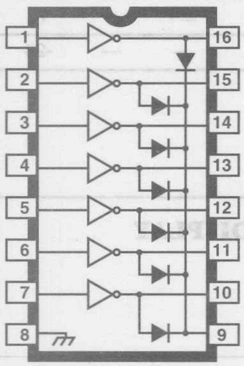


Dwg. No. A-10,261B

7003

29304.10

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAY



Dwg. No. A-9594

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{CEX} .... 135 V
Output Sustaining Voltage,
$V_{CE(sus)}$ .... **90 V**
Output Current, I_C .... **300 mA**
Input Current, I_{IN} .... **25 mA**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current may be limited by duty cycle, number of drivers operating, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified maximum current rating or a junction temperature of 150°C.

Integrating seven high-voltage, high-current npn Darlingtons into a monolithic power array, the ULN7003A is designed for interfacing between TTL or CMOS logic and a variety of peripheral loads. The seven open-collector Darlington outputs are specified for 135 V minimum breakdown and 90 V minimum sustaining. Included are integral power diodes for switching inductive loads. Typical applications include relays, lamps, print heads and hammers, solenoids, and level shifting to power discretes.

The ULN7003A includes input current-limiting resistors compatible with the drive capabilities of TTL and (most) CMOS operating at a nominal logic supply of 5 V. Operation with 12 V CMOS may require additional input current limiting.

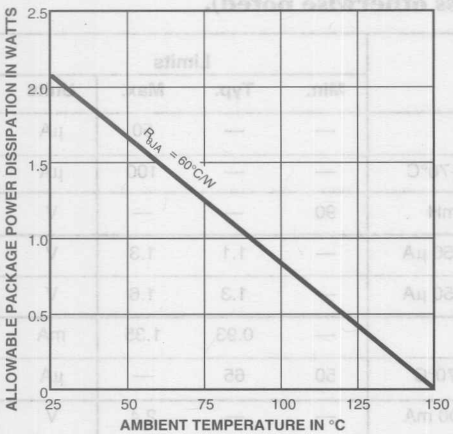
The high sustaining voltage rating of this power array makes it ideal for inductive load applications where Zener diode flyback techniques are used. The increased flyback voltage provides a much faster inductive load turn-OFF current decay that is especially useful with dc stepper motors, solenoids, and print heads.

The ULN7003A is pinned with outputs opposite inputs to facilitate ease of circuit board layout. It is supplied in a 16-pin plastic dual in-line package with a copper lead frame to maximize device power dissipation capabilities.

FEATURES

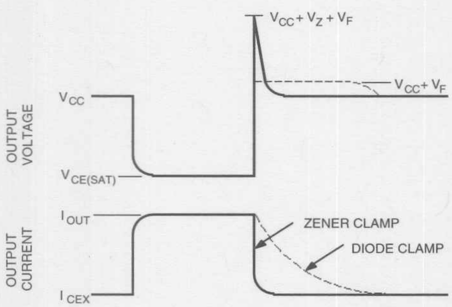
- 150 V Minimum Output Breakdown
- 90 V Minimum Sustaining Voltage
- 300 mA Output Current
- Internal High-Current Clamp Diodes
- Logic-Compatible Inputs

Always order by complete part number: ULN7003A .



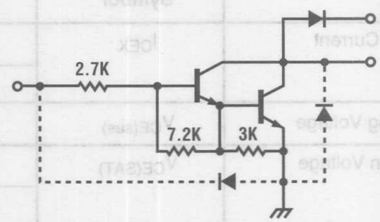
Dwg. No. GP-016

A Zener diode can be used to increase the flyback voltage. This gives a much faster inductive load turn-OFF current decay. The maximum Zener voltage plus the load supply voltage plus the internal diode forward voltage must not exceed the device's rated sustaining voltage.



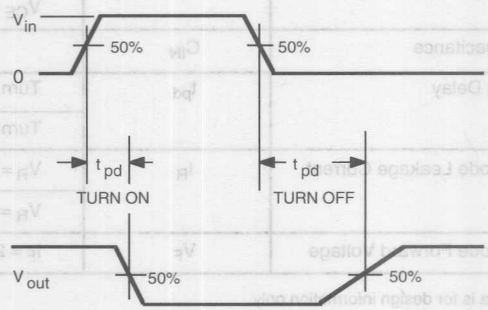
Dwg. No. WP-001

PARTIAL SCHEMATIC
(ONE OF SEVEN DRIVERS)



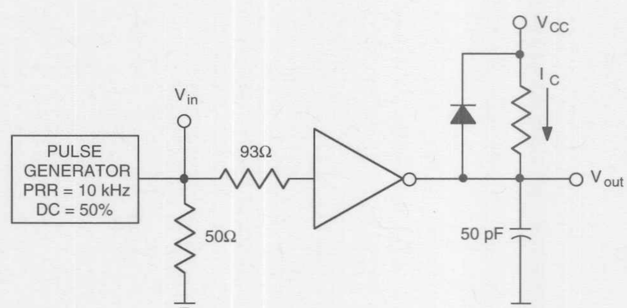
Dwg. No. A-9651

SWITCHING DELAY TEST CIRCUIT



V_{in} = 3.5 V for ULN7003A

Dwg. No. WP-010



Dwg. No. EP-020

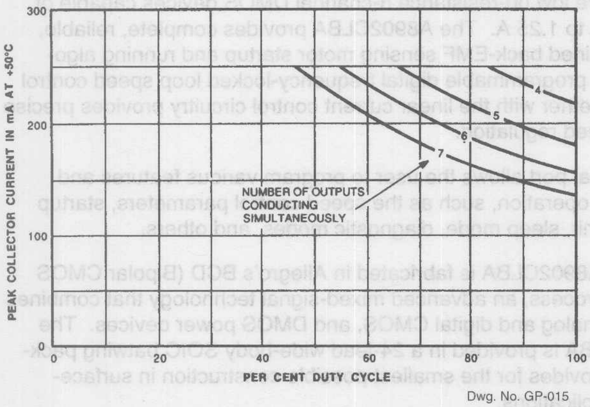
ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 135 V	—	—	50	µA
		V_{CE} = 135 V, T_A = +70°C	—	—	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 250 mA, L = 2 mH	90	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA, I_{IN} = 250 µA	—	1.1	1.3	V
		I_C = 250 mA, I_{IN} = 350 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	V_{IN} = 3.85 V	—	0.93	1.35	mA
	$I_{IN(OFF)}$	I_C = 500 µA, T_A = +70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
		V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
Input Capacitance	C_{IN}		—	15	25	pF
Switching Delay	t_{pd}	Turn On, I_C = 250 mA	—	0.05	1.0	µs
		Turn Off, I_C = 250 mA	—	0.5	1.0	µs
Clamp Diode Leakage Current	I_R	V_R = 150 V	—	—	50	µA
		V_R = 150 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 250 mA	—	1.7	2.0	V

Typical Data is for design information only.

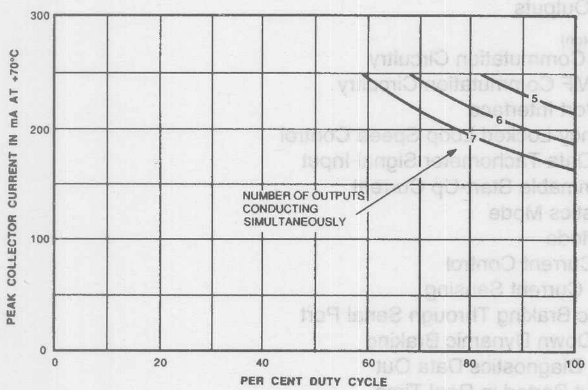
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

at T_A = +50°C



Dwg. No. GP-015

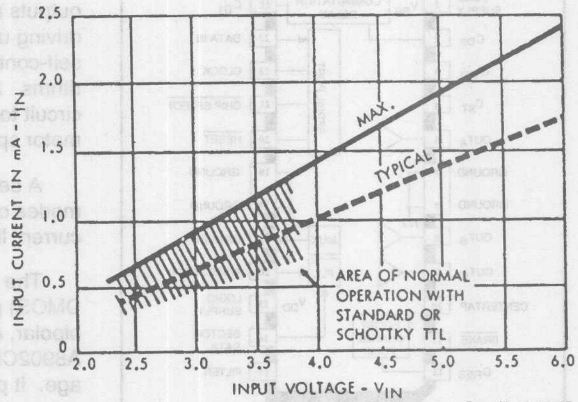
at T_A = +70°C



Dwg. No. GP-015-1

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

at T_A = +25°C

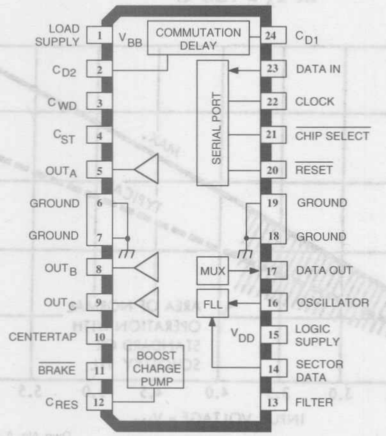


Dwg. No. A-9756B

8902–A

26301.2

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING



Dwg. PP-040B

The A8902CLBA is a three-phase brushless dc motor controller/driver for use in 5 V or 12 V hard-disk drives. The three half-bridge outputs are low on-resistance n-channel DMOS devices capable of driving up to 1.25 A. The A8902CLBA provides complete, reliable, self-contained back-EMF sensing motor startup and running algorithms. A programmable digital frequency-locked loop speed control circuit together with the linear current control circuitry provides precise motor speed regulation.

A serial port allows the user to program various features and modes of operation, such as the speed control parameters, startup current limit, sleep mode, diagnostic modes, and others.

The A8902CLBA is fabricated in Allegro's BCD (Bipolar CMOS DMOS) process, an advanced mixed-signal technology that combines bipolar, analog and digital CMOS, and DMOS power devices. The A8902CLBA is provided in a 24-lead wide-body SOIC batwing package. It provides for the smallest possible construction in surface-mount applications.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} . . . . 14 V
Output Current, I_{OUT} . . . . ±1.25 A
Logic Supply Voltage, V_{DD} . . . . 6.0 V
Logic Input Voltage Range,
V_{IN} . . . . -0.3 V to V_{DD} + 0.3 V
Package Power Dissipation,
P_D . . . . See Graph
Operating Temperature Range,
T_A . . . . 0°C to +70°C
Junction Temperature, T_J . . . . +150°C†
Storage Temperature Range,
T_S . . . . -55°C to +150°C

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

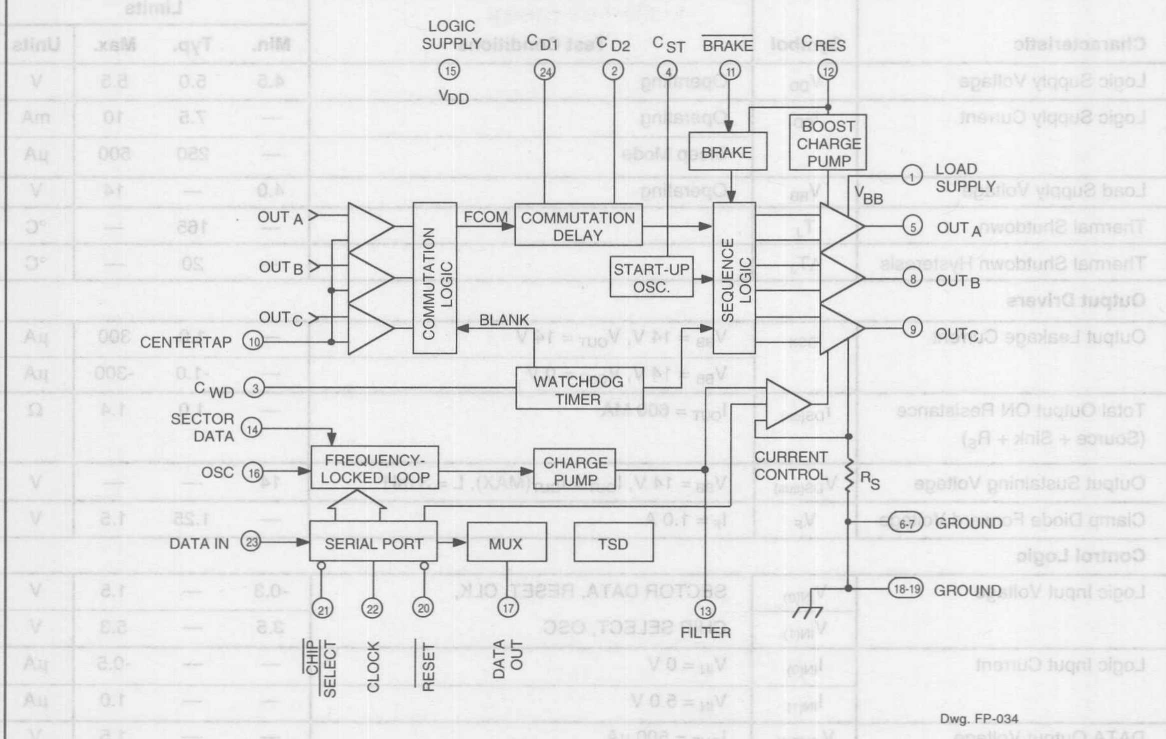
Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

FEATURES

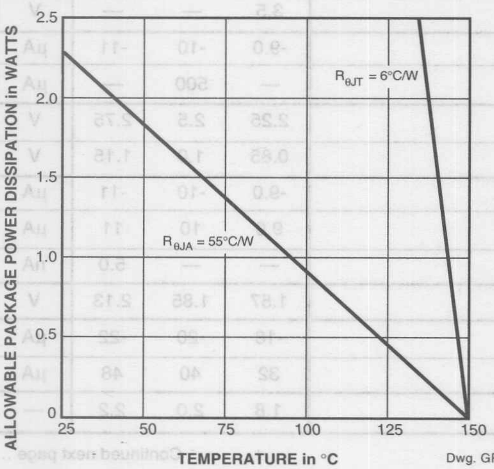
- DMOS Outputs
- Low $r_{DS(on)}$
- Startup Commutation Circuitry
- Back-EMF Commutation Circuitry
- Serial Port Interface
- Frequency-Locked Loop Speed Control
- Sector Data Tachometer Signal Input
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Internal Current Sensing
- Dynamic Braking Through Serial Port
- Power-Down Dynamic Braking
- System Diagnostics Data Out
- Data Out Ported in Real Time
- Internal Thermal Shutdown Circuitry

Always order by complete part number, e.g., **A8902CLBA**

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-034



Dwg. GP-019B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V

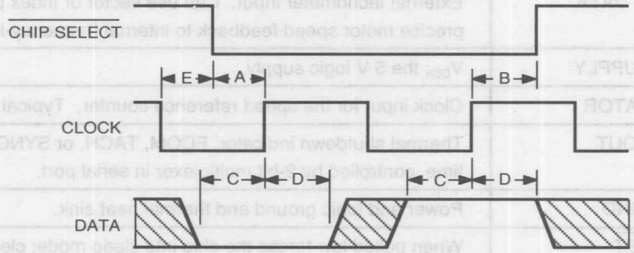
Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	250	500	µA
Load Supply Voltage	V_{BB}	Operating	4.0	—	14	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J			20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{BB} = 14 V, V_{OUT} = 14 V	—	1.0	300	µA
		V_{BB} = 14 V, V_{OUT} = 0 V	—	-1.0	-300	µA
Total Output ON Resistance (Source + Sink + R_S)	$r_{DS(on)}$	I_{OUT} = 600 MA	—	1.0	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	V_{BB} = 14 V, I_{OUT} = I_{OUT}(MAX), L = 3 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	SECTOR DATA, RESET, CLK,	-0.3	—	1.5	V
	$V_{IN(1)}$	CHIP SELECT, OSC	3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	-9.0	-10	-11	µA
		Discharging	—	500	—	µA
C_{ST} Threshold	V_{CSTH}		2.25	2.5	2.75	V
	V_{CSTL}		0.85	1.0	1.15	V
Filter Current	I_{FILTER}	Charging	-9.0	-10	-11	µA
		Discharging	9.0	10	11	µA
		Leakage, V_{FILTER} = 2.5 V	—	—	5.0	nA
Filter Threshold	$V_{FILTERTH}$		1.57	1.85	2.13	V
C_D Current (C_{D1} or C_{D2})	I_{CD}	Charging	-18	-20	-22	µA
		Discharging	32	40	48	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	1.8	2.0	2.2	—

Continued next page ...

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
C_D Threshold	V_{CDTH}		2.25	2.5	2.75	V
C_{WD} Current	I_{CWD}	Charging	-9.0	-10	-11	µA
C_{WD} Threshold Voltage	V_{TL}		0.22	0.25	0.28	V
	V_{TH}		2.25	2.5	2.75	V
Max. FLL Oscillator Frequency	f_{OSC}	V_{DD} = 5.0 V, T_A = 25°C	12	—	—	MHz
I_{OUT}(MAX) Accuracy	—	D3 = 0, D4 = 0	1.0	1.2	1.4	A
		D3 = 0, D4 = 1	0.9	1.0	1.1	A
		D3 = 1, D4 = 0	0.5	0.6	0.7	A
		D3 = 1, D4 = 1	—	250	—	mA
BRAKE Threshold	V_{BRK}		1.5	1.75	2.0	V
BRAKE Hysteresis Current	I_{BRKL}	V_{BRK} = 750 mV	—	20	—	µA
Transconductance Gain	g_m		0.42	0.50	0.58	A/V
Centertap Resistors	R_{CT}		5.0	10	13	kΩ
Back-EMF Hysteresis		V_{BEMF} - V_{CTAP} at	5.0	20	37	mV
		FCOM Transition	-5.0	-20	-37	mV

SERIAL PORT TIMING CONDITIONS



Dwg. WP-019

A. Minimum CHIP SELECT setup time before CLOCK rising edge .... **100 ns**

B. Minimum CHIP SELECT hold time after CLOCK rising edge .... **150 ns**

C. Minimum DATA setup time before CLOCK rising edge .... **150 ns**

D. Minimum DATA hold time after CLOCK rising edge .... **150 ns**

E. Minimum CLOCK low time before CHIP SELECT .... **50 ns**

F. Maximum CLOCK frequency .... **3.3 MHz**

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	LOAD SUPPLY	V_{BB}; the 5 V or 12 V motor supply.
2	C_{D2}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.
3	C_{WD}	Timing capacitor used by the watchdog circuit to disable the back-EMF comparators during commutation transients, and to detect incorrect motor position.
4	C_{ST}	Startup oscillator timing capacitor.
5	OUT_A	Power amplifier A output to motor.
6-7	GROUND	Power and logic ground and thermal heat sink.
8	OUT_B	Power amplifier B output to motor.
9	OUT_C	Power amplifier C output to motor.
10	CENTERTAP	Motor centertap connection for back-EMF detection circuitry.
11	$\overline{\text{BRAKE}}$	Active low turns ON all three sink drivers shorting the motor windings to ground. External capacitor and resistor at BRAKE provide brake delay. The brake function can also be controlled via the serial port.
12	C_{RES}	External reservoir capacitor used to hold charge to drive the source drivers' gates. Also provides power for brake circuit.
13	FILTER	Analog voltage input to control motor current. Also, compensation node for internal speed control loop.
14	SECTOR DATA	External tachometer input. Can use sector or index pulses from disk to provide precise motor speed feedback to internal frequency-locked loop.
15	LOGIC SUPPLY	V_{DD}; the 5 V logic supply.
16	OSCILLATOR	Clock input for the speed reference counter. Typical max. frequency is 10 MHz.
17	DATA OUT	Thermal shutdown indicator, FCOM, TACH, or SYNC signals available in real time, controlled by 2-bit multiplexer in serial port.
18-19	GROUND	Power and logic ground and thermal heat sink.
20	$\overline{\text{RESET}}$	When pulled low forces the chip into sleep mode; clears all serial port bits.
21	$\overline{\text{CHIP SELECT}}$	Strobe input (active low) for data word.
22	CLOCK	Clock input for serial port.
23	DATA IN	Sequential data input for the serial port.
24	C_{D1}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.

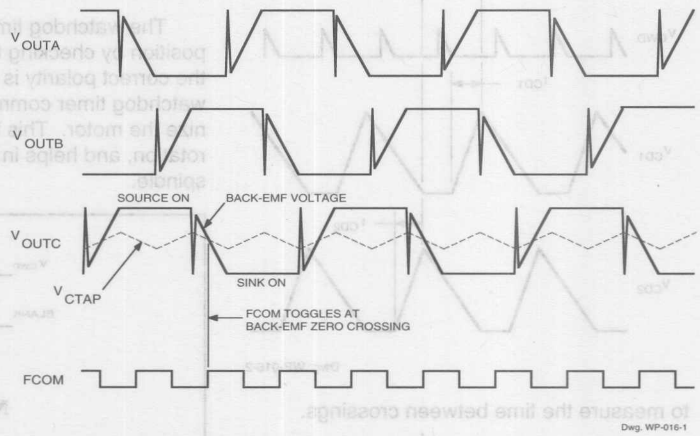
FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8902CLBA are n-channel DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1 Ω. Internal charge pump boost circuitry provides voltage above supply for driving the high-side DMOS gates. Intrinsic ground clamp and flyback diodes provide protection when switching inductive loads and may be used to rectify motor back-EMF in power-down conditions. An external Schottky power diode or pass FET is required in series with the load supply to allow motor back-EMF rectification in power down conditions.

Back-EMF Sensing Motor Startup and Running Algorithm. The A8902CLBA provides a complete self-contained back-EMF sensing startup and running commutation scheme. The three half-bridge outputs are controlled by a state machine. There are six possible combinations. In each state, one output is high (sourcing current), one low (sinking current), and one is OFF (high impedance or 'Z'). Motor back EMF is sensed at the OFF output. The truth table for the output drivers sequencing is:

Sequencer State	OUT_A	OUT_B	OUT_C
1	High	Low	Z
2	Z	Low	High
3	Low	Z	High
4	Low	High	Z
5	Z	High	Low
6	High	Z	Low

At startup, the outputs are enabled in one of the sequencer states shown. The back EMF is examined at the OFF output by comparing the output voltage to the motor centertap voltage at CENTERTAP. The motor will then either step forward, step backward, or remain stationary (if in a null-torque position). If the motor moves, the back-EMF detection circuit waits for the correct polarity back-EMF zero crossing (output crossing through centertap). True back-EMF zero crossings are used by the adaptive commutation delay circuit to advance the state sequencer (commutate) at the proper time to synchronously run the motor. Back-EMF zero crossings are indicated by FCOM, an internal signal that toggles at every zero crossing. FCOM is available at the DATA OUT terminal via the programmable data out multiplexer.

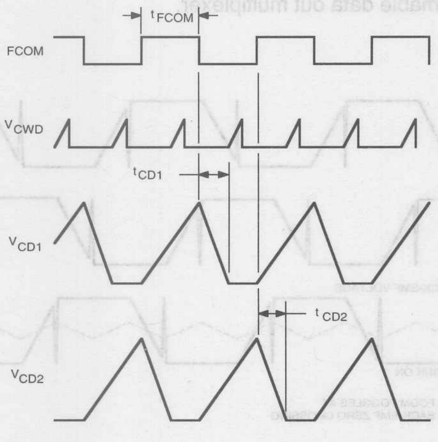


Startup Oscillator. If the motor does not move at the initial startup state, then it is in a null-torque position. In this case, the outputs are commutated automatically by the startup oscillator after a period set by the external capacitor at C_{ST} where

$$t_{CST} = \frac{4(V_{CSTH} - V_{CSTL}) \times C_{ST}}{I_{ST(charge)} + I_{ST(discharge)}}$$

In the next state, the motor will move, back EMF will be detected, and the motor will accelerate synchronously. Once normal synchronous back-EMF commutation occurs, the startup oscillator is defeated by pulses of pulldown current at C_{ST} at each commutation, which prevents C_{ST} from reaching its upper threshold and thus completing a cycle and commutating.

Adaptive Commutation Delay. The adaptive commutation delay circuit uses the back-EMF zero-crossing indicator signal (FCOM) to determine an optimal commutation time for efficient synchronous operation. This circuit commutates the outputs, delayed from the last zero crossing, using two external timing capacitors, C_{D1} and C_{D2},



Dwg. WP-016-2

to measure the time between crossings.

where $t_{CD} = t_{FCOM} \times \dfrac{I_{CD(charge)}}{I_{CD(discharge)}}$

C_{D1} charges up with a fixed current from its 2.5 V reference while FCOM is high. When FCOM goes low at the next zero crossing, C_{D1} is discharged at approximately twice the charging current. When CD_1 reaches the CD threshold, a commutation occurs. C_{D2} operates similarly except on the opposite phase of FCOM. Thus the commutations occur approximately halfway between zero crossings. The actual delay is slightly less than halfway to compensate for electrical delays in the motor, which improves efficiency.

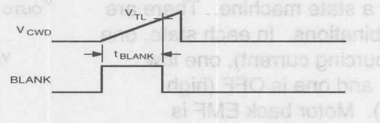
Blanking and Watchdog Timing Functions. The blanking and watchdog timing functions are derived from one timing capacitor, C_{WD}.

where $t_{BLANK} = \dfrac{V_{TL} \times C_{WD}}{I_{CWD}}$

and $t_{WD} = \dfrac{V_{TH} \times C_{WD}}{I_{CWD}}$

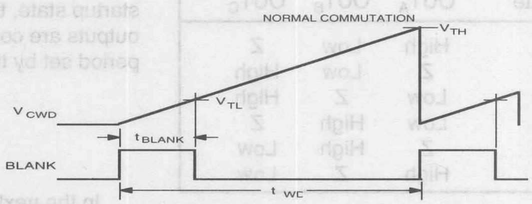
The CWD capacitor begins charging at each commutation, initiating the BLANK signal. BLANK is an internal signal that inhibits the back-EMF comparators during the commutation transients, preventing errors due to inductive recovery and voltage settling transients.

The watchdog timing function allows time to detect correct motor position by checking the back-EMF polarity after each commutation. If the correct polarity is not observed between t_{BLANK} and t_{WD}, then the watchdog timer commutates the outputs to the next state to synchronize the motor. This function is useful in preventing excessive reverse rotation, and helps in resynchronizing (or starting) with a moving spindle.



Dwg. WP-022

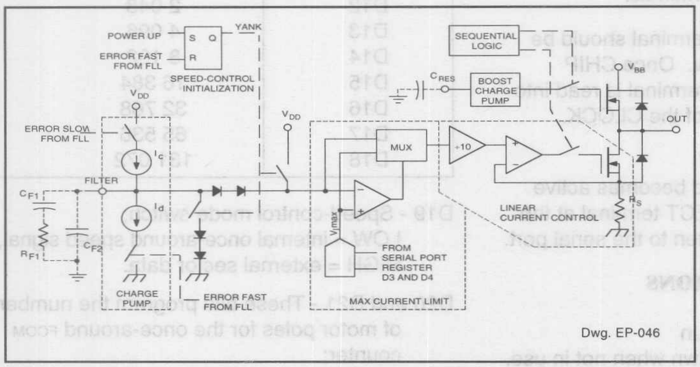
NORMAL COMMUTATION



Dwg. WP-021

WATCHDOG-TRIGGERED COMMUTATION

Current Control. The A8902CLBA provides linear current control via the FILTER terminal, an analog voltage input. Maximum current limit is also provided, and is controlled in four steps via the serial port. Output current is sensed via an internal sense resistor (R_S). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER terminal less the filter threshold voltage, or to the maximum current limit reference, whichever is lower. This transconductance function is $I_{OUT} = (V_{FILTER} - V_{FILTERTH}) / 10R_S$, where R_S is nominally 0.2 Ω and $V_{FILTERTH}$ is approximately 1.85 V.

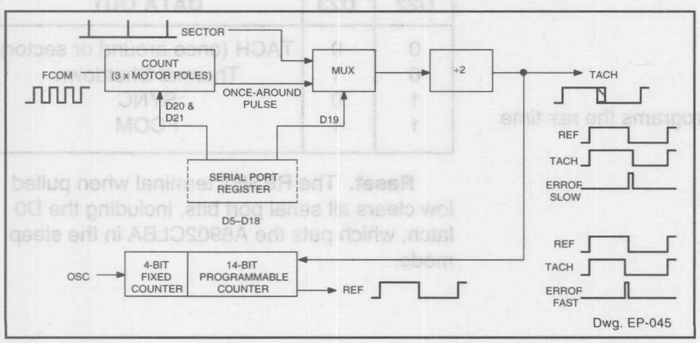


Speed Control. The A8902CLBA includes a frequency-locked loop speed control system. This system monitors motor speed via internal or external digital tachometer signals, generates a precision speed reference, determines the digital speed error, and corrects the motor current via an internal charge pump and external filtering components on the FILTER terminal.

A once per revolution TACH signal can be generated by counting cycles of FCOM (the number of motor poles must be selected via the serial port). TACH is then a jitter-free signal that toggles once per motor revolution. The rising edge of TACH triggers REF, a precision speed reference derived by a programmable counter. The duration of REF is set by programming the counter to count the desired number of OSC cycles

$$\text{desired total count} = \frac{60 \times f_{OSC}}{\text{desired motor speed (rpm)}}$$

where the total count (number of oscillator cycles) is equal to the sum of the selected (programmed low) count numbers corresponding to bits D5 through D18.



The speed error is detected as the difference in falling edges of TACH and REF. The speed error signals control the error-correcting charge pump on the FILTER terminal, which drive the external loop compensation components to correct the motor current.

Sector Mode. An external tachometer signal, such as sector or index pulses, may be used to create the TACH signal, rather than the internally derived once around. To use this mode, the signal is input to the SECTOR terminal, and the sector mode must be enabled via the serial port. When Switching from the once-around mode to sector mode, it is important to monitor the SYNC signal on DATA OUT, and switch modes only when SYNC is low. This ensures making the transition without disturbing the speed control loop. The speed reference counter should be reprogrammed at the same time.

Speed Loop Initialization (YANK). To improve the acquire time of the speed control loop, there is an automatic feature controlled by an internal YANK signal. The motor is started at the maximized programmed current by bypassing the FILTER terminal. The FILTER terminal is clamped to an internal reference (the filter threshold voltage), initializing it near the closed loop operating point. YANK is enabled at startup and stays high until the desired speed is reached. Once the first error-fast occurs, indicating the motor crossed through the

desired speed, YANK goes low. This releases the clamp on the FILTER terminal and current control is returned to FILTER. This feature optimizes speed acquire and minimizes settling. The Current Control Block Diagram illustrates the YANK signal and its effects.

Serial Port. The serial port functions to write various operational and diagnostic modes to the A8902CLBA. The serial port DATA IN is enabled/disabled by the CHIP SELECT terminal. When CHIP SELECT is high the serial port is disabled and the chip is not affected by changes in data at the DATA IN or CLOCK terminals.

To write data to the serial port, the CLOCK terminal should be low prior to the CHIP SELECT terminal going low. Once CHIP SELECT goes low, information on the DATA IN terminal is read into the shift register on the positive-going transition of the CLOCK. There are 24 bits in the serial input port.

Data written into the serial port is latched and becomes active upon the low-to-high transition of the CHIP SELECT terminal at the end of the write cycle. D0 will be the last bit written to the serial port.

SERIAL PORT BIT DEFINITIONS

D0 - Sleep/Run Mode; LOW = Sleep, HIGH = Run
This bit allows the device to be powered down when not in use.

D1 - Step Mode; LOW = Normal Operation, HIGH = Step Only
When in the step-only mode the back-EMF commutation circuitry is disabled and the power outputs are commutated by the start-up oscillator. This mode is intended for device and system testing.

D2 - Brake; LOW = Run, HIGH = Brake.

D3 and D4 - These two bits set the output current limit:

D3	D4	Current Limit
0	0	1.2 A
0	1	1 A
1	0	600 mA
1	1	250 mA

D5 thru D18 - This 14-bit word (active low) programs the REF time to set desired motor speed.

Bit Number	Count Number
D5	16
D6	32
D7	64
D8	128
D9	256
D10	512
D11	1 024
D12	2 048
D13	4 096
D14	8 192
D15	16 384
D16	32 768
D17	65 536
D18	131 072

D19 - Speed-control mode switch;
LOW = internal once-around speed signal,
HIGH = external sector data.

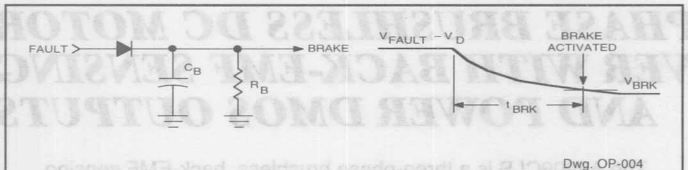
D20 and D21 - These bits program the number of motor poles for the once-around FCOM counter:

D20	D21	Motor Poles
0	0	8
0	1	–
1	0	16
1	1	12

D22 and D23 - Controls the multiplexer for DATA OUT:

D22	D23	DATA OUT
0	0	TACH (once around or sector)
0	1	Thermal Shutdown
1	0	SYNC
1	1	FCOM

Reset. The RESET terminal when pulled low clears all serial port bits, including the D0 latch, which puts the A8902CLBA in the sleep mode.



Dwg. OP-004

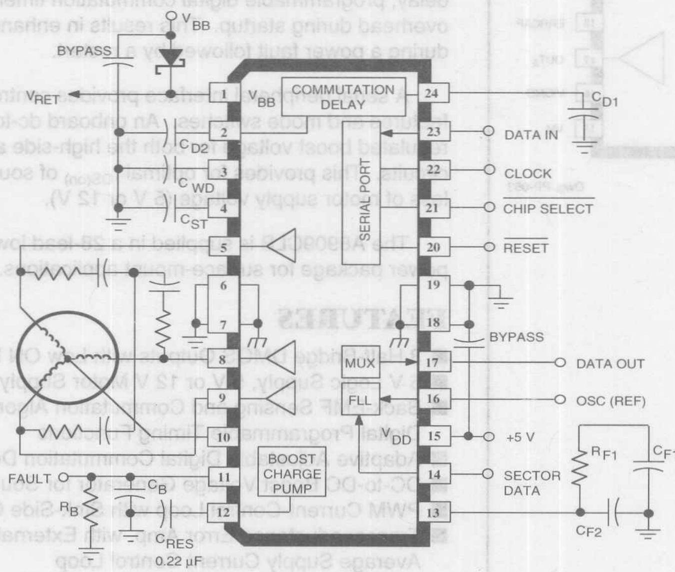
Braking. A dynamic braking feature of the A8902CLBA shorts the three motor windings to ground. This is accomplished by turning the three source drivers OFF and the three sink drivers ON. Activation of the brake can be implemented through the BRAKE input or through the D2 bit in the serial port. The supply voltage for the brake circuitry is the C_{RES} voltage, allowing the brake function to remain active after power failure. Power-down braking with delay can be implemented by using an external RC and other components to control the brake terminal, as shown. Brake delay can be set using the equation below to ensure that voice-coil head retract occurs before the spindle motor brake is activated. Once the brake is activated, due to the inherent capacitive input, the three sink drivers will remain active until the device is reset.

$$t_{BRK} = R_B C_B \left(1 - l_n \frac{V_{BRK}}{V_{FAULT} - V_D}\right)$$

Centertap. The A8902CLBA internally simulates the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Applications information regarding the selection of external component values is available from the factory for external component selection, frequency-locked loop speed control, and commutation delay capacitor selection.

TYPICAL APPLICATION

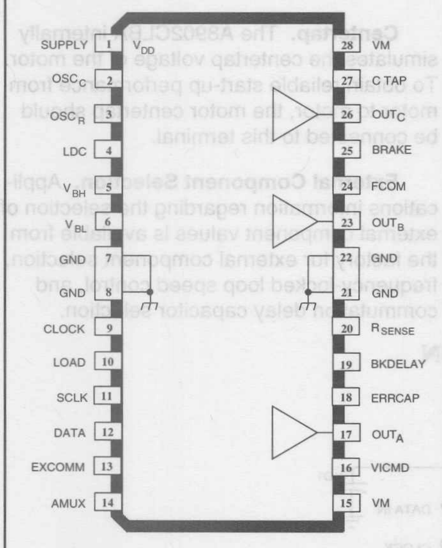


Dwg. EP-036C

8909

26301.10

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING AND POWER DMOS OUTPUTS



Dwg. PP-063

The A8909CLB is a three-phase brushless, back-EMF sensing, spindle-motor driver that integrates analog bipolar, analog and digital CMOS control functions, and DMOS power outputs on a single monolithic chip. It provides complete back-EMF sensing, commutation control, and drive of a spindle motor, and provides for an orderly spin-down in the event of supply-voltage removal. Energy for retracting the heads is regenerated from the spinning motor, while a controlled delay allows for a full retract before dynamic braking. The pulse-width modulation system and power DMOS outputs provide control of high currents with minimum power dissipation in the chip, and minimal average power supply currrent.

The internal sensorless commutation algorithm is based on earlier Allegro back-EMF sensing spindle-motor driver products that have proven capability. This system features digital adaptive commutation delay, programmable digital commutation timers, and minimal micro overhead during startup. This results in enhanced resynchronization during a power fault followed by a restart.

A serial peripheral interface provides control of programmable features and mode switches. An onboard dc-to-dc converter provides regulated boost voltage for both the high-side and sink-side gate-drive circuits. This provides for optimal $r_{DS(on)}$ of sources and sinks, regardless of motor supply voltage (5 V or 12 V).

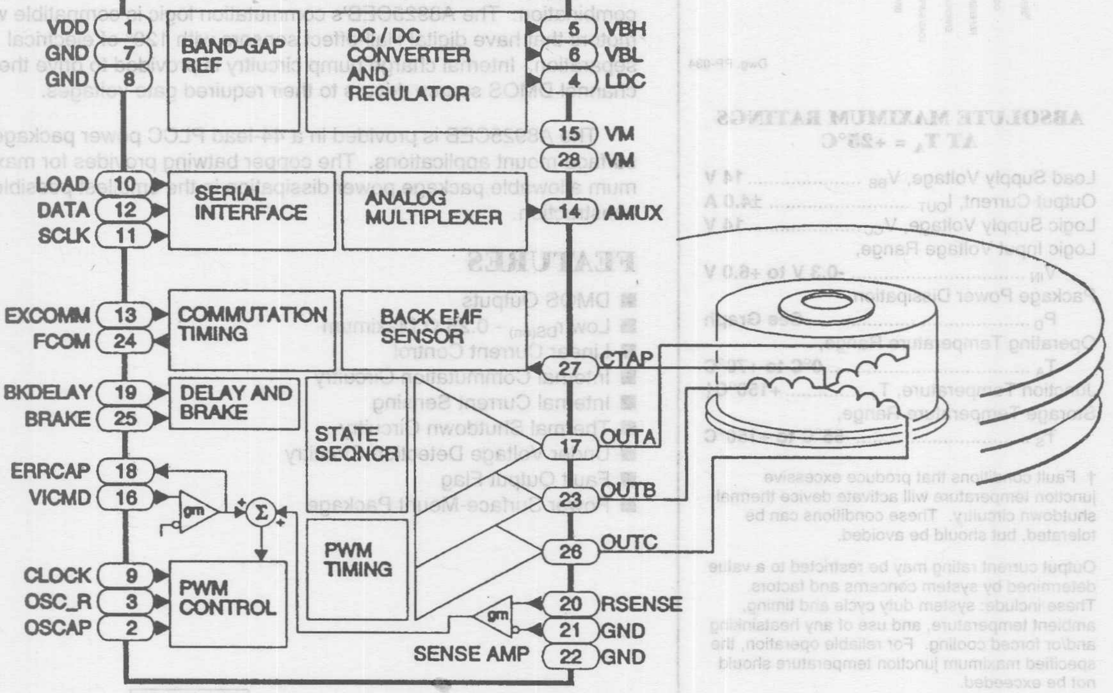
The A8909CLB is supplied in a 28-lead low-profile SOIC batwing power package for surface-mount applications.

FEATURES

- 3 Half-Bridge DMOS Outputs with Low ON Resistance
- 5 V Logic Supply, 5 V or 12 V Motor Supply
- Back-EMF Sensing and Commutation Algorithm with Digital Programmable Timing Functions
- Adaptive Adjustable Digital Commutation Delay
- DC-to-DC Boost Voltage Generator for Source and Sink Gate Drive
- PWM Current-Control Loop with Sink-Side Chopping
- Transconductance Error Amp. with External Compensation for Average Supply Current Control Loop
- PWM Oscillator with External Frequency-Setting Components
- Current-Sense Amplifier
- Power-Down Brake with Delay Set by External RC
- Analog/Digital Multiplexer for Diagnostics and Testing
- Thermal Monitor Voltage Available on Multiplexer

8909
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING AND POWER DMOS OUTPUTS

- Back-EMF Zero-Crossing Output for Monitoring Motor Speed
- Sleep Mode
- Serial Port for Programming Modes, Multiplexer, & Programmable Timers



Dwg. FP-040

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8925

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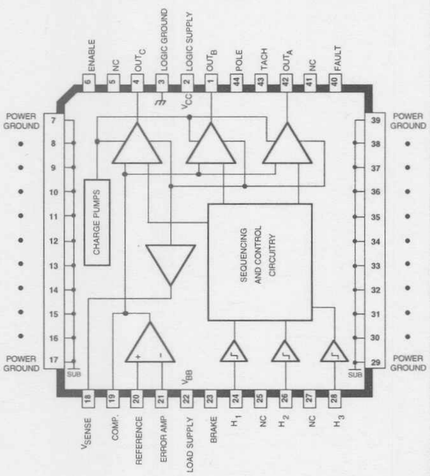
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/ DRIVER WITH LINEAR CURRENT CONTROL AND POWER DMOS OUTPUTS



Dwg. PP-034

The A8925CEB is a DMOS three-phase brushless dc motor controller/driver designed for use in Winchester disk drives and other data storage applications. The power output stages are capable of ±4 A output currents and have DMOS power outputs with less than 0.25 Ω $r_{DS(on)}$ for low power dissipation. Intrinsic ground clamp and flyback diodes protect the output drivers when switching inductive loads. Thermal shutdown circuitry is provided to protect the device from excessive junction temperature.

A transconductance amplifier is used to linearly regulate the load current and control motor speed. Internal current-sensing circuitry eliminates the need for external sense resistors. Analog and digital control circuitry provide complete sequencing of the output drivers as well as providing brake, disable, and tachometer functions. A FAULT output flag indicates the presence of an under-voltage condition on the 12 V supply, excessive junction temperature, or an invalid Hall input combination. The A8925CEB's commutation logic is compatible with motors that have digital Hall-effect sensors with 120° of electrical separation. Internal charge pump circuitry is provided to drive the N-channel DMOS source drivers to their required gate voltages.

The A8925CEB is provided in a 44-lead PLCC power package for surface-mount applications. The copper batwing provides for maximum allowable package power dissipation in the smallest possible construction.

ABSOLUTE MAXIMUM RATINGS AT T_A = +25°C

Load Supply Voltage, V_{BB} .... **14 V**
Output Current, I_{OUT} .... **±4.0 A**
Logic Supply Voltage, V_{CC} .... **14 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +6.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **0°C to +70°C**
Junction Temperature, T_J .... **+150°C†**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

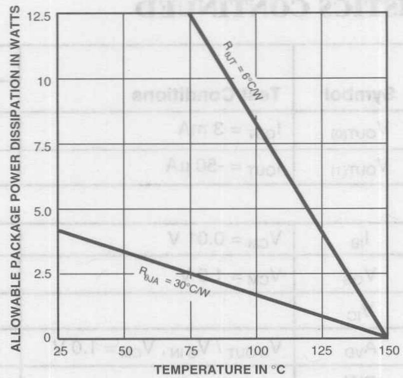
† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$ - 0.25 Ω Maximum
- Linear Current Control
- Internal Commutation Circuitry
- Internal Current Sensing
- Thermal Shutdown Circuitry
- Under Voltage Detection Circuitry
- Fault Output Flag
- Power Surface-Mount Package

Always order by complete part number: **A8925CEB** .



Dwg. GP-020B

ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Logic Supply Voltage	V_{CC}	Operating	10	12	14	V
Load Supply Voltage	V_{BB}	Operating	10	12	14	V
Supply Current	I_{CC}	Operating	—	30	50	mA
		V_{ENABLE} = 0 V	—	2.0	4.0	mA
Thermal Shutdown	T_J		—	165	—	°C
Output Drivers						
Output ON Resistance	$r_{DS(on)}$	I_{OUT} = ±4.0 A, Pulse Test	—	0.20	0.25	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	I_{OUT} = 4.0 A, L = 2 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = ±4.0 A	—	1.5	2.0	V
Output Leakage Current	I_{DSX}	V_{OUT} = 14 V	—	10	300	µA
		V_{OUT} = 0 V	—	-10	-300	µA
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	ENABLE, POLE	—	—	0.8	V
	$V_{IN(1)}$		2.4	—	—	V
Logic Input Voltage	$V_{IN(0)}$	BRAKE	—	—	0.8	V
	$V_{IN(1)}$		3.0	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	—	-1.0	µA
	$I_{IN(1)}$	V_{IN} = 2.4 V	—	—	1.0	µA

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

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ELECTRICAL CHARACTERISTICS CONTINUED

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Logic Output Voltage (FAULT, TACH)	$V_{OUT(0)}$	I_{OUT} = 3 mA	—	—	0.8	V
	$V_{OUT(1)}$	I_{OUT} = -50 µA	2.0	—	—	V
Error Amplifier						
Input Bias Current	I_{IB}	V_{CM} = 0.01 V	—	5.0	10	µA
Input Offset Voltage	V_{OS}	V_{CM} = 1.0 V	—	3.0	5.0	mV
Input Common-Mode Voltage Range	V_{IC}		0.01	—	6.0	V
Error Voltage Gain	A_{VD}	$V_{S\,OUT}$ / $V_{S\,IN}$, V_{CM} = 1.0 V	—	80	—	dB
Unity Gain Bandwidth	BW		—	1.0	—	MHz
Common-Mode Rejection Ratio	CMRR		—	80	—	dB
Power Supply Rejection Ratio	PSRR		—	50	—	dB
Miscellaneous						
Current Sense Gain	A_{ICS}	I_{OUT} = -1.0 A	1/1k	1/1.2k	1/1.4k	—
Current-Sense Matching	—	I_{OUT} = -1.0 A	—	±3.0	±5.0	%
Under-Voltage Trip Point	V_{CC}		8.0	—	9.5	V
Hall Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	-500	-1000	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	-250	-500	µA
Hall Input Threshold	V_{IN}		—	3.8	—	V
Hall Input Pull-Up Resistance	R_{PU}		—	25	—	kΩ

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

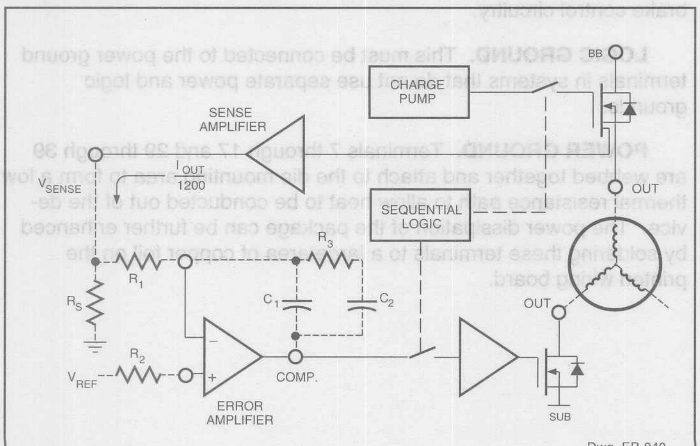
COMMUTATION TRUTH TABLE

Hall Sensor Inputs H_1	H_2	H_3	ENABLE	BRAKE	FAULT	Outputs OUT_A	OUT_B	OUT_C
High	Low	High	High	High	High	High	Low	Z
High	Low	Low	High	High	High	High	Z	Low
High	High	Low	High	High	High	Z	High	Low
Low	High	Low	High	High	High	Low	High	Z
Low	High	High	High	High	High	Low	Z	High
Low	Low	High	High	High	High	Z	Low	High
High	High	High	High	High	Low	Z	Z	Z
Low	Low	Low	High	High	Low	Z	Z	Z
X	X	X	Low	High	X	Z	Z	Z
X	X	X	X	Low	X	Low	Low	Low

X = Irrelevant
Z = High Impedance

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	OUT_B	Power DMOS output.
2	LOGIC SUPPLY	V_{CC}; low-current 12 V supply for the logic.
3	LOGIC GROUND	Low-level logic ground.
4	OUT_C	Power DMOS output.
6	ENABLE	Active high chip enable.
7–17	POWER GROUND	Power ground and thermal heat sink.
18	V_{SENSE}	External precision resistor for sense-FET current.
19	COMP.	Compensation; error amplifier output.
20	REFERENCE	V_{REF}; voltage input that sets the power output current.
21	ERROR AMP.	Input that controls the current in the load.
22	LOAD SUPPLY	V_{BB}; high-current 12 V supply for the voice-coil motor.
23	$\overline{BRAKE}$	A logic low turns OFF all source drivers and turns ON all sink drivers (shorts the windings to ground).
24	H_1	High-level input from a Hall sensor.
26	H_2	High-level input from a Hall sensor.
28	H_3	High-level input from a Hall sensor.
29–39	POWER GROUND	Power ground and thermal heat sink.
40	FAULT	A logic low at this output indicates a thermal shutdown, under -voltage fault, or an invalid Hall input combination.
42	OUT_A	Power DMOS output.
43	TACH	Speed reference output; the H_1 Hall input divided by the number of motor poles.
44	POLE	Designates four- or eight-pole motor; Low = 4 pole, High = 8 pole.



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FUNCTIONAL DESCRIPTION

Power Outputs (OUT_A, OUT_B, and OUT_C). The power outputs of the A8925CEB are DMOS transistors with a maximum $r_{DS(on)}$ of 0.25 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages.

Current Control. Current in the load is monitored by an internal sense amplifier that produces an output current that is approximately one twelve hundredth that of the load current (see Figure). This current is output to the V_{SENSE} terminal and develops a voltage

Continued next page...

across R_S that equals $R_S \bullet I_{LOAD}/1200$. This sense voltage ($V_{SENSE}$) is compared to a reference voltage (V_{REF}) and an error voltage is developed that is gated in by the sequential control logic to drive the gate of the appropriate output sink transistor. A transconductance control function is thus realized where $I_{OUT} = V_{REF} \bullet 1200/R_S$. External components C_1, C_2, R_1, R_2, and R_3 are compensation components used to obtain optimal response and settling of the current control loop. Information on how to select these components is available.

FAULT. The FAULT terminal when low indicates the presence of one of three fault conditions:

A) An under-voltage condition on the logic supply. The trip point for this function is between 8 and 9.5 volts.

B) An invalid Hall input combination … all inputs High or all inputs Low.

C) An excessive device junction temperature. The thermal shutdown circuitry disables the output drivers in addition to forcing the FAULT output signal low.

TACH and POLE. In order to develop a low-jitter tachometer signal (TACH) for use in controlling motor speed, the A8925CEB divides the frequency of the H_1 input by the number of poles in the motor. This eliminates the jitter caused by variations in Hall-effect device placement , sensitivity, and magnet strengths by always changing state when looking at the same magnet/sensor pair. The resulting TACH signal changes state every mechanical revolution of the motor. The POLE input sets the TACH signal for four-pole motors when Low or eight-pole motors when High.

HALL INPUTS (H_1, H_2, H_3). The A8925CEB is configured for use with open-collector Hall-effect devices. Internal 25 kΩ pull up resistors to 10 volts are connected to these inputs.

ENABLE. The ENABLE terminal when Low puts the device in a low current consumption, power-down mode. When ENABLE is High the device is active.

BRAKE. When the BRAKE input goes Low the output source drivers are disabled and the gates of the sink drivers are pulled high and left floating. This achieves optimum passive braking performance since the sink power DMOS output drivers are ON until the motor has fully completed braking. The braking control circuitry operates off the load supply (V_{BB}) to allow it to remain operational during power loss by using the back-EMF voltage of the motor as it's supply.

LOAD SUPPLY (V_{BB}). This terminal is the power supply connection for the power output drivers and braking control circuitry. This terminal should be decoupled with a large-value capacitor to absorb load currents dumped back into the supply during the de-energization of motor windings. These currents can cause the supply voltage to exceed the maximum voltage rating of the device if not properly decoupled. The intrinsic ground clamp and flyback diodes will rectify the motor's back-EMF voltage during power loss. In applications were use of the motor's back-EMF voltage is desired a series diode should be used to isolate this terminal from the logic supply (V_{CC}). This is to avoid dumping the charge back into the supply and therefor clamping the voltage available from rectification of the motor's back-EMF voltage.

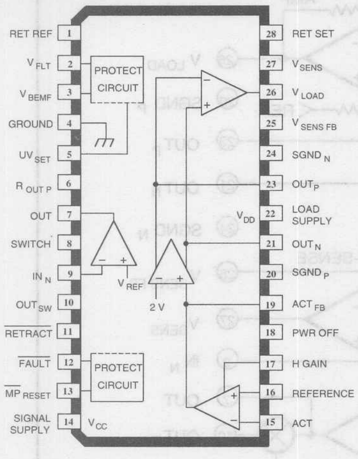
LOGIC SUPPLY (V_{CC}). This is the 12 volt supply terminal for the A8925CEB and powers all circuitry except the power outputs and brake control circuitry.

LOGIC GROUND. This must be connected to the power ground terminals in systems that do not use separate power and logic grounds.

POWER GROUND. Terminals 7 through 17 and 29 through 39 are webbed together and attach to the die mounting area to form a low thermal resistance path to allow heat to be conducted out of the device. The power dissipation of the package can be further enhanced by soldering these terminals to a large area of copper foil on the printed wiring board.

8932-A

VOICE COIL MOTOR DRIVER



Dwg. PP-042B

ABSOLUTE MAXIMUM RATINGS

Supply Voltages, V_{CC} and V_{DD} .... **6.0 V**
Output Current, I_{OUT} (peak) .... **±600 mA**
(continuous) .... **±500 mA**
Analog Input Voltage Range,
V_{IN} .... **-0.3 V to V_{CC}**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +6.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **0°C to +70°C**
Junction Temperature, T_J .... **+150°C†**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation the specified maximum junction temperature should not be exceeded.

Providing control and drive of the voice coil motor used for head positioning in 5 V disk drive applications, the second-generation A8932CLWA is a full-bridge driver which can be configured so that its output current is a direct function of an externally applied control voltage or current. This linear current control function is supplemented by additional circuitry to protect the heads and the data disk during system failure or normal system shutdown.

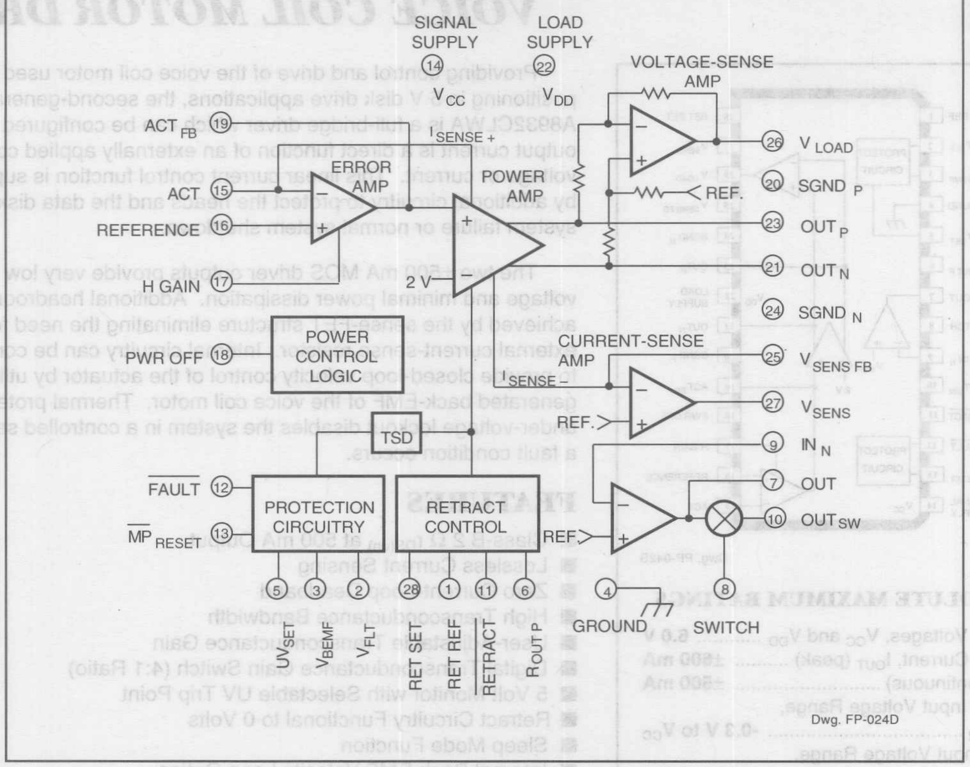
The two ±500 mA MOS driver outputs provide very low saturation voltage and minimal power dissipation. Additional headroom is achieved by the sense-FET structure eliminating the need for an external current-sense resistor. Internal circuitry can be configured to provide closed-loop velocity control of the actuator by utilizing the generated back-EMF of the voice coil motor. Thermal protection and under-voltage lockout disables the system in a controlled sequence if a fault condition occurs.

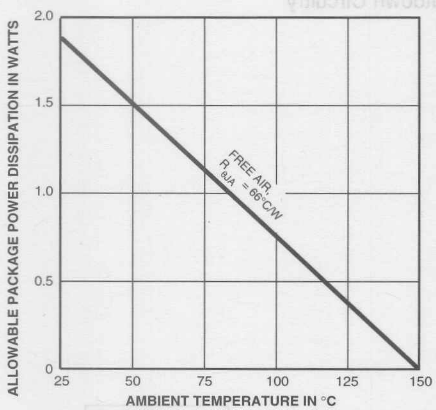
FEATURES

- Class-B 2 Ω $r_{DS(on)}$ at 500 mA Output
- Lossless Current Sensing
- Zero Current-Loop Deadband
- High Transconductance Bandwidth
- User-Adjustable Transconductance Gain
- Digital Transconductance Gain Switch (4:1 Ratio)
- 5 Volt Monitor with Selectable UV Trip Point
- Retract Circuitry Functional to 0 Volts
- Sleep Mode Function
- Internal Back-EMF Velocity Loop Option
- Internal Thermal Shutdown Circuitry

Always order by complete part number, e.g., A8932CLWA .

FUNCTIONAL BLOCK DIAGRAM





ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{DD} = 5.0 V, V_{REF} = V_{IN} = 2.0 V, Load = 150 μH/3.5 Ω (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Error Amplifier						
Input Offset Voltage	V_{IO}	I_{LOAD} = 0 mA	—	—	±50	mV
Current Gain	A_{iH}	H GAIN ≥ 3.5 V	7200	8000	8800	—
	A_{iL}	H GAIN ≤ 0.7 V	1800	2000	2200	—
Current Gain Linearity	$E_{L(adj)}$	I_{OUT} = 5 mA to 500 mA, A_i = A_{iL}	—	—	±10	%
		I_{OUT} = 5 mA to 500 mA, A_i = A_{iH}	—	—	±10	%
Reference Voltage Range	V_{REF}		1.5	—	2.5	V
Voltage-Sense Amplifier						
Voltage Gain	A_{VD}		0.36	0.40	0.44	—
Output Offset Voltage	V_{OO}	I_{LOAD} = 0 mA	—	—	±25	mV
Current-Sense Amplifier						
Amplifier Error	E_{VD}	$(R_s \times I_{LOAD} / (A_i \times V_{SENSE})) - 1$	—	1.0	—	
Input Offset Voltage	V_{IO}	I_{LOAD} = 0 mA, A_i = A_{iL}	—	—	±25	mV
Output Drivers						
Total ON Resistance	$r_{DS(on)}$	I_{LOAD} = 100 mA	—	2.0	2.5	Ω
(Source + Sink)		I_{LOAD} = 500 mA	—	2.0	2.5	Ω
Retract Output Voltage Error	$E_{OUT(PN)}$	$V_{OUT(P)} - V_{OUT(N)} - V_{RETSET}$			±100	mV
Full Power Bandwidth	BW	-3 dB	1.0	—	—	kHz
Uncommitted Op Amp						
Voltage Gain	A_{VS}		—	91	—	dB
Unity Gain Bandwidth	BW		—	1.0	—	MHz
Max. Load Capacitance	C_{LOAD}		—	40	—	pF
Slew Rate	SR		—	4.2	—	V/μs
Output Voltage	V_O	V_{SWITCH} ≤ 0.7 V	2.5	—	3.5	V
	V_{OSW}	V_{SWITCH} ≥ 3.5 V	2.5	—	3.5	V
Max. Output Current	I_O		—	±250	—	μA
Input Offset Voltage	V_{IO}		—	<±10	—	mV

Negative current is defined as coming out of (sourcing) the specified device terminal.
Typical Data is for design information only.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{DD} = 5.0 V, V_{REF} = V_{IN} = 2.0 V, Load = 150 μH/3.5 Ω (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Miscellaneous						
Supply Voltage	V_{CC}	Operating	4.5	5.0	5.5	V
	V_{DD}	Operating	4.5	5.0	5.5	V
Under-Voltage Lockout Voltage	V_{CC}	$V_{CC} = V_{DD}$	3.9	4.2	4.35	V
Fault Logic Output	V_{FAULT}	$V_{RETRACT} \geq 3.5$ V	—	—	500	mV
		$V_{RETRACT} \leq 0.7$ V	4.5	—	—	V
	I_{FAULT}	V_{FLT} = 2.25 V	—	>20	—	μA
Power-On Reset	$V_{MPRESET}$	$V_{RETRACT} \geq 3.5$ V	4.5	—	—	V
		$V_{RETRACT} \leq 0.7$ V, I_{MPREST} = 1.5 mA	—	—	800	mV
Total Supply Current	$I_{CC} + I_{DD}$	Outputs Balanced, No Load	—	—	10	mA
		Sleep Mode, PWR OFF = V_{CC}	—	—	2.0	mA
Logic Input Voltage	$V_{IN(0)}$		—	—	0.7	V
	$V_{IN(1)}$		3.5			V
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C

Negative current is defined as coming out of (sourcing) the specified device terminal.
Typical Data is for design information only.

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	RET REF	The reference supply for setting the voltage across the load during retract.
2	V_{FLT}	Reservoir (energy storage) capacitor used to operate fault circuitry.
3	V_{BEMF}	Back-EMF voltage from spindle motor used to retract heads during loss of power.
4	GROUND	Circuit reference.
5	UV_{SET}	Under-voltage trip point reference input. Set internally to 4.2 V but may be overridden by external resistor divider. (Equation 4).
6	$R_{OUT\ P}$	Source driver used for retract; externally connected to OUT_P.
7	OUT	Output of uncommitted operational amplifier.
8	SWITCH	Logic input for transmission gate; a high level connects OUT to OUT_{SW}.
9	IN_N	Inverting input to uncommitted operational amplifier.
10	OUT_{SW}	Transmission-gated output of uncommitted operational amplifier.
11	RETRACT	An active-low logic input that initiates the retract sequence.
12	FAULT	A logic low at this MOS output indicates a thermal shutdown, under-voltage fault, or retract command.
13	MP_{RESET}	(Power-On Reset) A logic low at this open-collector output may be used to reset the system on under-voltage fault or power ON.
14	SIGNAL SUPPLY	V_{CC}; low-current supply voltage in the range of 4.5 V to 5.5 V.
15	ACT	Input which controls the current in the load. Transconductance gain is set with an external resistor in series with this input (Equation 1).
16	REFERENCE	V_{REF}; reference input for all amplifiers; ac ground.
17	H GAIN	Logic input to switch the error amplifier transconductance gain: LOW = 2000, HIGH = 8000.
18	PWR OFF	An active-high logic input that puts the device in a “sleep mode”. All fault circuitry remains active.
19	ACT_{FB}	Input connection for feedback network which sets the error amplifier gain and bandwidth.
20	$SGND_P$	Power ground for the OUT_P sink driver.
21	OUT_N	Power output. Sinks current when $V_{ACT} < V_{REF}$.
22	LOAD SUPPLY	V_{DD}; high-current supply voltage for the voice-coil motor.
23	OUT_P	Power output. Sinks current when $V_{ACT} > V_{REF}$.

TERMINAL FUNCTIONS (cont'd)

Term.	Terminal Name	Function
24	$SGND_N$	Power ground for the OUT_N sink driver.
25	$V_{SENS\ FB}$	Input connection for feedback network which sets the current-sense amplifier gain and bandwidth. Also called gm SET.
26	V_{LOAD}	An output voltage proportional to the load voltage. Used in conjunction with closed-loop velocity control.
27	V_{SENS}	Voltage output representing load current (Equation 2). Also called MONITOR.
28	RET SET	An external resistor divider to set the retract voltage across the load. Used in conjunction with $V_{RET\text{-}REF}$ (Equation 3).

DEVICE DESCRIPTION

Current Amplifier. The A8932CLWA voice coil motor driver features a wide transconductance bandwidth and minimal crossover distortion. The transconductance gain is user selectable:

$$g_m = \frac{A_i}{R_{gm}} \quad \text{(Equation 1)}$$

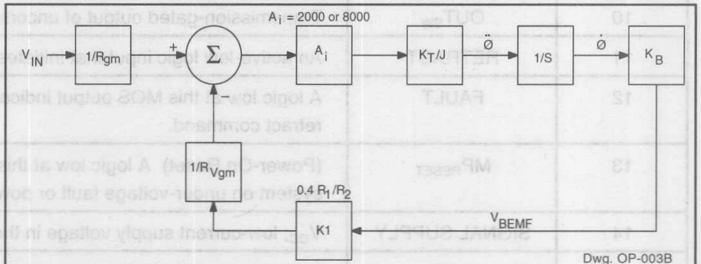
where A_i is either 2000 (H GAIN = Low) or 8000 (H GAIN = High)

The error amplifier's bandwidth and load compensation zero are set utilizing external resistor and capacitor feedback components around the amplifier.

The actuator main loop compensation can be set by applying a square wave and adjusting R_Z and C_Z for optimum response.

Current and Voltage Sensing. The load current is sensed internally. Three auxiliary amplifiers are also included to allow various control functions to be implemented. The first of these amplifiers provides a voltage output that is proportional to the load current:

$$V_{SENSE} = \frac{R_S\ I_{LOAD}}{A_i} \quad \text{(Equation 2)}$$



Dwg. OP-003B

The second and third auxiliary amplifiers may be used in conjunction with the first to provide a closed-loop velocity control system for the actuator arm during a controlled retract for head parking. This is achieved by determining the back-EMF voltage generated by the voice coil and feeding back this information to the main actuator control input. The back-EMF feedback voltage can be switched in as required by means of the SWITCH logic input.

The back-EMF voltage represents the velocity of the actuator. By subtracting the $I_{LOAD}R_{LOAD}$ voltage component from the voltage across the load, the back-EMF term can be isolated and fed back to close a velocity control loop.

The amplifier output voltage V_{LOAD} is proportional to the voltage across the load ($A_{VD}(V_{OUTN} - V_{OUTP})$). R_S is selected so that V_{SENSE} represents I_{LOAD} while R_3 is dependent on R_{LOAD} as shown in the following equations:

$$V_{LOAD} = -A_{VD}\ ((I_{LOAD}\ R_{LOAD}) + V_{BEMF})$$

$$V_{SENSE} = R_S\, I_{LOAD}/A_{iL}$$

where A_i = 2000 (H GAIN = logic Low)

$$OUT_{SW} = 0.4\,(V_{BEMF}\, R_1/R_2)$$

$$R_3 = \frac{R_2\, R_S}{0.4\, A_i\, R_{LOAD}}$$

$$\frac{V_{BEMF}}{V_{IN}} = \frac{R_2\, R_{Vgm}}{0.4\, R_{gm}\, R_1}$$

$$BW = 0.4\,\frac{R_1\, K_B\, K_T\, A_i}{2\pi\, R_{VGM}\, R_2\, J}$$

where J is the moment of inertia, K_B is the back-EMF motor constant, and K_T is the torque constant.

Velocity loop compensation = $L_{LOAD}/R_{LOAD} = R_1\, C_1 = R_3\, C_2$

Retract and Brake. A retract-brake sequence is initiated on receiving a fault indication from the internal thermal shutdown (TSD), or under-voltage lockout (UVLO), or an externally applied logic High at the RETRACT input.

If the velocity control scheme is implemented, the head can be retracted under the full control of V_{IN} in conjunction with OUT_{SW} back-EMF voltage if no fault condition exists. If a fault condition were to occur however, the retract velocity would be controlled by applying a constant user-defined voltage across the load:

$$V_{RET\text{-}SET} = \frac{2\, R_8}{1000 + R_7 + R_8} \qquad \text{(Equation 3)}$$

where $R_7 + R_8 >> 1000\ \Omega$.

When the sequence is operated, the output voltage is forced to approximately $V_{RET\text{-}SET}$ to retract the heads, and then a fault command ("brake") is sent to the spindle motor driver. The user determines the total time for the retract sequence, before the spindle brake is enabled, by the choice of an external resistor and capacitor at the FAULT output.

Power for the retract function is provided by the rectified back EMF of the spindle motor by way of the V_{BEMF} terminal. The A8932CLWA will perform the retract function under low supply conditions (nominally down to 2 V). Operation down to almost 0 V requires an energy-storage capacitor at the V_{FLT} terminal.

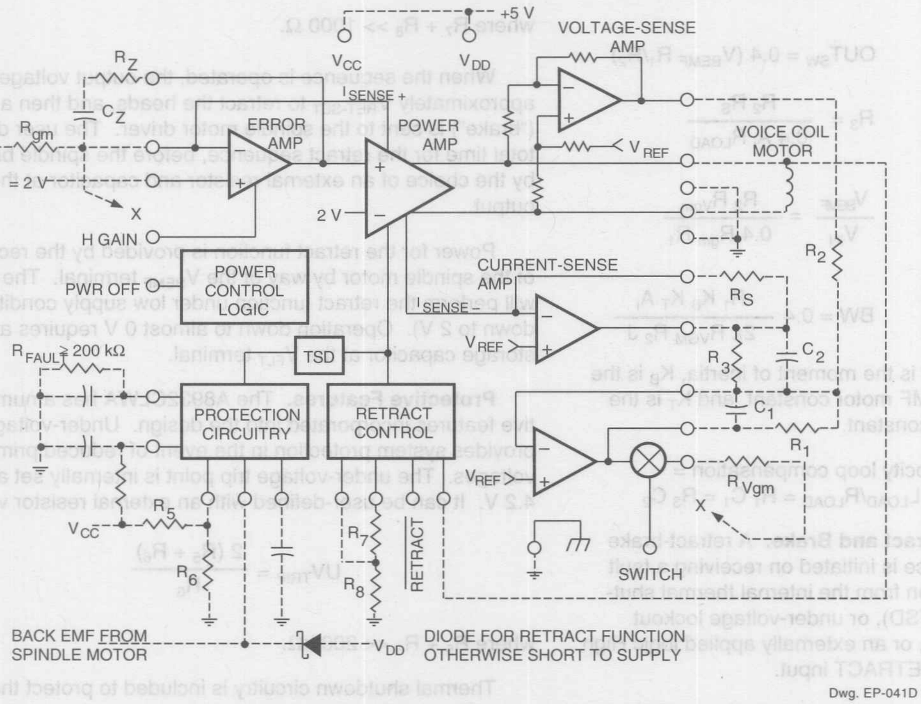
Protective Features. The A8932CLWA has a number of protective features incorporated into the design. Under-voltage lockout provides system protection in the event of reduced primary supply voltages. The under-voltage trip point is internally set at approximately 4.2 V. It can be user-defined with an external resistor voltage divider:

$$UV_{TRIP} = \frac{2\,(R_5 + R_6)}{R_6} \qquad \text{(Equation 4)}$$

where $R_5 + R_6 << 200\ k\Omega$.

Thermal shutdown circuitry is included to protect the device from excessive junction temperature. It is only intended to protect the chip from catastrophic failures due to excessive junction temperature.

TEST CIRCUIT AND TYPICAL APPLICATION

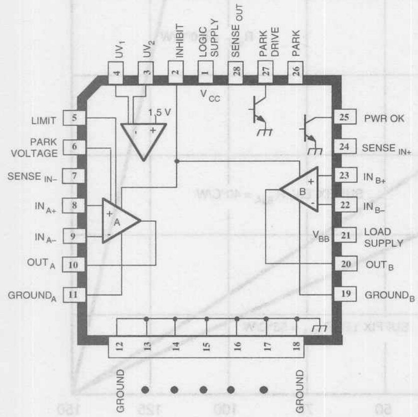


8958

26300.5

VOICE COIL MOTOR DRIVER

A8958CEA



Dwg. PP-038A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Supply Voltages, V_{BB} and V_{CC} .... **16 V**
Output Current, I_{OUT} .... **±1.0 A**
Park Drive Output Current, I_{PARK}
Continuous .... **250 mA**
Peak .... **1.0 A**
Amplifier Input Voltage Range,
V_{IN} .... **-2.0 V to V_{CC}**
Sense Input Voltage Range,
$V_{SENSE\ IN}$ .... **-0.3 V to V_{CC}**
Comparator and Digital Inputs,
V_{IN} .... **-0.3 V to 10 V**
I_{IN} .... **±10 mA**
Power OK Output, V_{CEX} .... **20 V**
I_C .... **30 mA**
Output Clamp Diode Current,
I_F (pulsed) .... **1.0 A**
Package Power Dissipation, P_D . **See Graph**
Operating Temperature Range,
T_A .... **0°C to +70°C**
Junction Temperature, T_J .... **150°C***
Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Providing control and drive of the voice coil motor used for head positioning in disk drive applications, the A8958– is a full-bridge driver which can be configured so that its output current is a direct function of an externally applied control voltage or current. This linear current control function is supplemented by additional circuitry to protect the heads and the data disk during system failure or normal system shutdown.

The two ±800 mA driver outputs provide very-low saturation voltage drops and precise current control utilizing a single current-sensing resistor connected in series with the load. Under-voltage lockout disables the system in a controlled sequence if a fault condition occurs.

When activated by the under-voltage comparator, or a park command, the output power drivers change from a controlled current to a user-determined constant park voltage. Other features include a power ok flag, a limit input to force the outputs to their maximum level in either polarity, an over-riding output disable to shut down both power amplifiers and reduce quiescent supply current, and internal thermal shutdown which disables the load (but still allowing the head to be parked) in the event of excessive junction temperatures. The load is re-enabled when the junction temperature returns to a safe level.

The A8958CEA is supplied in a 28-lead power PLCC for surface-mount applications; the A8958CLB is supplied in a 24-lead power SOIC. The copper half-batwing/batwing construction provides for maximum package power dissipation in a minimum package size. Both are rated for continuous operation over the temperature range of 0°C to +70°C.

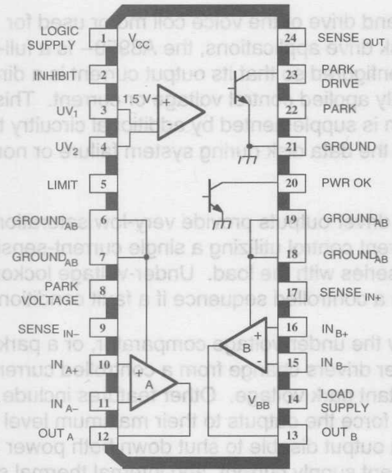
FEATURES

- Controlled-Velocity Head Parking
- Zero Deadband
- High Transconductance Bandwidth
- User-Adjustable Transconductance Gain
- ±800 mA Load Current
- Dual Under-Voltage Monitors with Flag and User-Selectable Trip Points
- Internal Thermal Shutdown Circuitry
- Replaces UC3175

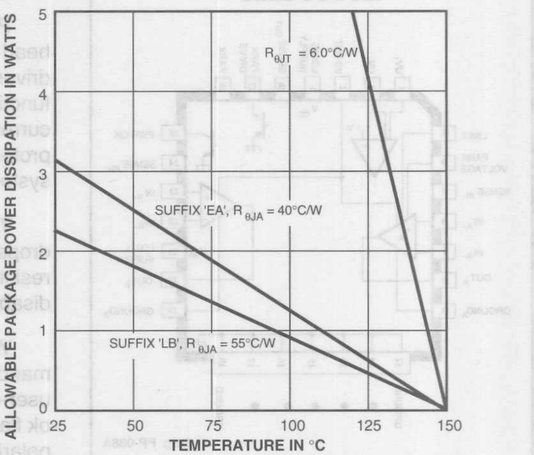
Always order by complete part number:

Part Number	Package
A8958CEA	**28-Lead Half-Batwing PLCC**
A8958CLB	**24-Lead Batwing SOIC**

A8958CLB

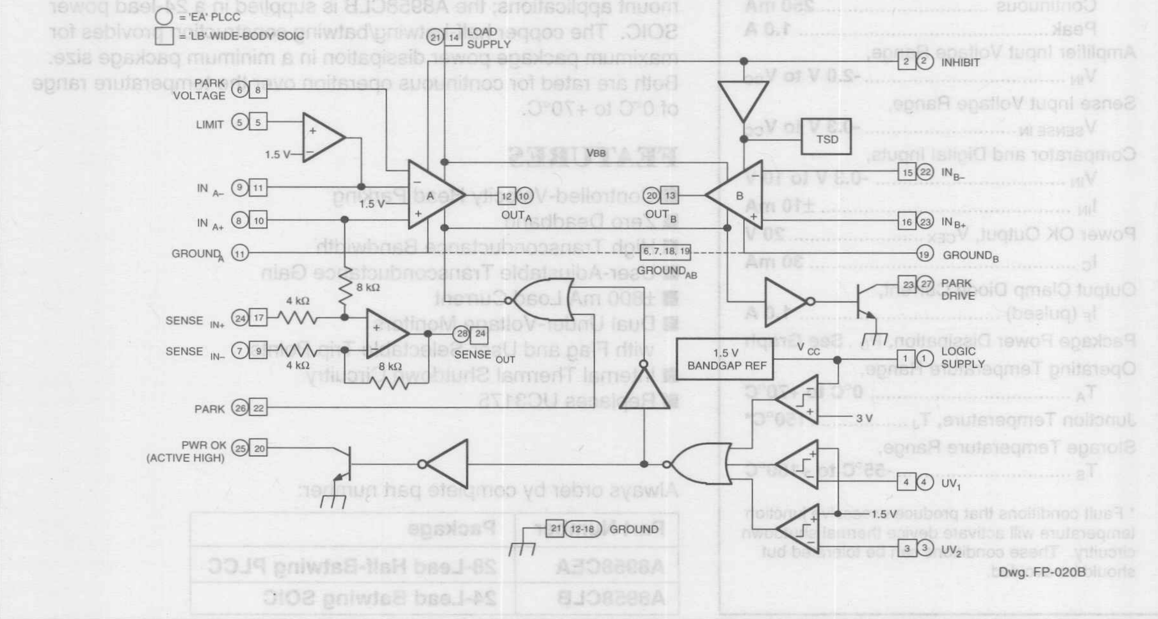


Dwg. PP-054



Dwg. GP-049-1

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-020B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Logic Supply Voltage Range	V_{CC}	Operating	8.0	12	16	V
Logic Supply UV Threshold	V_{CC}	High-to-low transition	—	2.8	3.0	V
Logic Supply UV Hysteresis	ΔV_{CC}		—	200		mV
Supply Current	I_{BB}	V_{OUT} = 6 V, no load	—	2.0	—	mA
	I_{CC}		—	23	—	mA
Inhibited Supply Current	—	$I_{BB} + I_{CC}$, $V_2 \geq 1.7$ V	—	3.0	8.0	mA
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	8.0		°C
Output Power Drivers						
Output Saturation Voltage	V_{SAT}	I_{OUT} = 250 mA	—	250	—	mV
		I_{OUT} = 800 mA	—	450	—	mV
		I_{OUT} = -250 mA	—	750	—	mV
		I_{OUT} = -800 mA	—	950	—	mV
Total Saturation Voltage (Source+Sink)	V_{SAT}	I_{LOAD} = 250 mA	—	1.0	1.4	V
		I_{LOAD} = 800 mA	—	1.4	2.0	V
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	5.0	8.0	mV
Input Offset Drift	ΔV_{IO}		—	—	25	µV/°C
Input Bias Current	I_{IN}	Except IN_{A+}, V_{CM} = 6 V	—	-150	-500	nA
		IN_{A+} to $SENSE_{IN+}$ = 12 kΩ, T_J = 25°C	69	84	105	µA/V
Input Offset Current	I_{IO}	IN_B only, V_{CM} = 6 V	—	—	200	nA
Differential Sense Input Current	I_{ID}	I_{OUT} = 5 mA	—	±300		µA
		I_{OUT} = 500 mA	—	3.0	—	mA
Large Signal Gain	A_{VS}	V_{OUT} = 2 V to 10 V, I_{OUT} = ±500 mA	1.5	5.0	—	V/mV
Slew Rate	SR		—	4.0	—	V/µs
Unity Gain Bandwidth	BW	Amplifier A	0.5	1.0	1.7	MHz
		Amplifier B	0.5	2.0	2.2	MHz
Common-Mode Rejection	k_{CMR}	V_{CM} = 1 V to 10 V	70	90		dB
Clamp Diode Forward Voltage	V_F	I_F = 800 mA, $V_2 \geq 1.7$ V	—	1.0	1.2	V
High-Side Current Limit	I_{OUT}	T_J = 25°C	—	1.0	1.2	A
Power Supply Rejection	k_{SVR}	V_{CC} = 4 V to 15 V, V_{CM} = 1.5 V	70	90	—	dB

Continued next page...

Negative current is defined as coming out of (sourcing) the specified device terminal.
Typical Data is for design information only.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Current Sense Amplifier						
Input Offset Voltage	V_{IO}	V_{CM} = 6 V	—	—	2.0	mV
Input Offset Drift	ΔV_{IO}	V_{CM} = 0 V to 12 V	—	—	3000	µV/V
			—	—	8.0	µV/°C
Voltage Gain	A_{VS}	V_{ID} = -1 V to +1 V, V_{CM} = 6 V	1.95	2.00	2.05	—
Output Saturation Voltage	V_{SAT}	V_{OUT}, $I_{OUT(SINK)}$ = 1.5 mA	—	300	500	mV
		V_{CC} - V_{OUT}, $I_{OUT(SOURCE)}$ = -1.5 mA	—	400	700	mV
Park Function						
PARK DRIVE Leakage Current	I_{CEX}	V_{CEX} = 20 V	—		100	µA
PARK DRIVE Saturation Voltage	$V_{CE(SAT)}$	I_C = 200 mA	—	300	500	mV
PARK Input Threshold	V_{PARK}		0.7	1.1	1.7	V
PARK Input Current	I_{PARK}	V_{PARK} = 1.7 V	—	—	100	µA
PARK VOLTAGE Input Current	$I_{PARK\ V}$		—	-150	-500	nA
Under-Voltage Protection						
UV Threshold	V_{UV}	Low-to-High Trans., Other Input = 6 V	1.48	1.50	1.52	V
UV Threshold Hysteresis	ΔV_{UV}		15	25	45	mV
UV Input Current	I_{UV}	V_{UV} = 1 V	—	-0.5	-1.5	µA
PWR OK Saturation Voltage	$V_{CE(SAT)}$	I_C = 5 mA	—	—	450	mV
PWR OK Leakage Current	I_{CEX}	V_{CEX} = 20 V	—	—	5.0	µA
Auxiliary Functions						
LIMIT Input Voltage	$V_{LIMIT(L)}$	OUT_A forced Low	0.7	0.8	—	V
	$V_{LIMIT(H)}$	OUT_A forced High	—	2.2	2.3	V
	V_{LIMIT}	Limit inactive	1.2	—	1.8	V
		Open circuit	1.45	1.50	1.55	V
LIMIT Input Resistance	R_{LIMIT}	V_{LIMIT} = 1.2 V to 1.8 V	—	10	—	kΩ
INHIBIT Input Threshold	V_2		0.7	1.1	1.7	V
INHIBIT Input Current	I_2	V_2 = 1.7 V	—	—	200	µA

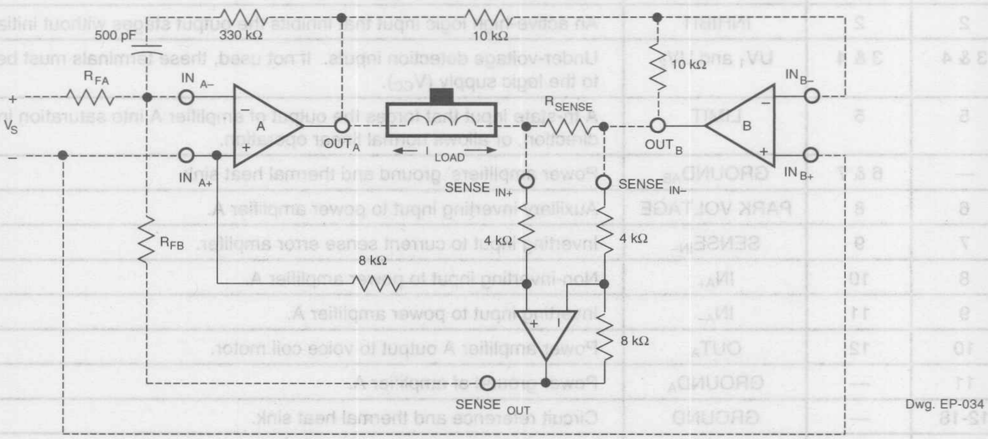
Negative current is defined as coming out of (sourcing) the specified device terminal.

Typical Data is for design information only.

TERMINAL FUNCTIONS

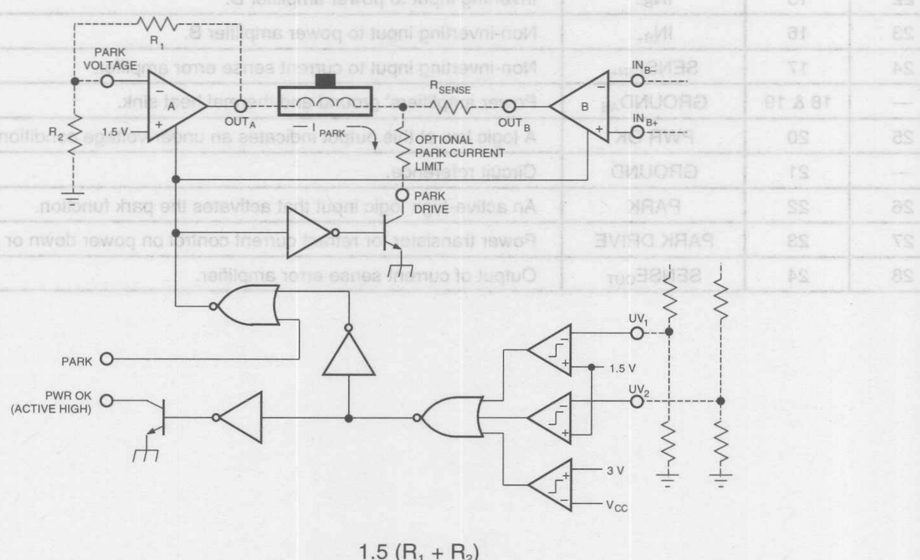
'EA' Term.	'LB' Term.	Terminal Name	Function
1	1	LOGIC SUPPLY	V_{CC}; logic supply voltage.
2	2	INHIBIT	An active-high logic input that inhibits the output stages without initiating a park.
3 & 4	3 & 4	UV_1 and UV_2	Under-voltage detection inputs. If not used, these terminals must be connected to the logic supply (V_{CC}).
5	5	LIMIT	A tri-state input that forces the output of amplifier A into saturation in either direction, or allows normal linear operation.
—	6 & 7	$GROUND_{AB}$	Power amplifiers' ground and thermal heat sink.
6	8	PARK VOLTAGE	Auxiliary inverting input to power amplifier A.
7	9	$SENSE_{IN-}$	Inverting input to current sense error amplifer.
8	10	IN_{A+}	Non-inverting input to power amplifier A.
9	11	IN_{A-}	Inverting input to power amplifier A.
10	12	OUT_A	Power amplifier A output to voice coil motor.
11	—	$GROUND_A$	Power ground of amplifier A.
12-18	—	GROUND	Circuit reference and thermal heat sink.
19	—	$GROUND_B$	Power ground of amplifier B.
20	13	OUT_B	Power amplifier B output to voice coil motor.
21	14	LOAD SUPPLY	V_{BB}; load supply voltage.
22	15	IN_{B-}	Inverting input to power amplifier B.
23	16	IN_{B+}	Non-inverting input to power amplifier B.
24	17	$SENSE_{IN+}$	Non-inverting input to current sense error amplifer.
—	18 & 19	$GROUND_{AB}$	Power amplifiers' ground and thermal heat sink.
25	20	PWR OK	A logic low at this output indicates an under-voltage condition.
—	21	GROUND	Circuit reference.
26	22	PARK	An active-high logic input that activates the park function.
27	23	PARK DRIVE	Power transistor for retract current control on power down or park command.
28	24	$SENSE_{OUT}$	Output of current sense error amplifier.

CURRENT SENSING



Dwg. EP-034

PARKING FUNCTION



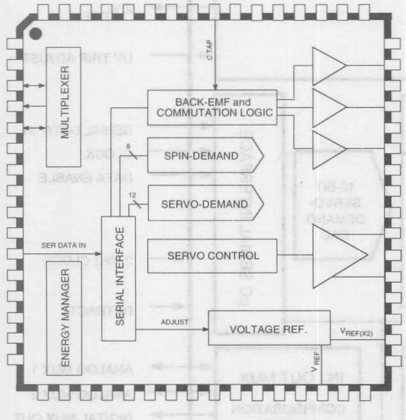
$$V_{OUT\ A} = \frac{1.5\,(R_1 + R_2)}{R_2}$$

Dwg. EP-039

8980

26310

SuperServo™ SPINDLE & VOICE-COIL ACTUATION MANAGER/DRIVER



Dwg. PP-048

The A8980CJT provides complete drive, management, and control of the voice-coil and spindle motor power actuation subsystems used in hard disk drives. Extensive programmable control features and system diagnostics are provided via a serial interface under the direction of an external microcontroller. The large-scale integration and use of advanced DABiC™ (*d*igital/*a*nalog-*BiC*MOS) merged technologies results in minimum power dissipation, minimum operating voltage requirements, and minimum external components.

The spindle drive function incorporates a three-phase MOS power driver and a back-EMF sensing motor commutation scheme. Internal logic and analog circuitry provide complete start-up and µC-assisted run modes without the need for snubbers or other external components. Additional headroom is achieved by a proprietary circuit, which eliminates the need for an external current-sense resistor. Intrinsic ground clamp and flyback diodes are also provided.

The voice-coil function contains a 12-bit DAC, tunable low-pass and notch filters, and a full-bridge power driver. The MOS outputs provide increased available voltage and lower power dissipation over bipolar devices. Voice-coil current is sensed by internal circuitry that eliminates the need for an external current-sense resistor. Additional internal circuitry can be configured to provide an over-velocity fault limit by utilizing the internally monitored current of the voice-coil motor.

The spindle and voice-coil control functions are supplemented by an Energy Manager™ subsystem, which efficiently channels available power to protect the heads and the data disk during system failure or normal system shutdown. Synchronous rectification of spindle back-EMF voltage provides nearly lossless conversion of spindle rotational inertia into power to operate the voice coil motor for parking the heads. A dc-to-dc converter provides continuous operation at minimum supply voltages. In addition, the Energy Manager subsystem provides several sleep modes and latched fault states for undervoltage or thermal faults.

The A8980CJT is supplied in a 64-lead thin quad flatpack for surface-mount applications.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, $V_{CC(PWR)}$ .... **7.0 V**
Spindle Output Current, $I_{OUT(S)}$ .... **±1.6 A**
Voice-Coil Output Current, $I_{OUT(S)}$ ...... **±0.9 A**
Output Current, $I_{OUT(S)}$ .... **±1.6 A**
Logic Supply Voltage $V_{CC(D)}$ .... **6.0 V**
Operating Temperature Range,
T_A .... **0°C to +70°C**

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling.

FEATURES

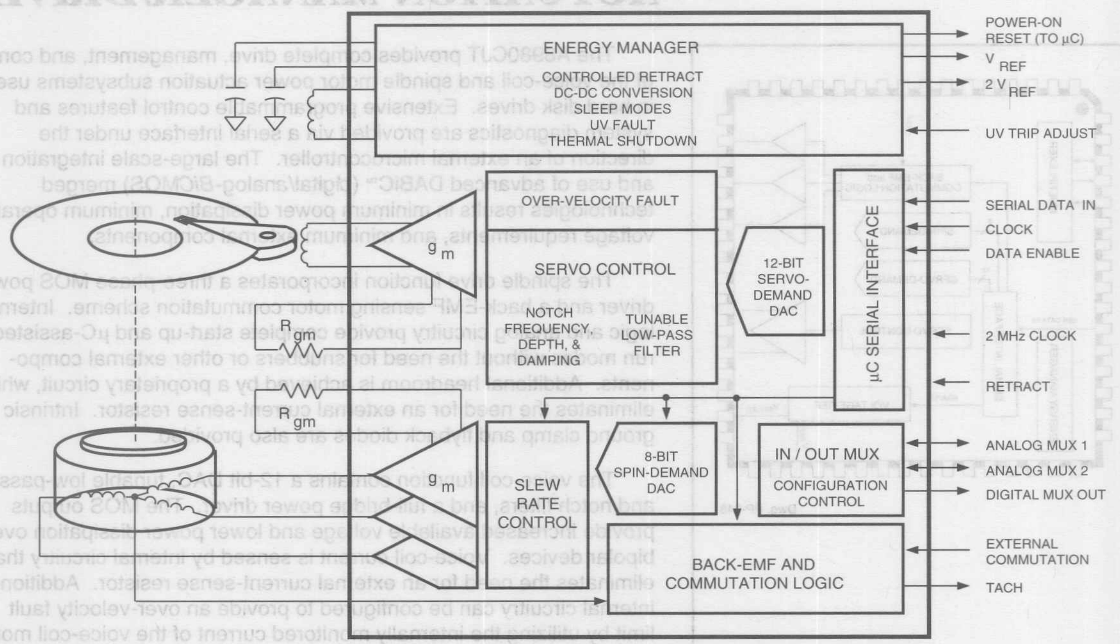
Voice Coil Motor Driver:

- Low $r_{DS(on)}$ MOS Outputs
- Lossless Current Sensing
- Zero Deadband
- User-Adjustable Transconductance Gain
- Retract Circuitry Functional to 0 V

8980

SUPERSERVO™ SPINDLE & VOICE-COIL ACTUATION MANAGER/DRIVER

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-028B

Spindle Motor Controller/Driver:
- Low $r_{DS(on)}$ MOS Outputs
- Back-EMF Circuitry Eliminates Hall-Effect Sensors
- Programmable Slew Rate Eliminates Snubbers
- Lossless Current Sensing
- Improved Speed Disturbance Performance
- Dynamic Braking with Delay
- Active Braking

Servo Compensator/Notch:
- Over-Velocity Fault Circuitry
- 12-Bit Servo-Demand DAC
- Programmable Complex Pole Low-pass-Filter
- Programmable Notch Frequency, Depth, and Damping

Energy Manager:
- 3.0 V to 5.5 V Operation
- Independent Power-Down (Sleep) Modes for all Functional Blocks
- Efficient Synchronous Rectification Supplies Power During Blackout
- Thermal Fault Shutdown Circuitry
- Trimmed Bandgap Voltage Reference
- Smart DAC Reference Generator
- Programmable Voltage Reference for Relative Ground
- Over-Velocity Fault Circuitry
- Supply Under-Voltage Monitor with Adjustable Trip Point
- System Diagnostics Data Out
- Power-On Reset Generator

FUNCTIONAL DESCRIPTION

ACTUATOR

Servo-Demand DAC. A 12-bit DAC is provided to bridge the DSP "soft" domain to the analog hardware domain. The term "demand" refers to the distinction between the newly requested voice-coil current and the prior current being supplied. The DAC, operating in straight binary format, spans the full dynamic range between a large signal velocity and a precision position mode. The DAC output is updated synchronously with the notch functions to avoid the creation of aliasing products.

Low-Pass Filter. This double, non-intrinsic complex-pole low-pass filter is provided to attenuate undesirable, out-of-band information. The input of this discrete time filter is sampled synchronously with the 12-bit DAC and notch function in order to avoid aliasing products.

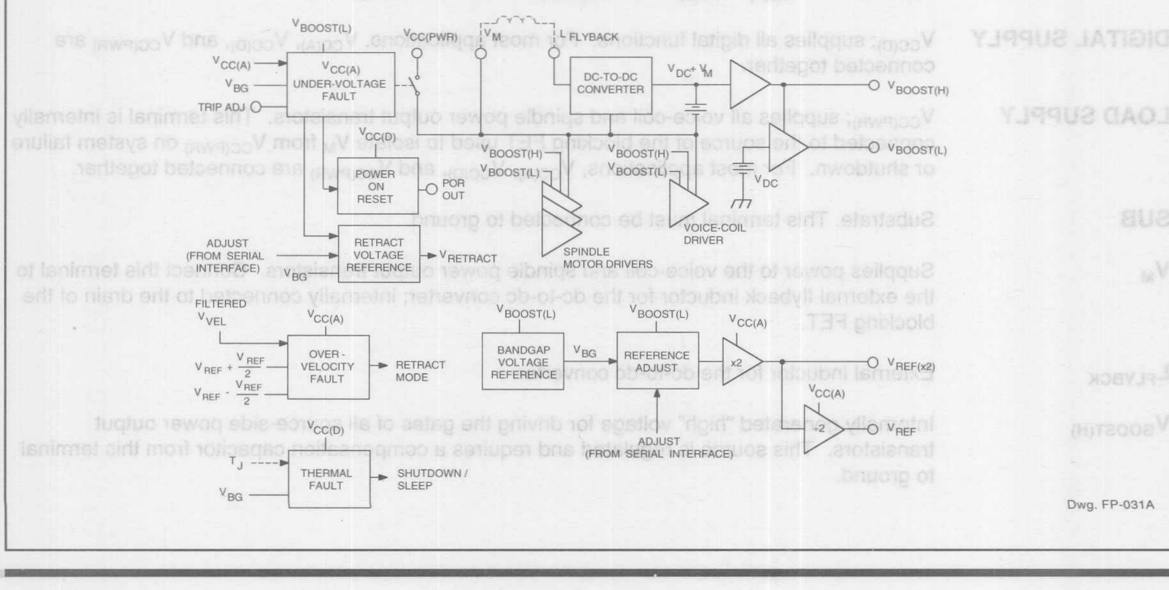
Notch Filter. This notch filter has a programmable center frequency and programmable notch depth to provide truly independent control of notch damping. Enough range and granularity are provided to allow versatile and accurate out-of-band attenuation of undesirable energy sources.

Actuator Transconductance Amplifier. The final transconductance function of the voice-coil actuation signal path is achieved by monitoring the load current and generating an error voltage to drive a local g_m amplifier control loop. The error voltage is scaled by an external precision resistor ($R_{gm(act)}$). This resistor does not carry load current and is intended only for accurate determination of the transconductance. The function is:

$$g_{m(act)} = \frac{5800}{R_{gm(act)}} \text{ A/V}$$

and $I_{OUT} = V_{SERVO} \bullet g_{m(ACT)}$.

Actuator Power Outputs. The voice-coil output driver is a full-bridge power driver operating in a class-B mode. The power output devices are enhancement-mode MOS transistors. Special internal circuitry results in nearly zero cross-over distortion when switching from one source/sink pair to another.



Dwg. FP-031A

SPINDLE

The spindle function is a three-phase back-EMF sensing motor controller and driver. During start-up, internal circuitry provides complete spindle control and drive. At speed however, an external microcontroller is used to provide speed (phase/frequency) detection as well as compensation.

ENERGY MANAGER

The management of available energy is provided by automatic operating modes envoked by the fault monitor or sleep-mode manager. The fault monitor consists of an over-velocity fault circuit, a $V_{CC(A)}$ under-voltage fault circuit, and a thermal fault circuit. The operating modes include $V_{CC(PWR)}$ isolation, active rectification of spindle back-EMF voltage to provide nearly lossless conversion of spindle rotational inertia into power to operate the voice-coil motor for parking the heads, actuator retract mode controlled by constant voltage, and several sleep modes. In addition, a power-on reset function and two programmable voltage references (V_{REF} and $V_{REF(x2)}$) are provided that are suitable for output to the user.

An onboard dc-to-dc converter generates two regulated “high” (greater than the supply) voltages referred to as $V_{BOOST(H)}$ and $V_{BOOST(L)}$. These voltages supply critical functions with maximum immunity from supply variations.

SERIAL INTERFACE

The serial interface is used to alter the control state of the device from an external microcontroller or other digital CMOS source. In addition to the various operational and diagnostic control states (modes), all critical constants, variables, and parameters can be adjusted through this interface. The serial interface is a synchronous serial three-wire port with serial data input, clock, and load (active low) functions. When LOAD is high, the serial interface is disabled and the chip is not affected by changes in SER DATA IN or CLK SER. To write data to the serial interface, CLK SER should be low prior to LOAD going low. Once LOAD goes low, information at SER DATA IN is read into the shift register on the positive-going transitions of CLK SER.

TERMINAL FUNCTIONS

ANALOG SUPPLY $V_{CC(A)}$; supplies all analog functions except for gate drive of power output transistors. For most applications, $V_{CC(A)}$, $V_{CC(D)}$, and $V_{CC(PWR)}$ are connected together.

DIGITAL SUPPLY $V_{CC(D)}$; supplies all digital functions. For most applications, $V_{CC(A)}$, $V_{CC(D)}$, and $V_{CC(PWR)}$ are connected together.

LOAD SUPPLY $V_{CC(PWR)}$; supplies all voice-coil and spindle power output transistors. This terminal is internally connected to the source of the blocking FET used to isolate V_M from $V_{CC(PWR)}$ on system failure or shutdown. For most applications, $V_{CC(A)}$, $V_{CC(D)}$, and $V_{CC(PWR)}$ are connected together.

SUB Substrate. This terminal must be connected to ground.

V_M Supplies power to the voice-coil and spindle power output transistors. Connect this terminal to the external flyback inductor for the dc-to-dc converter; internally connected to the drain of the blocking FET.

L_{FLYBCK} External inductor for the dc-to-dc converter.

$V_{BOOST(H)}$ Internally generated “high” voltage for driving the gates of all source-side power output transistors. This source is regulated and requires a compensation capacitor from this terminal to ground.

$V_{BOOST(L)}$	Internally generated intermediate voltage for driving the gates of all sink-side power output transistors, the bandgap reference, and fault monitors. This source is regulated and requires a compensation capacitor from this terminal to ground.
$V_{PF(GATE)}$	Control voltage provided to drive the gate of an optional external enhancement-mode power FET, augmenting the internal blocking FET between $V_{CC(PWR)}$ and V_M.
V_{REF}	Programmable reference voltage output. This reference tracks $V_{REF(x2)}$ and may be used as a relative signal ground.
$V_{REF(x2)}$	Programmable reference voltage output. Derived from a trimmed internal bandgap reference. May be used as the reference for system DAC and ADC.
POR_{OUT}	Power-on reset for the application system. Active low guaranteed by design to be active on power up. Also occurs as a result of $V_{CC(A)}$ degrading below the BLACKOUT under-voltage threshold.
TRIP ADJ	$V_{UV\ (TRIP)}$; trip threshold adjust input (an external resistor divider between $V_{CC(A)}$ and ground) for the under-voltage BLACKOUT fault monitor. A capacitor at this terminal can provide for time domain filtering.
CLK	$f_{CLK(2MHz)}$; reference for all internal analog signal-processing functions. Affects frequency domain placement of all poles, zeros, and bandwidths.
SER DATA IN	Non-inverting microcontroller serial-data input used for transferring data to all internal parameter and mode-control registers.
CLK SER	$f_{CLK(SER)}$; reference for the serial data interface. Data is transferred on the positive-going edge of this clock.
LOAD	Active low. Begins and ends data transfer.
EXT XFR	Direct clock gating data from temporary internal latch to control register. This continuous time input is redundant to the XFR bit, which is embedded in the serial data format. It is internally synchronized to the $f_{CLK(2MHz)}$ positive-going edge.
$AMUX_1$	Analog input or output. Also used to drive internal nodes.
$AMUX_2$	Analog input or output. Also used to drive internal nodes for calibration and measurement on internal analog functions.
$DMUX_{OUT}$	Non-inverting digital multiplexer output. Used to probe internal nodes allowing precise time-domain measurements. Also used to extract internal status and diagnostic information.
OUT_P	$V_{OUT(P)}$; voice-coil power output. Full-bridge differential complement to $V_{OUT(N)}$.
OUT_N	$V_{OUT(N)}$; voice-coil power output. Full-bridge differential complement to $V_{OUT(P)}$.
$V_{SENS(act)}$	The voltage at this terminal is proportional to voice-coil actuator current.

$R_{gm(act)}$	A resistor between this terminal and $V_{SENS(act)}$ is used to adjust the forward transconductance gain of the voice-coil transconductance amplifier.
RETRACT	Active high retract input from the system. Continuous-time direct input to cause immediate retract mode.
EXT ACT	V_{SERVO}; summing junction at the input of the voice-coil transconductance amplifier. This direct continuous-time input to the actuator g_m amplifier provides diagnostic as well as feed-forward access.
$OP_{1(IN)}$	Operational amplifier inverting input. The non-inverting input is internally connected to V_{REF}.
$OP_{1(OUT)}$	Operational amplifier output. This undedicated operational amplifier functions in continuous time.
VEL_{INN}	Inverting input of operational amplifier portion of over-velocity fault circuit.
VEL_{INP}	Non-inverting input of operational amplifier portion of over-velocity fault circuit.
VEL	V_{VEL}; output of the over-velocity operational amplifier. Also internally connected to the inputs of two comparators that provide the positive and negative velocity fault thresholds.
OUT_A	$V_{OUT(A)}$; spindle motor power output terminal.
OUT_B	$V_{OUT(B)}$; spindle motor power output terminal.
OUT_C	$V_{OUT(C)}$; spindle motor power output terminal.
C TAP	Connection to spindle motor center tap; provides the differential reference for detection of back-EMF zero crossings. If this terminal is not connected, the device will internally simulate the centertap of the motor.
$V_{SENS(spin)}$	The voltage at this terminal is proportional to the spindle motor current.
$R_{gm(spin)}$	A resistor connected from this terminal to $V_{SENS(spin)}$ provides for adjusting the forward transconductance gain of the spindle transconductance amplifier.
f_{com}	A digital logic output that goes low to high on a back-EMF zero crossing; provides tach-like information to the spin controller.
EXT COM	f_{sync}; hard external commutation sequence start (positive-edge triggered). May be used to place spindle commutation edges in the inter-sector gap, or for phase-locking multiple spindle drivers.
EXT SPIN	V_{spin}; direct continuous time input to the spindle transconductance amplifier/driver. Zero demand current occurs at 2.00 V; full-scale positive demand current occurs at 4.00 V.
SW_{IN}	Input for uncommitted analog switch.
SW_{OUT}	Output of uncommitted analog switch.
SW_{ON}	Logic input for uncommitted analog switch; a high level connects SW_{IN} to SW_{OUT}.

ADDRESS MAP AND DATA BIT ASSIGNMENTS

Address Word	Data Bit	Function
00H	0 – 3	Blanking Time
	4 – 7	Commutation Delay Time
01H	0 – 5	Coast Time
	6	Commutation Multiplexer
	7	Not used at this time
02H	0 – 3	Startup Time
	4 – 7	Watchdog Time
03H	0 – 7	Spindle-Demand DAC Current Magnitude
	8	Reverse Commutation Mode
04H	0 – 3	Spindle Slew Rate Control
	4 – 6	Spindle Multiplexer
	7	Not used at this time
05H	0 – 3	Spindle Transconductance Amp. Bandwidth
	4 – 6	Spindle Transconductance Amp. Local Zero
06H	0 – 3	Internal 6.25 kHz Oscillator Frequency Trim
	4 – 7	Not used at this time
07H	0 – 7	Not used at this time
08H	0 – 11	Servo-Demand DAC Current Magnitude
09H	0 – 7	Not used at this time
0AH	0 – 3	Low-Pass Filter Damping (Zeta) Control
	4	Not used at this time
	5	Low-Pass Filter Reset Control
	6 – 7	Not used at this time
0BH	0 – 3	Notch Depth (α_3) Control
	4 – 7	Not used at this time
0CH	0 – 3	Notch Width (Zeta D_{Z3}) Control
	4	Notch Reset Control
	5 – 7	Not used at this time
0DH	0 – 4	Low-Pass Filter Freq. Synth. (D_{n2}) Control
	5 – 7	Not used at this time
0EH	0 – 4	Notch Center Frequency (D_{n3}) Control
	5 – 7	Not used at this time
0FH	0 – 3	Actuator Bandwidth (BW_{ACT}) Control
	4 – 6	Actuator Zero (Damping) Control
	7	Not used at this time
10H	0 – 2	Retract Velocity Demand Voltage
	3 – 5	Actuator Analog Multiplexer Input Select
	6 – 7	Not used at this time
11H	0 – 7	Sleep Mode Manager
12H	0 – 3	Fault Control Monitor
	4 – 6	Programmable References Voltage Select
	7	Long Spindle Braking Delay
13H	0 – 2	Analog Multiplexer-2 Selection
	3 – 5	Digital Multiplexer Output Selection
	6 – 7	Not used at this time
14H	0 – 2	Analog Multiplexer-1 Selection
	3	Chopper Stabilization of LP & Notch Filters
	4	Disable actuator retract during fault
	5 – 7	Not used at this time
15H	0 - 2	Actuator Power Voltage Amplifier Deadband Trim

8983

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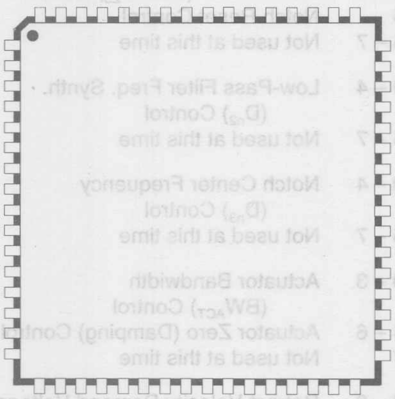
SPINDLE & VOICE-COIL ACTUATION MANAGER/DRIVER



Dwg. PP-060

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, $V_{CC(PWR)}$ .... 7.0 V
Spindle Output Current, $I_{OUT(S)}$ .... ±1.6 A
Voice-Coil Output Current, $I_{OUT(A)}$ ...... ±0.9 A
Logic Supply Voltage $V_{CC(D)}$ .... 6.0 V
Operating Temperature Range,
T_A .... 0°C to +70°C

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling.

The A8983CJT provides for complete spindle and voice coil power electronics for small form-factor HDDs (hard disk drives). The large-scale integration and use of advanced DABiC (digital/analog-BiCMOS) merged technologies result in minimum power dissipation, minimum operating voltage, and minimum external components.

The spindle driver system incorporates a three-phase MOS power driver and a back-EMF sensing motor commutation scheme. A patented circuit eliminates the need for an external current-sense resistor, achieving additional headroom. Intrinsic ground clamp and flyback diodes are also provided.

The voice-coil system incorporates a MOS H-bridge driver, sense amplifier, error amplifier, and programmable retract circuitry.

The spindle and voice-coil control functions are supplemented by an ENERGY MANAGER™, which efficiently channels available spindle BEMF to protect the heads and the data disk during system power supply failure. Active regeneration of spindle BEMF provides nearly lossless conversion of spindle BEMF into supply voltage to operate the voice coil motor for parking the heads. A dc-to-dc converter provides for full power MOS $r_{DS(on)}$ performance at minimum supply voltages. In addition, the ENERGY MANAGER provides several energy-saving sleep modes and latched fault states for undervoltage and serial port commanded fault.

The A8983CJT is supplied in a 64-lead low-profile quad flatpack for surface-mount applications.

FEATURES

Voice Coil Motor Driver:

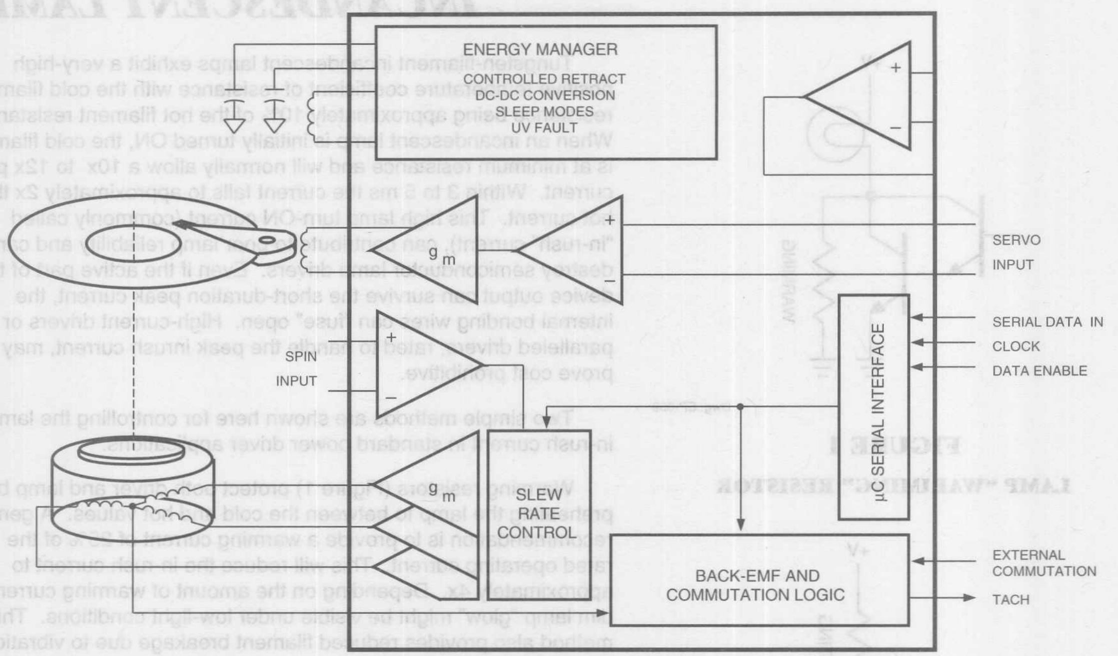
- Low $r_{DS(on)}$ MOS Outputs
- Zero Deadband
- Externally Determined Transconductance, with Hi/Lo Configuration Switched via Serial Port
- Current Sensing with External Series Sense Resistor
- Serial Port Programmable Actuator Retract Circuitry
- Retract Circuitry Functional to 1.7 V Spindle BEMF

Spindle Motor Controller/Driver:

- Low $r_{DS(on)}$ MOS Outputs
- Back-EMF Circuitry Eliminates Hall-Effect Sensors
- Adaptive Commutation Delay Programmable via Serial Port
- Programmable Slew Rate (soft switching) Eliminates Snubbers
- Intrinsic Ground Clamp and Flyback Diodes

8983
SPINDLE & VOICE-COIL ACTUATION MANAGER/DRIVER

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-028-1

- Patented Lossless Current Sensing Eliminates Need for External Current-Sense Resistor
- Externally Determined Transconductance, with Hi/Lo Configuration Switched via Serial Port
- Forward or Reverse Torque Serial Port Bit Allows Improved Speed Disturbance Performance
- Dynamic Braking with User Delay, Activated by Undervoltage or Serial Port Command
- Power-On-Reset Generator for Power Up or Power Loss with User-Defined Delay
- Chip Powers Up in Sleep Mode for Minimum Power Dissipation
- External 2 MHz System Clock, or Internal Serial Port Trimmed 2 MHz Clock
- System Diagnostics
- Uncommitted Op-amp

Energy Manager:

- 3.0 V to 5.5 V Operation
- DC-to-DC Converter Maintains $r_{DS(on)}$ Performance at Low Supply
- Independent Power-Down (Sleep) Modes for all Functional Blocks
- Efficient Active Regeneration Supplies Power During Retract
- Supply Under-Voltage Fault Monitor with Adjustable Trip Point

A PRIMER ON DRIVING INCANDESCENT LAMPS

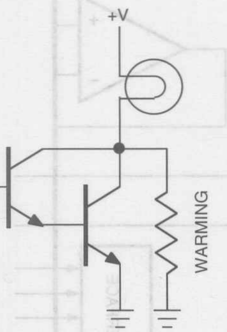


FIGURE 1

LAMP "WARIMING" RESISTOR

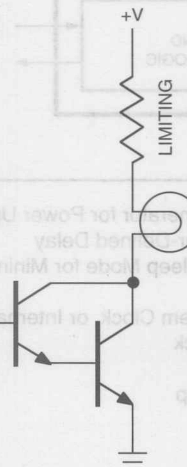


FIGURE 1

CURRENT-LIMITING RESISTOR

Tungsten-filament incandescent lamps exhibit a very-high positive temperature coefficient of resistance with the cold filament resistance being approximately 10% of the hot filament resistance. When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and will normally allow a 10x to 12x peak current. Within 3 to 5 ms the current falls to approximately 2x the hot current. This high lamp turn-ON current (commonly called "in-rush" current), can contribute to poor lamp reliability and can destroy semiconductor lamp drivers. Even if the active part of the device output can survive the short-duration peak current, the internal bonding wires can "fuse" open. High-current drivers or paralleled drivers, rated to handle the peak inrush current, may prove cost prohibitive.

Two simple methods are shown here for controlling the lamp in-rush current in standard power driver applications.

Warming resistors (Figure 1) protect both driver and lamp by preheating the lamp to between the cold and hot values. A general recommendation is to provide a warming current of 25% of the rated operating current. This will reduce the in-rush current to approximately 4x. Depending on the amount of warming current, a dim lamp "glow" might be visible under low-light conditions. This method also provides reduced filament breakage due to vibration but adds significant power consumption when the lamp is OFF.

Alternatively, an inexpensive current-limiting resistor (Figure 2) can be used to protect the lamp and driver, which will dissipate only a small amount of power when the lamp is ON. The minimum resistor value is easily calculated as

$$R_S \geq V_{CC} - \underset{I_{cm}}{V_{CE(sat)}} - \frac{V_L}{10 \times I_L}$$

where I_L = rated lamp current
I_{cm} = rated peak driver current
V_{CC} = supply voltage
$V_{CE(sat)}$ = driver saturation voltage at rated peak current
V_L = rated lamp voltage

The required resistor power rating is determined by the hot filament current and is usually 1/4 or 1/2 W ($P_S = I_L^2 \times R_S$). The slightly reduced lamp voltage, caused by the series resistor voltage drop ($I_L \times R_S$), should have minimum effect on lamp brightness and will prolong lamp life. If brightness is an important concern, the supply voltage can be increased* to compensate for

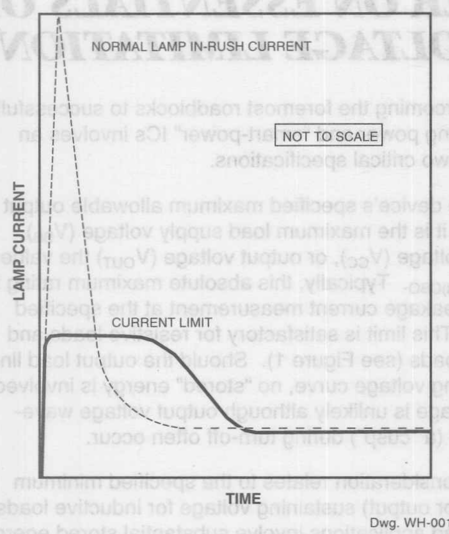


FIGURE 3

LAMP CURRENT vs TIME

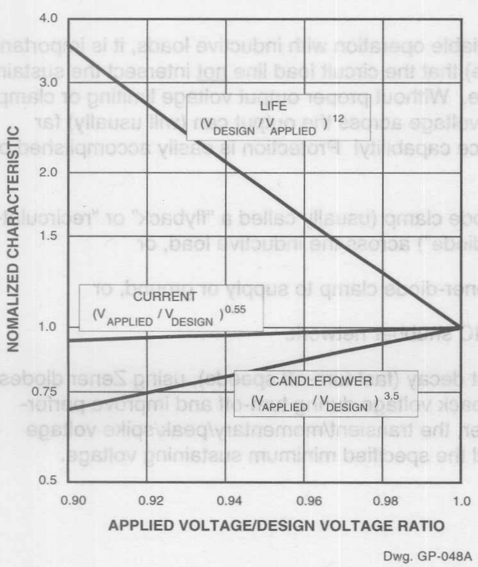


FIGURE 4

LAMP CHARACTERISTICS AT REDUCED VOLTAGE

the driver saturation voltage and the series resistor voltage drop or, alternatively, a negative-temperature coefficient resistor can be used where R_S is its cold resistance.

Lamps can also be efficiently driven by current-limited power drivers without the need for warming or current-limiting resistors. These current-limited drivers are listed below. With these drivers, during turn-ON, the high in-rush current is sensed by an internal low-value resistor and/or a thermal-gradient sensing circuit. During this transition period, the output stage is driven in a linear fashion, limiting the current while the filament resistance increases to its hot value (Figure 3). As the lamp current falls, the output stage goes into saturation and applies full supply voltage to the lamp.

Allegro Lamp Driver(s)	Channels per Driver	Maximum Continuous Current	Current Limit Value
UDN/UDQ2543B	4	700 mA	1.0 A
UDN2547B	4	600 mA	1.3 A
UDN2549B/EB	4	600 mA	1.0 A
UGQ5140K Hall	1	300 mA	900 mA

Some Allegro drivers, with over-current protection in the form of a fault latch (as in the UDN2987A), cannot be used in lamp driver applications except with stringent design efforts. In applications controlling multiple lamp filaments, the internal clamp diodes may be connected together through an appropriate current-limiting resistor to a simple “lamp test” switch. A side-effect with any current-limiting method is that lamp turn-on time will increase, but generally this is unimportant and not noticeable.

For reference, as approximations, the light output of an incandescent lamp (other than long life (>5000 hrs) or halogen-cycle lamps) varies as the 3.5 power of the applied voltage-to-design voltage ratio, the lamp current varies as the 0.55 power of the voltage ratio, and lamp life varies inversely as the 12th power of the voltage ratio (Figure 4).

* Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ times the nominal dc operating voltage (where N is the number of digits), to obtain sufficient brightness.

A PRIMER ON ESSENTIALS OF OUTPUT VOLTAGE LIMITATIONS

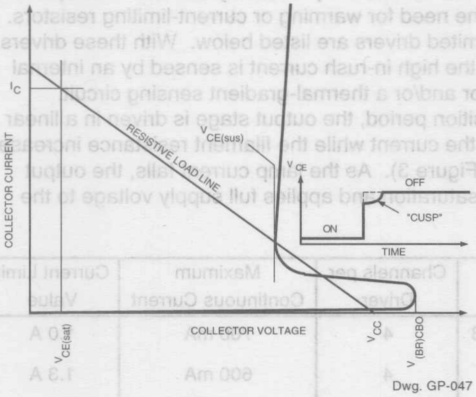


FIGURE 1

LOAD LINE WITH RESISTIVE LOAD

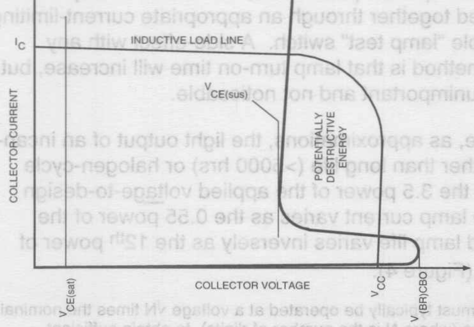


FIGURE 2

LOAD LINE WITH INDUCTIVE LOAD

Typically, overcoming the foremost roadblocks to successfully and reliably applying power and "smart-power" ICs involves an understanding of two critical specifications.

The first is the device's specified maximum allowable output voltage. Whether it is the maximum load supply voltage (V_{BB}), collector supply voltage (V_{CC}), or output voltage (V_{OUT}) the value approximates $V_{(BR)CBO}$. Typically, this absolute maximum rating is guaranteed by a leakage current measurement at the specified maximum value. This limit is satisfactory for resistive loads and some capacitive loads (see Figure 1). Should the output load line cross the sustaining voltage curve, no "stored" energy is involved. Thus, device damage is unlikely although output voltage wave-shape aberrations (a "cusp") during turn-off often occur.

The second consideration relates to the specified minimum collector-emitter (or output) sustaining voltage for inductive loads. Many inductive load applications involve substantial stored energy. The output load line during turn-off resembles that of Figure 2 and this stored energy can cause instantaneous, catastrophic failure of the device.

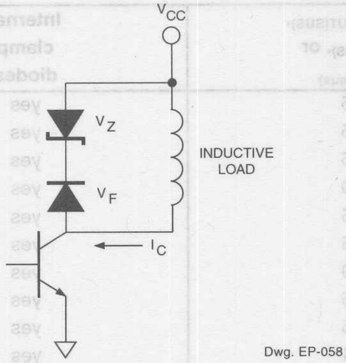
For safe, reliable operation with inductive loads, it is important (even imperative) that the circuit load line <u>not</u> intersect the sustaining voltage curve. Without proper output voltage limiting or clamping, the turn-off voltage across the output can (will usually) far exceed the device capability! Protection is easily accomplished by providing:

(a) a diode clamp (usually called a "flyback" or "recirculating diode") across the inductive load, or

(b) a Zener-diode clamp to supply or ground, or

(c) an RC snubber network.

For rapid current decay (fast turn-off speeds), using Zener diodes will raise the flyback voltage during turn-off and improve performance. However, the transient/momentary/peak/spike voltage must not exceed the specified minimum sustaining voltage.



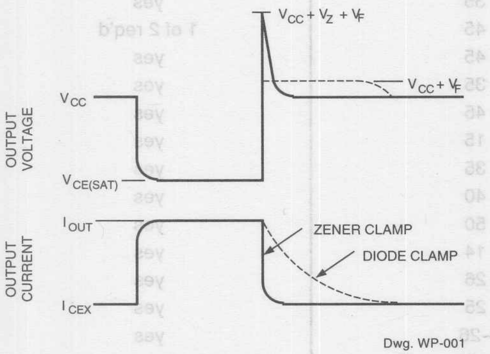


FIGURE 3

"PROTECTED" INDUCTIVE LOAD DRIVER

Power supply and circuit values are chosen such that V_{CC} (supply) + V_F (diode forward voltage) + V_Z (Zener voltage, if used) $\leq V_{CE(sus)}$.

Further, for reliable operation, the peak current ratings of both the flyback and Zener diodes must be at least as high as the load current. Note – surge power ratings of Zener diodes are typically greater than 10 times the continuous rating in repetitive, low-duty cycle (5% to 10%) applications.

The output voltage ratings of popular Allegro power drivers follows. Additional assistance pertaining to sustaining voltage issues can be provided by Allegro Applications Engineering.

Part Number(s)	Max. V_{BB}, V_{CC}, V_{OUT}, or V_{CEX}	Min. $V_{OUT(SUS)}$, $V_{CE(SUS)}$, or $V_{CE(sus)}$	Internal clamp diodes
2064	50	35	yes
2065	80	50	yes
2068	50	35	yes
2069	80	50	yes
2540	50	50	yes
2543	25*	35	yes
2544	50	50	yes
2547	25*	40	no
2549	25*	40	yes

Continued...

A PRIMER ON ESSENTIALS OF OUTPUT VOLTAGE LIMITATIONS

Part Number	Max. V_{BB}, V_{CC}, V_{OUT}, or V_{CEX}	Min. $V_{OUT(SUS)}$, $V_{CE(SUS)}$, or $V_{CE(sus)}$	Internal clamp diodes
2580	50	35	yes
2585	25	15	yes
2588	50	35	yes
2588-1	80	50	yes
2597	50	35	yes
2878 and 2878-2	50	35	yes
2879	80	50	yes
2916, 2917, and 2918	45	45	yes
2936	45	45	yes
2943	45	24	yes
2944	60	35	yes
2961	45	45	1 of 2 req'd
2962	45	45	yes
2981 and 2982	50	35	yes
2983 and 2984	80	45	yes
2985	30	15	yes
2987	35	35	yes
2993	40	40	yes
2998	50	50	yes
3625 Hall	14*	14	yes
3626 Hall	26*	26	yes
5140 Hall	25*	25	yes
5275 Hall	60	~26	yes
5703 and 5706	80	~50	yes
5713	80	~50	yes
5800 and 5801	50	~35	yes
5804	50	35	yes
5821	50	~35 (use 5841 for inductive loads)	no
5829	50	50	no
5841	50	35	yes
5842	80	50	yes
5881	20	15	yes
5890	80	50	yes
5891	50	35	yes
5895	50	35	yes
7003	150	90	yes
8902-A	14	14	yes
8925	14	14	yes

* Maximum allowable supply voltage is specified higher. Listed here is maximum useful operating voltage defined by an internal overvoltage shutdown or current limiting.

APPLICATIONS INFORMATION

POWER INTEGRATED CIRCUITS FOR MOTOR-DRIVE APPLICATIONS

Improved systems performance and reliability, lower component counts, and reduced cost are among benefits offered by space-saving power interface ICs. Many of the following devices are specifically designed for motor-drive applications. The development of these devices is especially significant in view of the increasing use of microprocessor-controlled servo and stepper motors.

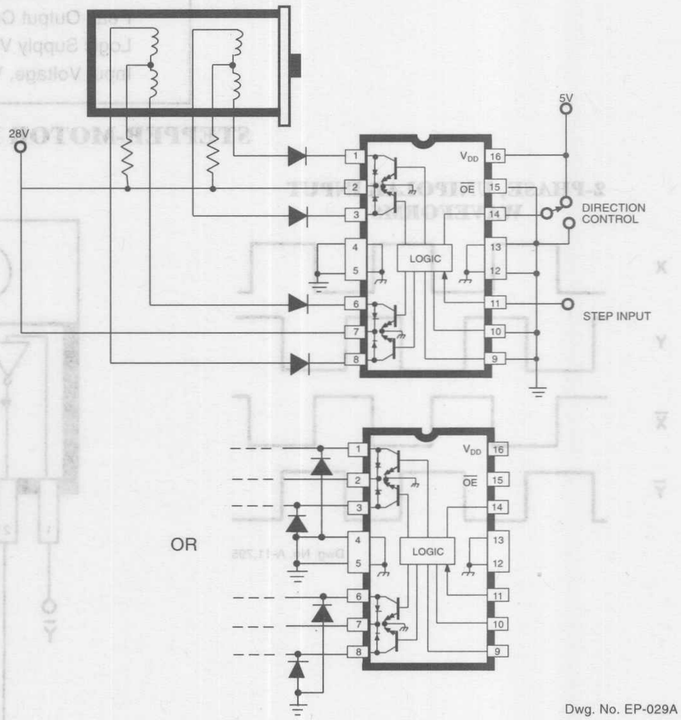
UNIPOLAR STEPPER-MOTOR TRANSLATOR/DRIVER

The UCN5804B integrated circuit drives permanent magnet stepper motors rated to 1.25 A and 35 V with a minimum of external components.

Internal step logic activates one or two of the four output sink drivers to step the load from one position to the next. The logic is activated when STEP INPUT (pin 11) is allowed to go HIGH. Single-phase (A-B-C-D), two-phase (DA-AB-BC-CD), or half-step (A-AB-B-BC-C-CD-D-DA) operation, and step-inhibit are selected by connections at pins 9 and 10. The sequence of states is determined by the DIRECTION CONTROL (pin 14).

Drive Format	Pin 9	Pin 10
Two-Phase	L	L
One-Phase	H	L
Half-Step	L	H
Step-Inhibit	H	H

L/R STEPPER-MOTOR DRIVE



Dwg. No. EP-029A

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage, V_{OUT} .... **35 V**
Output Current, I_{OUT} .... **1.25 A**
Logic Supply Voltage, V_{CC} .... **4.5 V to 5.5 V**
Input Voltage, V_{IN} .... **5.5 V**

QUAD DARLINGTON SWITCHES

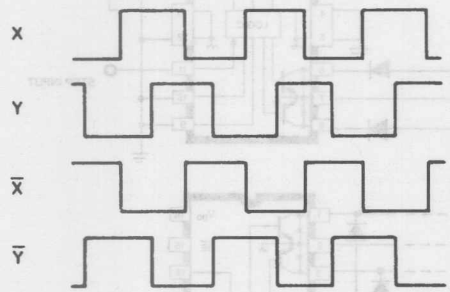
The UDN2878W and UDN2879W drive motor windings at up to 200 watts per channel. The integrated circuits include transient-suppression diodes and input logic that is compatible with most TTL, LS TTL, and 5 V CMOS. The 12-pin single in-line power-tab package allows maximum power-handling capability.

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Load Voltage, V_{CC} (UDN2878W)	**35 V**
(UDN2879W)	**50 V**
Continuous Output Current, I_C	**4 A**
Peak Output Current, I_{CP}	**5 A**
Logic Supply Voltage Range, V_S	**4.5 V to 7.0 V**
Input Voltage, V_{IN}	**V_S**

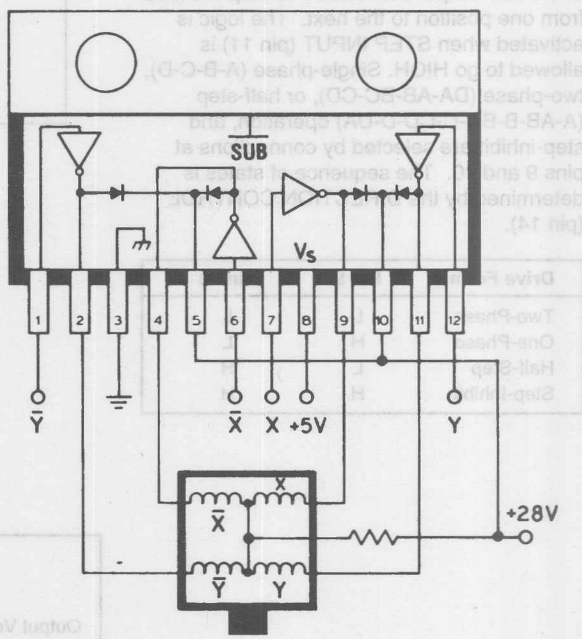
STEPPER-MOTOR DRIVE

2-PHASE, UNIPOLAR INPUT WAVEFORMS



Dwg. No. A-11,795

UDN2878W



Dwg. No. A-11,975

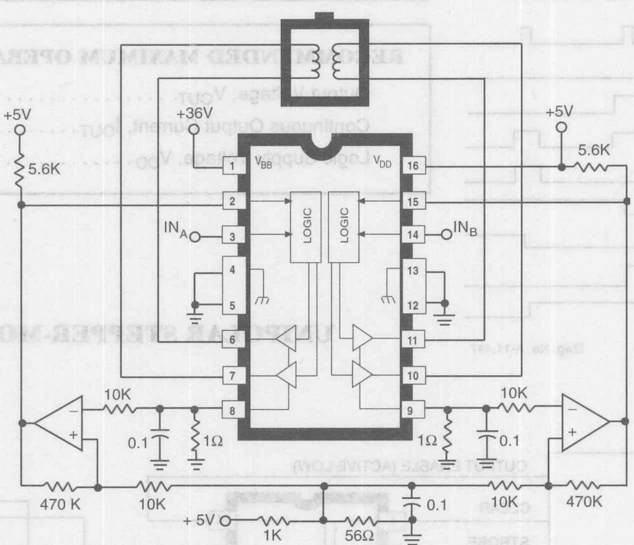
DUAL FULL-BRIDGE MOTOR DRIVER

The UDN2993B motor driver contains two independent full-bridges capable of operating with load currents of up to 600 mA. An internally generated deadtime prevents potentially destructive crossover currents when changing load phase. Internal transient-suppression diodes are included for use with inductive loads. Emitter outputs allow for current sensing in pulse-width modulated applications.

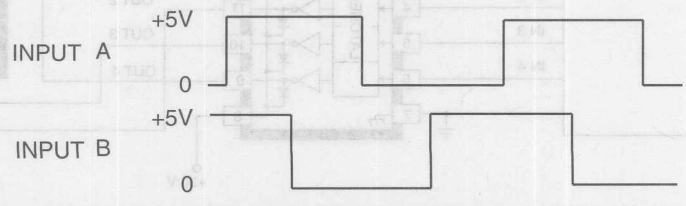
RECOMMENDED MAXIMUM OPERATING CONDITIONS

Load Voltage Range, V_{BB} .... **10 V to 40 V**
Output Current, I_{OUT} .... **±500 mA**
Logic Voltage Range, V_{DD} .... **4.5 V to 5.5 V**

2-PHASE BIPOLAR STEPPER-MOTOR DRIVE
(Pulse-Width Modulated)

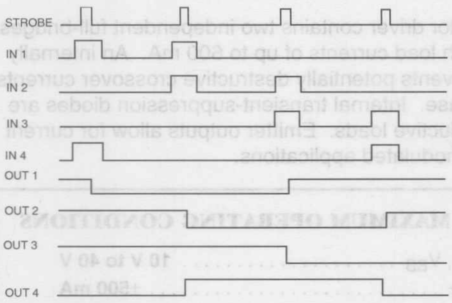


Dwg. No. A-12,453



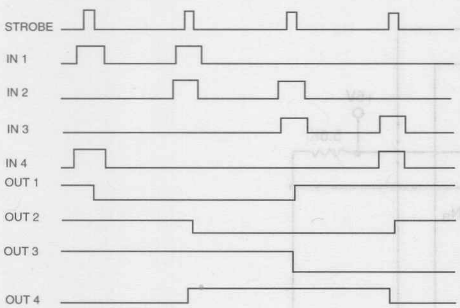
Dwg. No. A-12,454

UNIPOLAR WAVE DRIVE



Dwg. No. A-11,446

UNIPOLAR 2-PHASE DRIVE



Dwg. No. A-11,447

BiMOS UNIPOLAR MOTOR DRIVERS

Driving unipolar motors is one of many successful applications for the UCN5800A and UCN5801A BiMOS II latched sink drivers.

All devices contain CMOS data latches, CMOS control circuitry, high-voltage, high-current bipolar Darlington outputs, and output transient protection diodes for use with inductive loads.

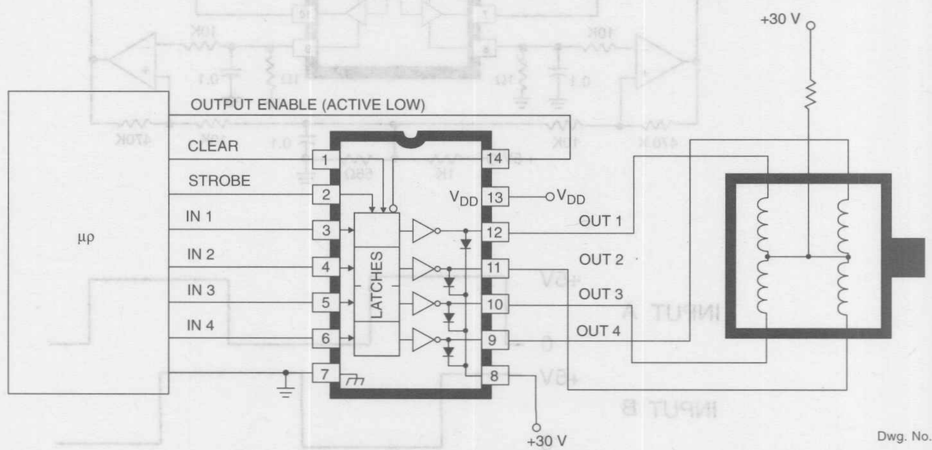
The UCN5800A is a direct replacement for the original UCN4401A. The UCN5801A replaces the UCN4801A. With a 5 V supply, BiMOS II devices typically operate at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable.

Device	Package	Drivers	Features
UCN5800A	14-pin DIP	4	Clear, Strobe, Output Enable
UCN5801A	22-pin DIP	8	Clear, Strobe, Output Enable

RECOMMENDED MAXIMUM OPERATING CONDITIONS

Output Voltage, V_{OUT} . . . . 35 V
Continuous Output Current, I_{OUT} . . . . 350 mA
Logic Supply Voltage, V_{DD} . . . . 4.5 V to 12 V

UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. No. B-1537

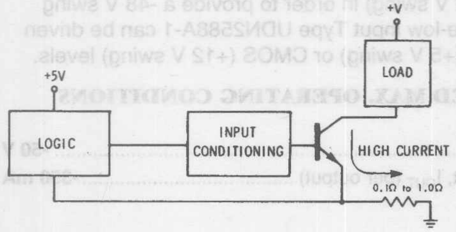
APPLICATIONS INFORMATION

INTEGRATED CIRCUITS FOR CURRENT-SOURCING APPLICATIONS

During recent years, the appearance of many new low-power monolithic devices (LSI and microprocessors) has created an increased need of peripheral power driver integrated circuits. Interface drivers are typically categorized in terms of their output-drive functions. When current flows out of the driver output terminal and into the load, the device is said to "source" current. Conversely, current flows from a load into a "sink" driver.

Integrated source drivers usually consist of high-voltage PNP devices and high-power NPN Darlington outputs (which provide PNP-type action), with input-level shifting. These power ICs are useful for interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps (incandescent, LED, neon), motors, and displays (gas-discharge, LED, vacuum-fluorescent). They can also be used to provide multi-channel buffers for discrete power semiconductors.

FLOATING LOGIC-GROUND LEVEL
(Sink Driver)

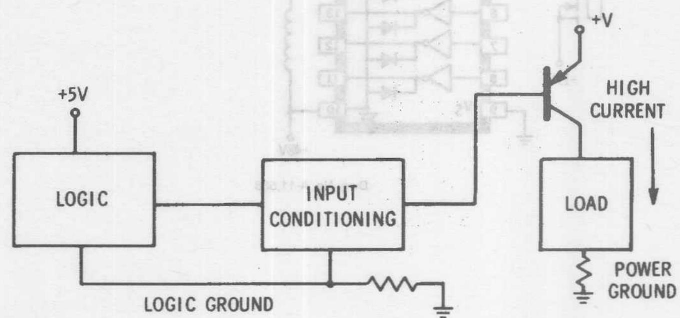


Dwg. No. A-11,532

The advantages of source drivers for display interface are quite evident. The X-Y addressing of most readouts requires both source and sink functions to minimize pin count, interconnections, and package count.

A more subtle advantage of source drivers is related to their use with inductive loads or incandescent lamps. Both types of load generate troublesome transients and noise currents on common logic/load ground lines. In addition, high ground currents can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

SEPARATE GROUND RETURNS
(Source Driver)



Dwg. No. A-11,531

RELAY-DRIVER APPLICATIONS

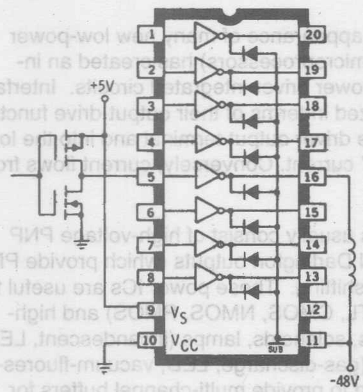
Series UDN2580A, eight-channel source drivers provide current/voltage translation from TTL, positive CMOS, or negative CMOS logic to -48 V telecommunication relays requiring less than 350 mA. All devices have internal inductive-load transient-suppression diodes.

Type UDN2580A is best driven from negative-reference CMOS or NMOS logic (-5 V or -12 V swing) in order to provide a -48 V swing at the output. The active-low input Type UDN2588A-1 can be driven from positive logic TTL (+5 V swing) or CMOS (+12 V swing) levels.

RECOMMENDED MAX. OPERATING CONDITIONS

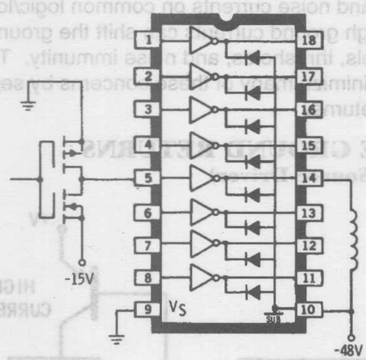
Supply Voltage, V_{EE} .... -50 V
Continuous Output Current, I_{OUT} (per output) .... -350 mA

TELECOMMUNICATIONS RELAY DRIVER
(Positive logic)



Dwg. No. A-11,524

TELECOMMUNICATIONS RELAY DRIVER
(Negative logic)



Dwg. No. A-11,538

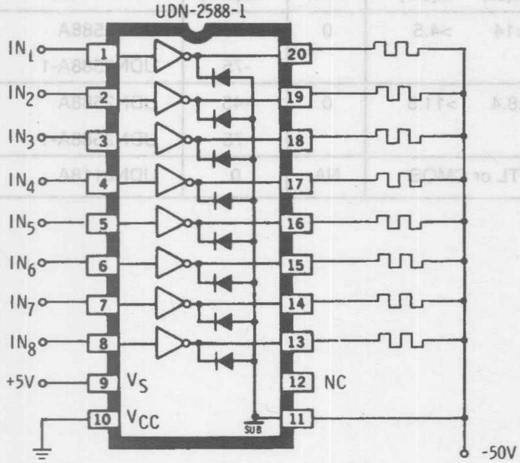
PRINTER APPLICATIONS

Source drivers have been used extensively in electrosensitive, thermal, and impact printer applications. Multi-channel devices in the Series UDN2580A and UDN2980A reduce parts count and provide up to 350 mA per output at voltages up to 75 V (resistive load). Copper lead frames make these devices capable of simultaneously delivering up to 125 mA continuously from all eight channels at an ambient temperature of +50°C.

RECOMMENDED MAX. OPERATING CONDITIONS

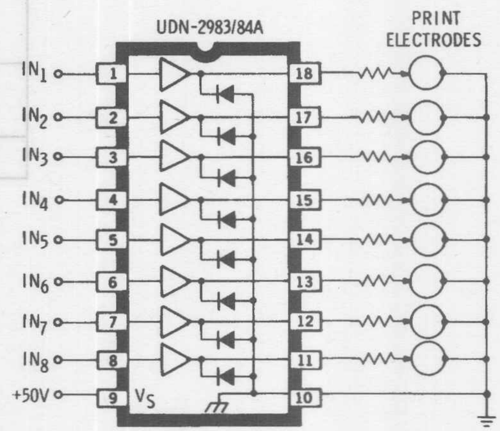
Supply Voltage Range, V_S
UDN2588A-1 .... to 75 V
UDN2981A and UDN2982A .... 5 V to 45 V
UDN2983A and UDN2984A .... 35 V to 75 V
Logic Voltage, V_{IN} .... 12 V
Continuous Output Current, I_{OUT} (per output) .... -350 mA
Peak Output Current, I_{OP} .... - 500 mA

THERMAL PRINTER APPLICATION



Dwg. No. A-11,530

ELECTROSENSITIVE PRINTER APPLICATION



Dwg. No. A-11,529

VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS

Series UDN6100A and UDN2580A source drivers provide solutions to problems encountered in driving higher-voltage vacuum-fluorescent and planar gas-discharge displays. Both series of parts provide TTL, CMOS, and NMOS input-logic compatibility. Series UDN6100A devices are active high (non-inverting) drivers. Series UDN2580A drivers are active low (inverting) devices.

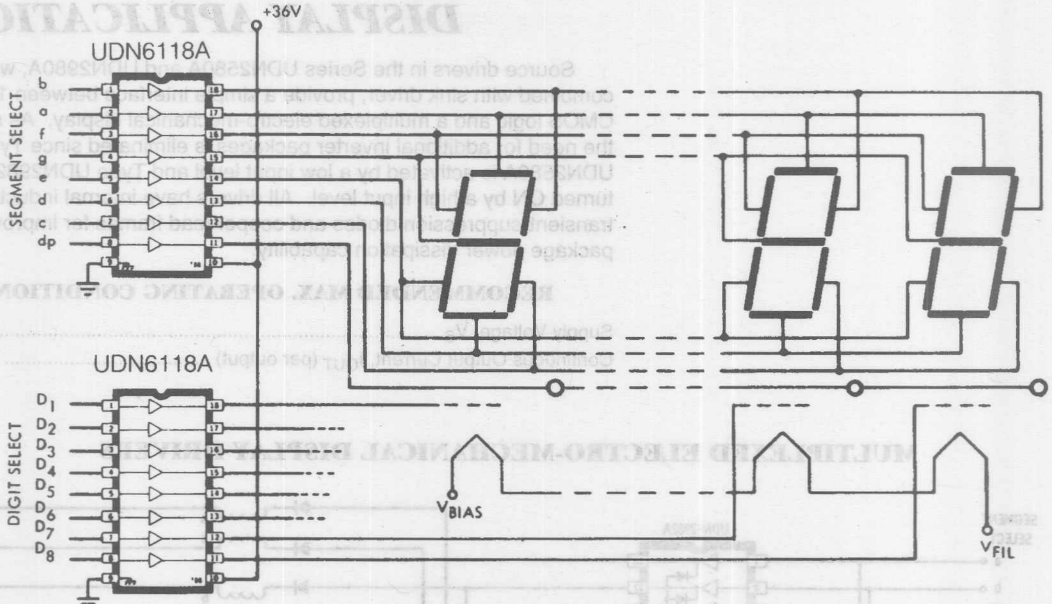
At minimum cost, UDN6118A devices offer 85 V output breakdowns for vacuum-fluorescent displays typically utilizing less than 40 characters. Featuring a minimum 80 V output breakdown voltage, UDN6118A drivers guarantee 25 mA per output. UDN6118A drivers include internal pull-down resistors and provide operation from single-ended positive supplies.

For vacuum-fluorescent display applications requiring a higher current capability (operating several displays with common drive circuitry), Type UDN2588A can be used with appropriate external output pull-down resistors to provide up to 350 mA per output.

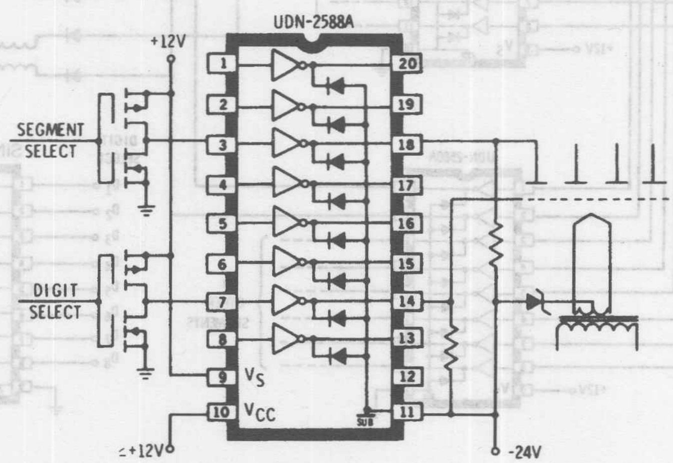
MAXIMUM OPERATING VOLTAGES

V_S V_{BB}	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
+5	<14	>4.5	0	-45	UDN2588A
				-75	UDN2588A-1
+12	<8.4	>11.5	0	-45	UDN2588A
				-75	UDN2588A-1
+80	TTL or CMOS		NA	0	UDN6118A

MULTIPLEXED VACUUM-FLUORESCENT DISPLAY DRIVERS



Dwg. No. A-11,522



Dwg. No. A-11,526

ELECTRO-MECHANICAL DISPLAY APPLICATIONS

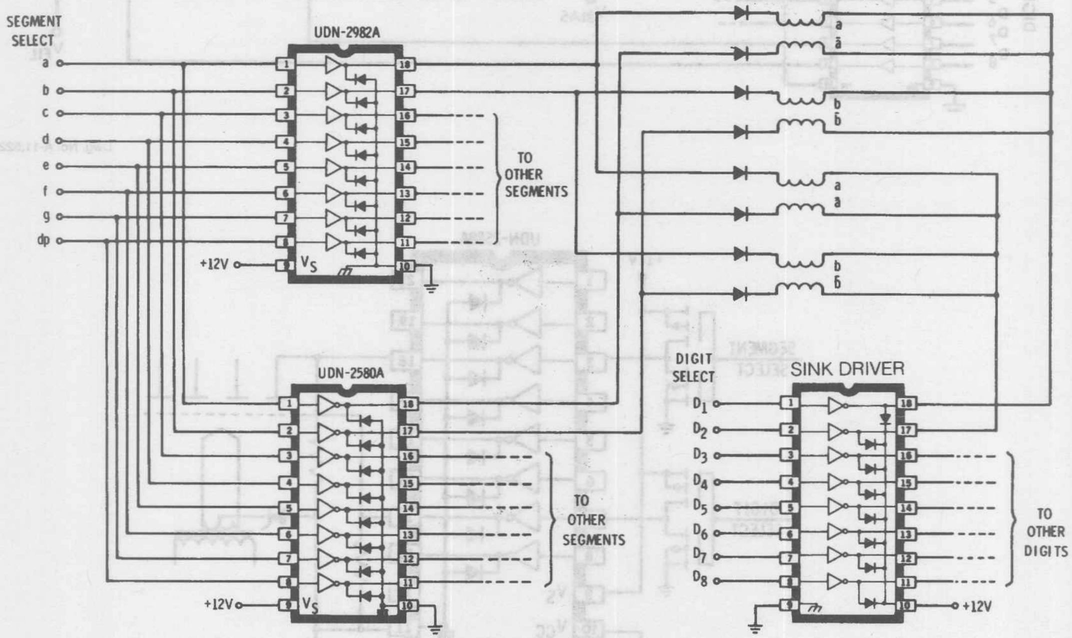
Source drivers in the Series UDN2580A and UDN2980A, when combined with sink driver, provide a simple interface between 12 V CMOS logic and a multiplexed electro-mechanical display. As shown, the need for additional inverter packages is eliminated since Type UDN2580A is activated by a low input level and Type UDN2982A is turned ON by a high input level. All drivers have internal inductive-load transient-suppression diodes and copper lead frames for improved package power dissipation capability.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S .... **35 V**

Continuous Output Current, I_{OUT} (per output) .... **-350 mA**

MULTIPLEXED ELECTRO-MECHANICAL DISPLAY DRIVERS



Dwg. No. B-1476

LIGHT-EMITTING DIODE APPLICATIONS

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S	
UDN2585A	**15 V**
UDN2982A	**45 V**
Continuous Output Current, I_{OUT} (per output)	
UDN2585A	**-120 mA**
UDN2982A	**-350 mA**
Input Voltage, V_{IN}	**15 V**

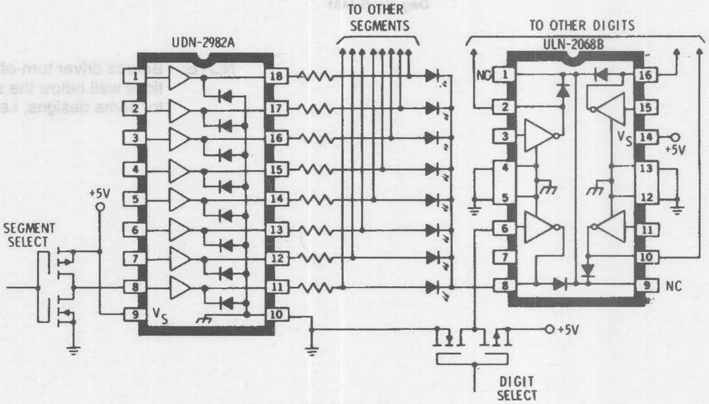
Series UDN2580A and Series UDN2980A 8-channel source drivers provide monolithic solutions to problems associated with driving multiplexed LED displays in common-cathode or common-anode configurations.

Type UDN2585A is a non-Darlington inverting (input low = output high) source driver that is frequently used as a segment or dot driver in a common-cathode LED display where multiplexed segment or dot currents do not exceed 120 mA. This device features input logic-level compatibility with open-collector TTL, standard TTL, CMOS, and NMOS, as well as low output saturation voltages.

For common-cathode applications requiring higher segment currents, or for common-anode digit drive applications, Series UDN2980A is recommended. This non-inverting (input high = output high) series features 350 mA per output continuous current ratings with peak currents reaching 500 mA per output. Outputs may be paralleled for higher current capability. Type UDN2982A is logic-compatible with 2.4 V output levels of TTL and CMOS. Similar high output current ratings, for use in inverting applications, are offered by the Type UDN2580A driver.

Combining source drivers with multi-channel, high-current sink drivers (such as Type ULN2068B or UDN2595A provides simple, compact, and economical solutions to driving high-current multiplexed LED displays.

COMMON-CATHODE LED DISPLAY

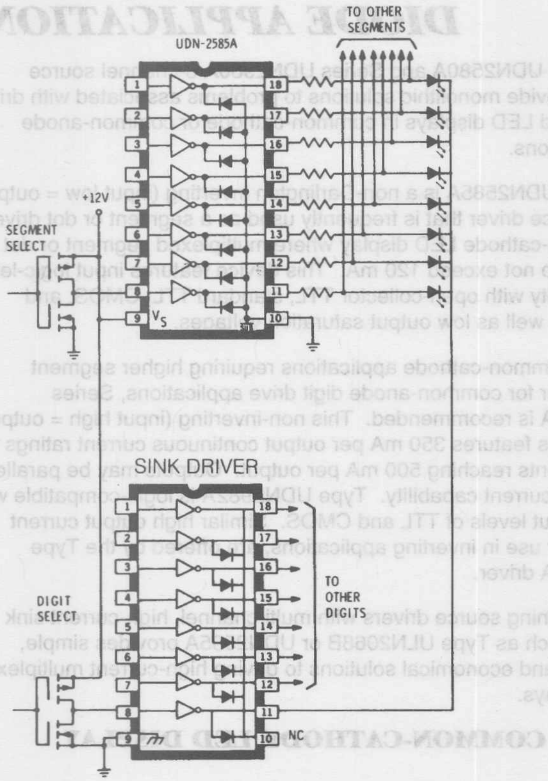


COMMON-CATHODE LED DISPLAY

Dwg. No. 1473A

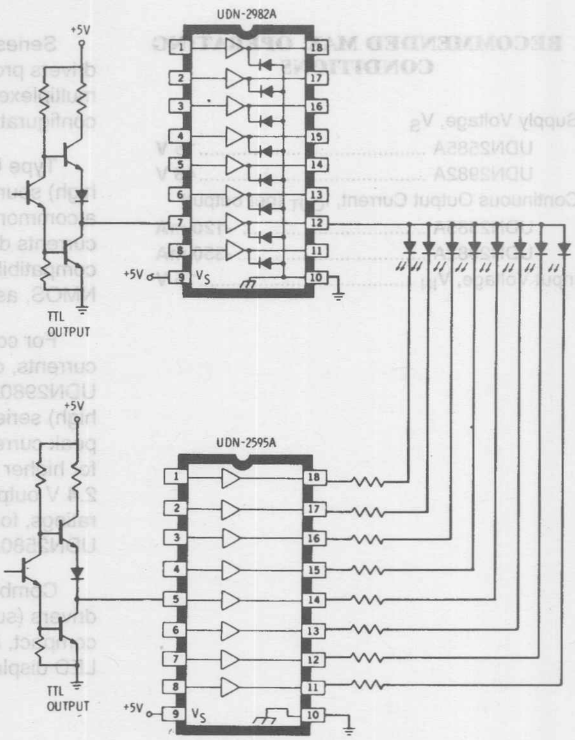
CURRENT-SOURCING APPLICATIONS

COMMON-CATHODE LED DISPLAY



Dwg. No. B-1481

COMMON-ANODE LED DISPLAY



Dwg. No. B-1480

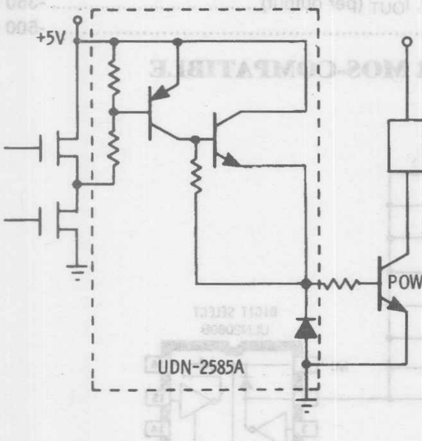
NOTE: Source driver turn-off delay is influenced by load conditions. System applica tions well below the specified output loading may require timing considerations for some designs, i.e., to prevent "ghosting" in multiplexed displays.

MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

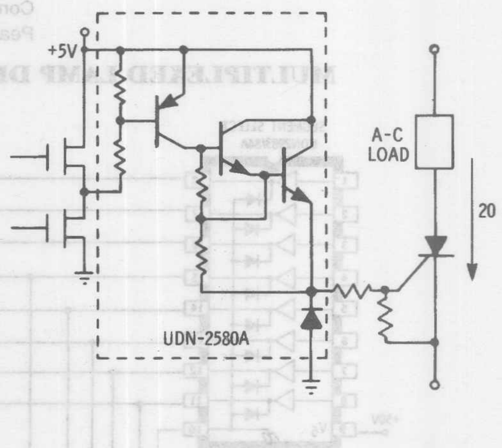
Source drivers can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, a UDN2580A 8-channel source driver can provide up to 350 mA of pre-drive current into the base of power NPN devices, making 5 A load currents readily available. Higher load currents can be obtained by using power NPN Darlington devices.

For a-c loads, it is possible to use a source driver to provide gate current (with appropriate current-limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors at up to 20 A.

DRIVER FOR HIGH-POWER DISCRETE DEVICES



Dwg. No. A-11,533



Dwg. No. A-11,534

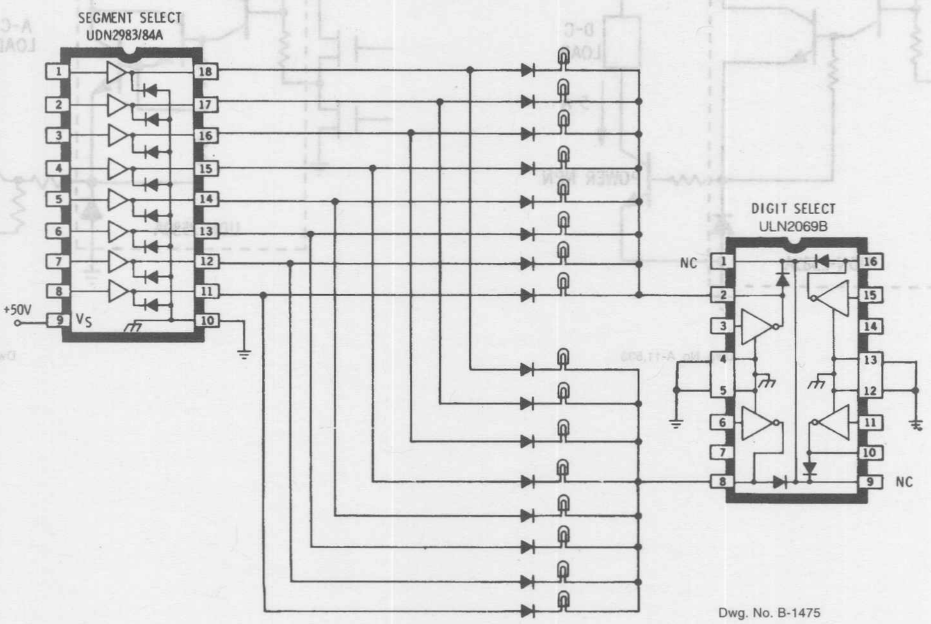
INCANDESCENT LAMP DRIVER APPLICATIONS

Driving multiplexed incandescent lamps at voltages up to 75 V with peak currents approaching 500 mA per segment, Series UDN2980A eight-channel source drivers, when combined with Type ULN2069B sink drivers, provide for a very cost-effective approach. Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ (N = the number of digits) times the nominal d-c voltage, to obtain sufficient brightness. For example, a four-digit, 28 V display requires 56 V to operate satisfactorily. In addition, care must be taken to select a proper driver to withstand the substantial inrush currents created by cold filaments. Peak currents of up to ten times the nominal operating currents have been observed. Multiplexed lamps must also incorporate diodes to prevent series/parallel paths to unaddressed elements.

RECOMMENDED MAX. OPERATING CONDITIONS

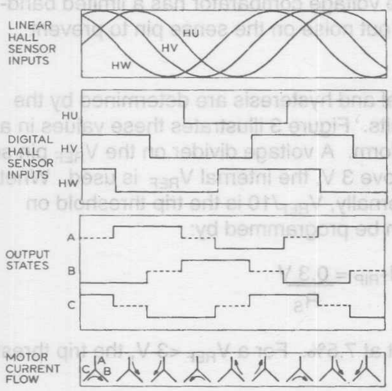
Supply Voltage Range, V_S	
UDN2981A and UDN2982A	5 V to 45 V
UDN2983A and UDN2984A	35 V to 75 V
Continuous Output Current, I_{OUT} (per output)	-350 mA
Peak Output Current, I_{OP}	-500 mA

MULTIPLEXED LAMP DRIVER, TTL- OR MOS-COMPATIBLE



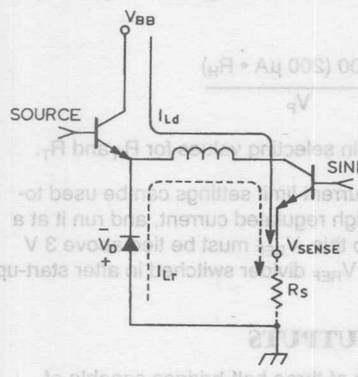
APPLICATIONS INFORMATION

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER



Dwg. No. A-14,146

FIGURE 1



Dwg. No. A-14,147

FIGURE 2

Three-phase brushless dc motors are especially useful because they have no brushes to make noise, dust, or wear out. The brushes of a conventional motor have been replaced by position sensors, usually Hall effect or optical devices. These sensors detect the rotor position with respect to the stator windings. This information is used to drive the windings in a sequence synchronized with the rotor position, called commutation. To use a three-phase brushless motor usually requires custom ICs to perform the commutation, and discretes for drivers. Then, to control the motor current, and with it speed and torque, requires pulse width modulation circuitry. All this adds up to many components and an expensive solution.

Now, due to progress in integrated power technology, all of the functions needed to drive three phase brushless motors can be performed by one chip. The UDN2936W incorporates Hall effect sensor decoding logic, power outputs capable of driving 2 A continuous at 45 V, PWM current limiting, direction control, dynamic braking, and integrated protection features. This device can be used to provide a simple, inexpensive, and reliable solution to the problem of driving brushless dc motors.

OVERALL CHIP STRUCTURE

The UDN2936W is made up of five sections, namely the commu-tation logic, output drivers, current limiting, direction and braking, and thermal shutdown. All logic and power functions utilize only bipolar processing, which allows for high power with an efficient use of die area.

MOTOR COMMUTATION

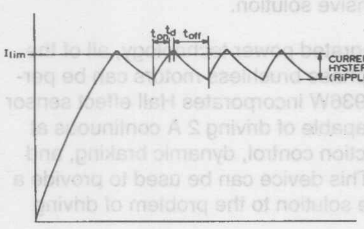
In a three-phase motor, winding current must be synchronized to rotor position to run the motor efficiently, i.e., with unidirectional torque. Hall effect sensors detect rotor position, which must be decoded to drive the coils in the proper sequence. Hall effect sensors produce low level differential analog outputs. Today's Hall effect ICs amplify this signal to make it easier to use. These Hall effect ICs produce either large signal ac linear waveforms, or open collector digital signals. The UDN2936W is compatible with both types of Hall effect ICs.

Position of the Hall effect sensors determines the decoding sequence to produce the correct driving waveforms for each motor. The decoding sequence programmed into this device is based on Hall effect cells 60 electrical degrees apart. This 60 degree sequence is one of the most common used in the industry. The truth table and timing waveforms found in Figure 1 illustrate how the Hall cell inputs, driving output waveforms, and motor currents states are interrelated.

Motors with other commutation sequences can typically be accommodated by inverting one of the position inputs.

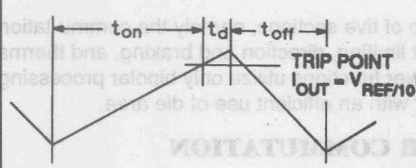
CHOPPING CURRENT CONTROL

The current limit technique chops the source drivers to control the load current level. The maximum current and percentage ripple, or hysteresis, can be programmed by the user or left to internal default values. Source chopping produces a continuous sense voltage (see Figure 2), so this voltage is an accurate representation of load current, even during recirculation. Also, chopping only the sources produces a fast current charge-up and a slower current decay. This occurs because of the different voltages across the coil in both states, and results in a controllable current waveform. The chopping method functions as follows: When the current reaches I_{TRIP}, the source is disabled and the current recirculates through a sink driver and a clamp diode. The motor current decays a fixed percentage, the source is enabled again, and the cycle repeats. The internal sense voltage comparator has a limited bandwidth that essentially filters out noise on the sense pin to prevent erroneous chopping.



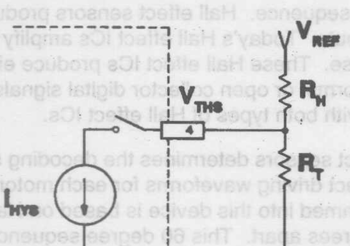
Dwg. No. A-14,148

FIGURE 3A



Dwg. No. A-14,149

FIGURE 3B



Dwg. No. A-14,150

FIGURE 4

The limiting current level and hysteresis are determined by the user or left to internal defaults. Figure 3 illustrates these values in a typical output current waveform. A voltage divider on the V_{REF} pin sets the external V_{REF}. If set above 3 V, the internal V_{REF} is used. Whether V_{REF} is set internally or externally, $V_{REF}/10$ is the trip threshold on V_{SENSE}. The default trip can be programmed by:

$$I_{TRIP} = \frac{0.3\ V}{R_S}$$

Default hysteresis is set at 7.5%. For a V_{REF} <3 V, the trip threshold is the following:

$$I_{TRIP} = \frac{V_{REF}}{10\ R_S}$$

In this case, hysteresis is created by drawing 200 μA from the resistor divider when the sources are chopped, lowering the trip theshold a certain percentage. The sources turn back when the sense voltage decays to the new lower threshold. Hystersis is given by this expression:

$$\%hys = \frac{100\ (200\ \mu A \bullet R_H)}{V_P}$$

The graphs in Figure 5 aid in selecting values for R_H and R_T.

The internal and external current limit settings can be used together to start a motor with a high regulated current, and run it at a lower regu-lated current. To do this, V_{REF} must be tied above 3 V when the motor starts, and the V_{REF} divider switched in after start-up (see Figure 6).

OUTPUTS

The output section consists of three half-bridges capable of sourcing or sinking 2 A continuously at a saturation voltage of less than 2 V per driver. They are built to sustain at least 45 V. Source and sink clamp diodes are included to provide a current path during

commuation and chopping. These are high-performance substrate isolated diodes that virtually eliminate the wasteful parasitic substrate currents of conventional diodes. The drivers, both source and sink, are bipolar double level metal Darlingtons.

DIRECTION AND BRAKING

The direction control allows the motor to be reversed even while running. When direction changes polarity, the state of the outputs is reversed, i.e., if the source was ON, the sink will turn ON, and vice versa. Because the turn off times are longer than the turn on times, the drivers turning ON must be delayed by a precise amount to prevent potentially destructive crossover currents. This delay is generated internally.

The brake function uses the back EMF of the motor to brake it dynamically. The windings are effectively 'shorted' together through sink drivers and clamp diodes.

THERMAL SHUTDOWN AND POWER DISSIPATION

The thermal shutdown feature protects the IC from overheating. This circuit turns OFF all drivers at about 165°C, and allows the device to cool down approximately 25°C before turning ON again.

The device is packaged in a 12-pin power SIP that has a large copper tab for excellent heat dissipation. The design of the tab, and the fact that it is at ground, make the package easy to use with a heat sink. The maximum allowable power dissipation in 25°C ambient air without a heat sink is 5.2 W. With minimal heat sinking, dissipation greater than 10 W can be accomplished.

APPLICATION

The application shown in Figure 7 is a simple one illustrating the use of the UDN2936W in an open-loop situation with bilevel current limiting. The motor uses digital open-collector Hall cells such as the UGN3113U or linear Hall effect ICs such as the UGN3503U. These Hall effect sensors

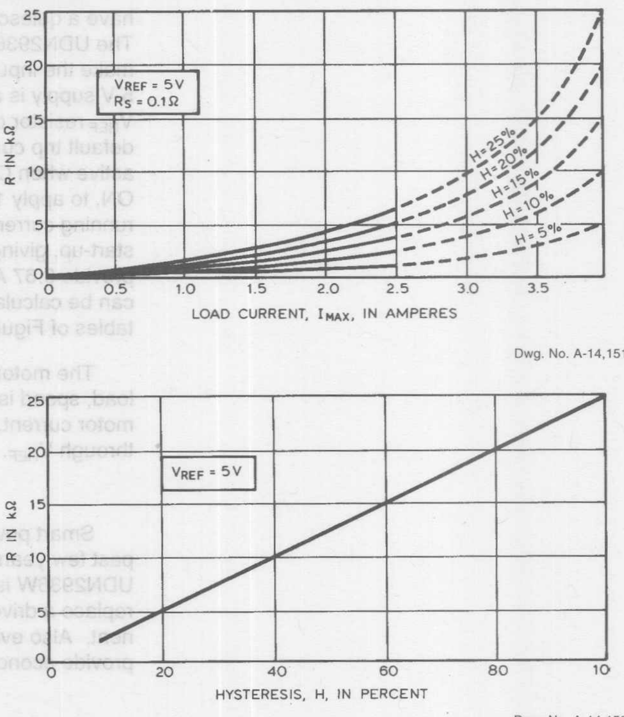


FIGURE 5

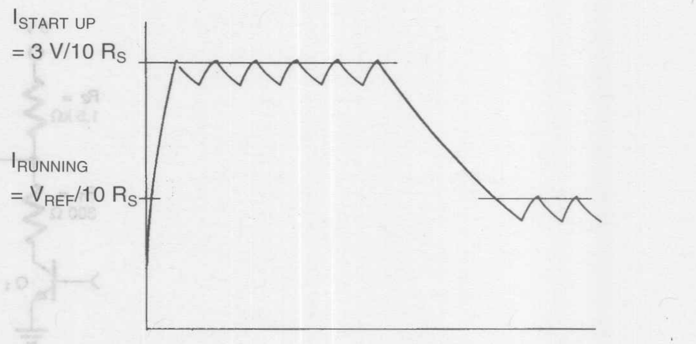


FIGURE 6

have a quiescent output voltage of 2.5 V, and emitter follower outputs. The UDN2936W has a regulated internal 2.5 V reference designed to make the inputs compatible with those linear Hall effect sensors. The 5 V supply is also used as a reference in the current limiting for the V_{REF} resistor divider. Choosing R_S = 0.15 ohms results in internal default trip current of 2 A, and 7.5% ripple. This internal limiting is active when Q1 is OFF. R1 and R2 form a resistor divider, when Q1 is ON, to apply 1 V to the V_{REF} input, producing 0.67 A of regulated running current and 5% ripple. Typically, Q1 would be OFF during start-up, giving 2 A of regulated start-up current, and then turned ON to provide 0.67 A of running current. The values of R_1, R_2, and V_{SENSE} can be calculated using the circuit and equations of Figure 5, or the tables of Figure 6.

The motor speed is controlled by the current limiting. For a given load, speed is proportional to torque, and torque is proportional to motor current. Subsequently, the motor speed can be controlled through V_{REF}.

CONCLUSION

Smart power integrated circuits have come a long way in the past few years in solving numerous motor driving problems. The UDN2936W is one example of how integrated monolithic devices can replace a drive circuit of many components with one reliable component. Also evident is the fact that bipolar transistors continue to provide economic solutions in the high current application.

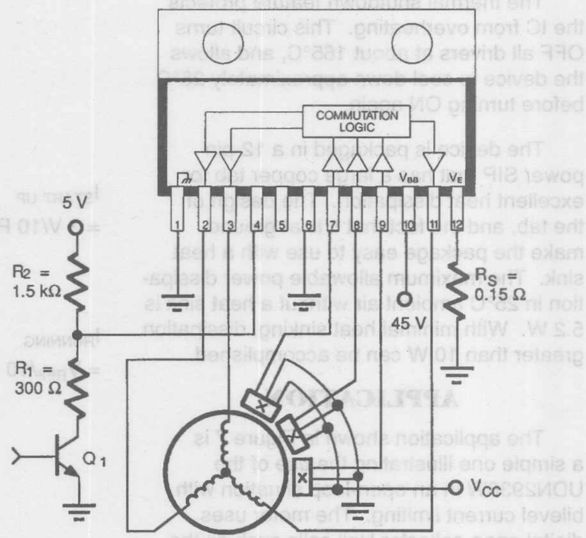


FIGURE 7

APPLICATIONS INFORMATION

SERIES 5800
BiMOS II POWER DRIVERS

INTRODUCTION

The second generation of merged CMOS/bipolar integrated circuits extends the lead in innovative interface forged by the original BiMOS power drivers.

Higher-density CMOS logic gives BiMOS II integrated circuits improved switching speeds at reduced costs. With a 5 V supply, second generation BiMOS typically operates at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. The BiMOS II series also offers new and improved functions.

Reliable, single-chip BiMOS II solutions are available for a wide variety of peripheral and power interface problems. Two or more devices are no longer required to interface low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as LEDs, gas-discharge or vacuum-fluorescent displays, relays, solenoids, thermal printers, motors, impact printer hammers, and incandescent lamps. Since all BiMOS devices include logic and control in addition to power functions, they also free the microprocessor from many housekeeping tasks.

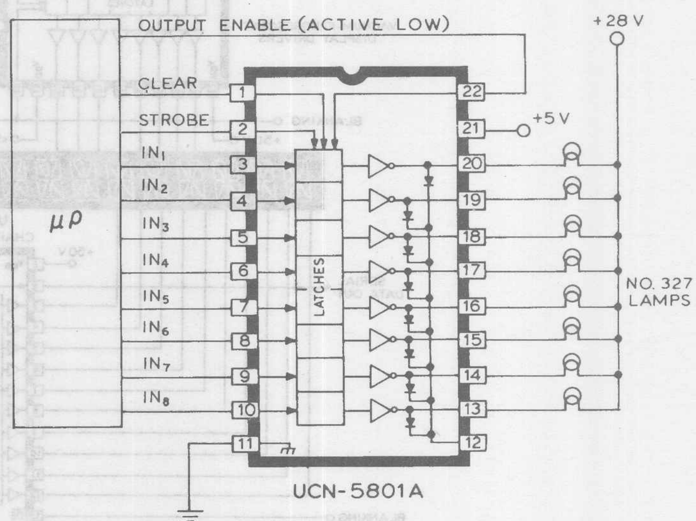
INCANDESCENT LAMP DRIVERS

Each of the UCN5800— or UCN5801— open-collector Darlington outputs will sink up to 500 mA and will sustain at least 50 V in the OFF state. The high peak current rating of these devices allows their use with the high inrush (10 x) currents normally associated with incandescent lamps. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximun current: Either a reduction in output current or a suitable combination of duty cycle and number of active outputs is usually required.

The UCN5800A is supplied in a standard 14-pin DIP; the UCN5800L is supplied in a 14-lead SOIC. The UCN5801A is furnished in a 22-pin DIP with 0.400" row spacing; the UCN5801EP is supplied in a 28-lead PLCC.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	**45 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**350 mA**



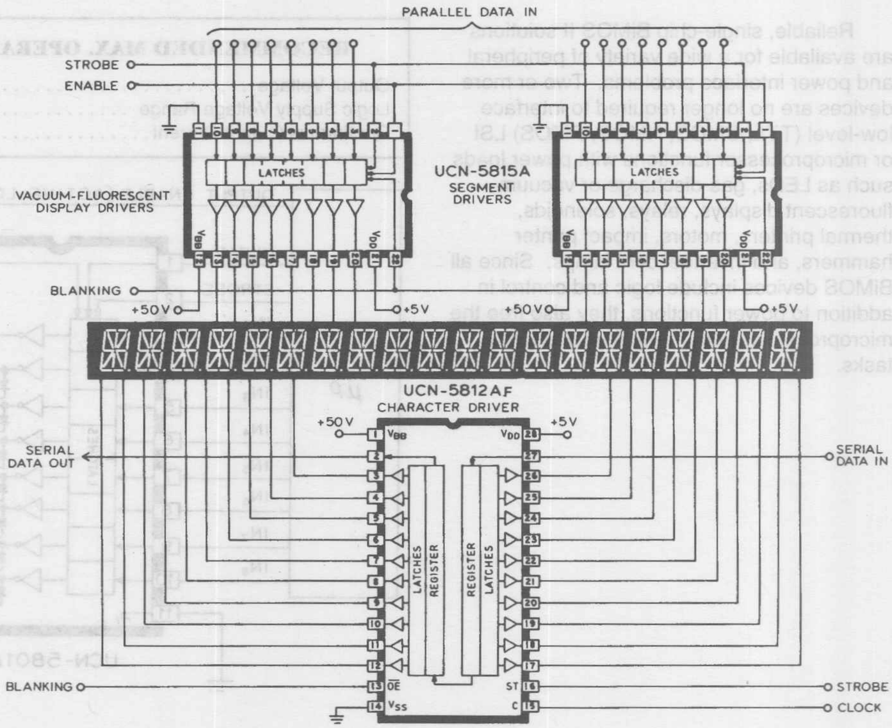
Dwg. A-12,550

VACUUM-FLUORESCENT DISPLAY DRIVERS

The UCN5815A 8-bit, latched, source driver provides a practical means of driving the segments, dots (matrix panel), or bars of multiplexed high-voltage vacuum-fluorescent displays. The UCN5810—F (10-bit), UCN5811A (12-bit), UCN5812—F (20-bit), or UCN5818—F (32-bit) serial-input latched source drivers are well-suited for use as character or digit drivers. The high-voltage versions (suffix-1) can also be used to drive the anodes of planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	
UCN5810AF/EPF/LWF, UCN5811A, UCN5812AF/EPF, UCN5818AF/EPF	55 V
UCN5810LWF-1	75 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	-25 mA



Dwg. D-1112

MULTIPLEXED INCANDESCENT LAMP DRIVERS

In order to obtain brightness equivalent to normal dc operation, multiplexed incandescent displays must be operated at a voltage:

$$E_{MPX} = E_{DC} \sqrt{N}$$

where E_{MPX} = the recommended operating supply voltage,

E_{DC} = the rated dc lamp voltage, and

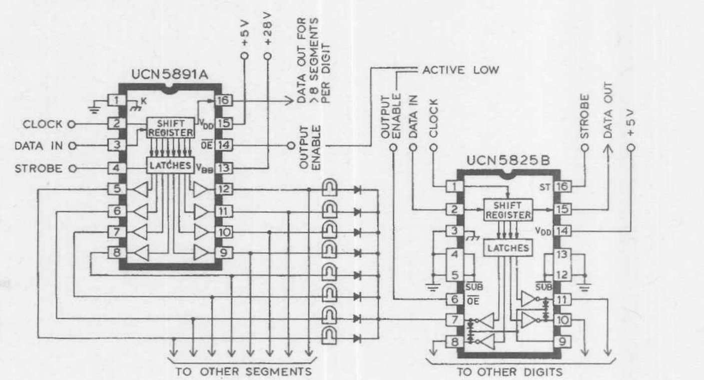
N = the number of digits being multiplexed.

Multiplexed lamps also require isolation diodes to prevent sneak series/parallel paths to unaddressed elements.

Serial-input, latched source drivers provide simple, compact, and economical segment drivers for mutiplexed incandescent lamp applications. The UCN5890A and UCN5891A feature high-voltage, high-current (500 mA, peak) Darlington outputs. The UCN5895A/EP have saturated outputs for minimum voltage drop and will source up to 250 mA per driver. The drivers are supplied in an economical 16-pin "A" package or 20-lead "EP" package. The UCN5890, UCN5891, and UCN5895 are pin-compatible except for output ratings.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	
UCN5890A	**75 V**
UCN5891A	**45 V**
UCN5895A/EP	**45 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	
UCN5890A	**-350 mA**
UCN5891A	**-350 mA**
UCN5895A/EP	**-120 mA**



Dwg. B-1541

MULTIPLEXED LED DRIVERS

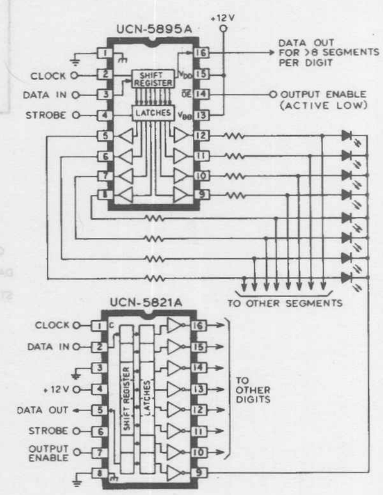
Latched source drivers are simple, compact, and economical segment drivers for multiplexed LED and incandescent and lamp applications. The UCN5895A/EP feature saturated outputs for minimum voltage drop. It sources a minimum of 120 mA per driver. The source driver is supplied in an economical 16-pin ‘A’ package.

A typical common-cathode LED display driver application is shown below. The high-current UCN5821A, a latched sink driver, is used to drive the digits. Common-anode LED displays would require the use of the UCN5891A source driver and UCN5821A sink driver.

In order to obtain sufficient brightness, multplexed LED displays must typically be operated at greatly increased current. Appropriate current limiting is required.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	
UCN5821A	45 V
UCN5890A	75 V
UCN5891A	45 V
UCN5895A/EP	45 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	
UCN5821A	350 mA
UCN5890A	-350 mA
UCN5891A	-350 mA
UCN5895A/EP	-120 mA



Dwg. B-1541

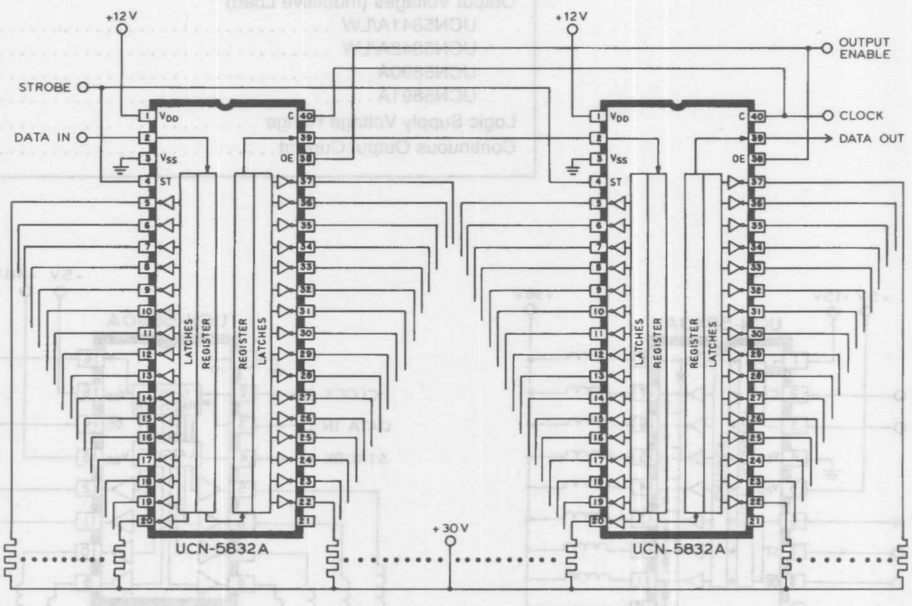
THERMAL PRINTHEAD DRIVER

Designed primarily for use with thermal printheads, the UCN5832A/EP are optimized for low output-saturation voltage and high-speed operation. Each device has 32 bipolar, open-collector saturated outputs, a CMOS data latch for each driver, a 32-bit CMOS shift register, and CMOS control circuitry. A CMOS serial data output allows these devices to be cascaded in applications requiring more than 32 bits.

The UCN5832A is supplied in a 40-pin DIP with 0.600" row spacing; the UCN5832EP is supplied in a 44-lead PLCC. Under normal conditions, all outputs will sustain 100 mA continuously without derating. They can also be supplied in unpackaged chip form or in a leaded chip carrier.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	**40 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**100 mA**



Dwg. D-1113

RELAY AND SOLENOID DRIVERS

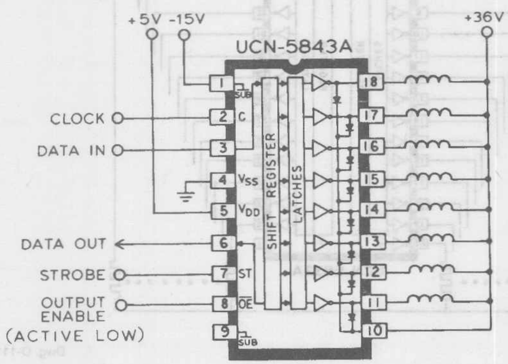
BiMOS II drivers provide an interface flexibility beyond the reach of standard logic buffers and power-driver arrays. Drivers with internal, transient-suppression diodes are ideal for use with relay and solenoid loads.

Series UCN5840A/LW sink drivers feature isolated logic and power grounds that allow split-supply operation or isolated grounds for reduction of transients and noise currents on common logic/load ground lines. The UCN5890A source driver requires load supply voltages of at least 20 V. For lower-voltage operation, the UCN5891A is recommended.

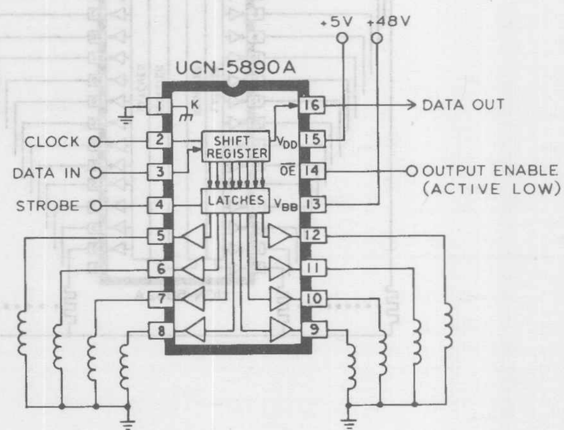
The serial DATA OUTPUT allows cascading for interface applications requiring additional drive lines. The OUTPUT ENABLE can also provide a CHIP ENABLE function that uses a minimum number of drive lines to control output from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltages (Inductive Load)	
UCN5841A/LW	**35 V**
UCN5842A/LW	**50 V**
UCN5890A	**50 V**
UCN5891A	**35 V**
Logic Supply Voltage Range	**5.0 V to 12 V**
Continuous Output Current	**350 mA**



Dwg. A-12,547

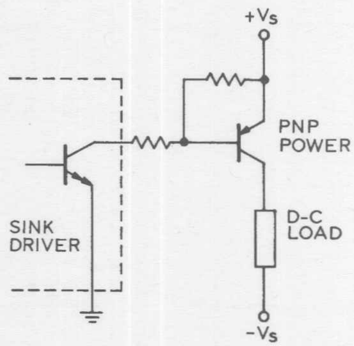


Dwg. A-12,548

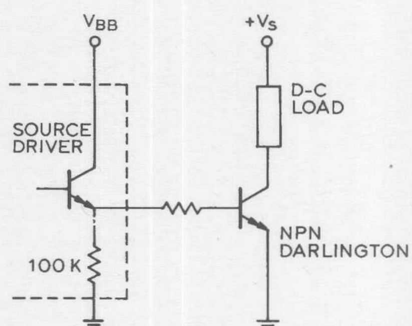
MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

BiMOS II power drivers can also be used as multi-channel pre-drivers for discrete high-current semiconductors, reducing the need for many discrete components. BiMOS II sink drivers provide enough switching current to the bases of discrete PNP power transistors for load currents of up to 20 A. Higher load currents can be obtained by using power Darlington devices. BiMOS II source drivers may require discrete Darlington power drivers for significant load currents, but have the advantage of allowing rather wide load-voltage swings.

For ac loads, source drivers can be used to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical approach to many applications such as driving incandescent lamps or ac motors with current levels of up to 20 A.



Dwg. A-11,744A



Dwg. A-11,745A

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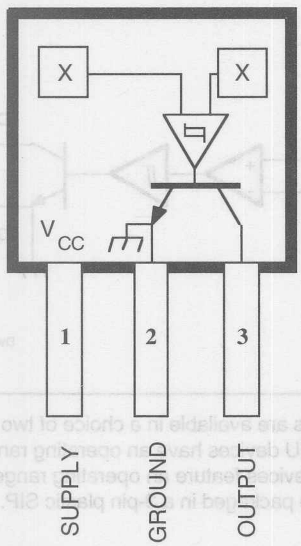
27612A*

3046, 3056, AND 3058

HALL EFFECT GEAR-TOOTH SENSORS–ZERO SPEED



Dwg. PH-012

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . **28 V**
Reverse Battery Voltage,
V_{RCC} . . . . **-30 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . **28 V**
Reverse Output Voltage, V_{OUT} . . . . . **-0.5 V**
Output Current, I_{OUT} . . . . **25 mA**
Package Power Dissipation, P_D . . **500 mW**
Operating Temperature Range, T_A
Suffix "EU" . . . . **-40°C to +85°C**
Suffix "LU" . . . . **-40°C to +150°C**
Storage Temperature Range,
T_S . . . . **-65°C to +170°C**

The A3046EU/LU, A3056EU/LU, and A3058EU/LU Hall effect gear-tooth sensors are monolithic integrated circuits that switch in response to differential magnetic fields created by ferrous targets. These devices are ideal for use in gear-tooth-based speed, position, and timing applications and operate down to zero rpm over a wide range of air gaps and temperatures. When combined with a back-biasing magnet and proper assembly techniques, devices can be configured to give 50% duty cycle or to switch on either leading, trailing, or both edges of a passing gear tooth or slot.

The six devices differ only in their magnetic switching values and operating temperature ranges. The low hysteresis of the A3046/56EU and A3046/56LU makes them perfectly suited for ABS (anti-lock brake system) or speed sensing applications where maintaining large air gaps is important. The A3046EU/LU features improved switch point stability with temperature over the A3056EU/LU. The high hysteresis of the A3058EU and A3058LU, with their excellent temperature stability, makes them especially suited to ignition timing applications where switch-point accuracy (and latching requirements) is extremely important.

Continued next page...

BENEFITS

- Senses Ferrous Targets Down to Zero RPM
- Large Effective Air Gap
- Wide Operating Temperature Range
- Operation from Unregulated Supply
- High-Speed Operation
- Output Compatible With All Logic Families
- Reverse Battery Protection
- Solid-State Reliability
- Resistant to Physical Stress

SELECTION GUIDE

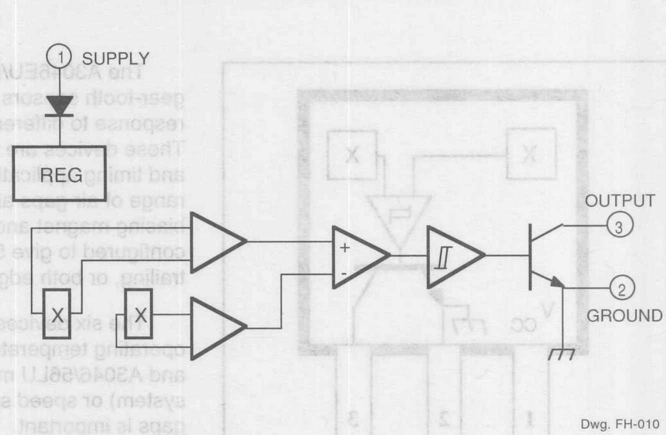
	Switching Hysteresis, B_{OP}-B_{RP}	
	15-90 G	**150-250 G**
Operating Temp. Range	Device Type Number	
-40°C to +85°C	**A3046EU** **A3056EU**	**A3058EU**
-40°C to +150°C	**A3046LU** **A3056LU**	**A3058LU**

3046, 3056, AND 3058
HALL EFFECT GEAR-TOOTH SENSORS–ZERO SPEED

All devices, when used with a back-biasing magnet, can be configured to turn ON or OFF with the leading or trailing edge of a gear tooth or slot. Changes in fields on the magnet face caused by a moving ferrous mass are sensed by two integrated Hall transducers and are differentially amplified by on-chip electronics. The on-chip temperature compensation and Schmitt trigger circuitry minimizes shifts in effective working air gaps and switch points over temperature making these devices ideal for use in ignition timing, anti-lock braking systems, and speed measurement systems in hostile automotive and industrial environments.

Each Hall effect digital Integrated circuit includes two quadratic Hall effect sensing elements, a voltage regulator, temperature compensating circuitry, low-level amplifier, Schmitt trigger, and an open-collector output driver. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The output stage can switch up to 20 mA at conservatively specified repetition rates to 20 kHz and is compatible with bipolar and MOS logic circuits.

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-010

Both magnetic characteristics are available in a choice of two operating temperature ranges. Suffix EU devices have an operating range of -40°C to +85°C while suffix LU devices feature an operating range of -40°C to +150°C. All devices are packaged in a 3-pin plastic SIP.

ELECTRICAL CHARACTERISTICS at V_{CC} = 8 V, over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Power-Up State	—	3058* only, V_{CC} = 0 → 4.5 V, B < B_{OP}		Output is OFF		—
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	135	400	mV
Output Leakage Current	I_{OFF}	V_{CC} = V_{OUT} = 24 V, B < B_{RP}	—	—	5.0	µA
Supply Current	I_{CC}	V_{CC} = 24 V, B < B_{RP}	—	7.2	14	mA
Output Rise time	t_r	R_L = 820 Ω, C_L = 20 pF	—	100		ns
Output Fall time	t_f	R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

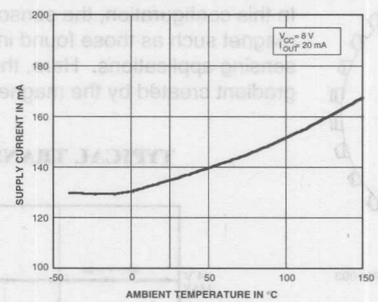
3046, 3056, AND 3058
HALL EFFECT GEAR-TOOTH SENSORS–ZERO SPEED

MAGNETIC CHARACTERISTICS in gauss at V_{CC} = 8 V.

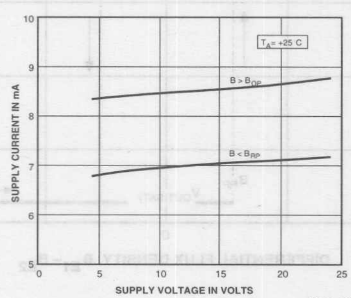
		Part Numbers*								
		3046			3056			3058		
Characteristic	Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
Operate Point, B_{OP}	Output Switches OFF to ON, T_A = +25°C	—	—	150	—	—	150	—	—	250
Release Point, B_{RP}	Output Switches ON to OFF, T_A = +25°C	-150	—	—	-150	—	—	-250	—	—
Hysteresis, B_{hys}	B_{OP}-B_{RP}, T_A = +25°C	15	50	90	15	50	90	150	200	250
Change in Trip Point, ΔB_{OP} or ΔB_{RP}	Over operating temperature range, Ref. B_{OP} or B_{RP} at T_A = +25°C	—	—	±50	—	—	±75	—	—	±50

NOTES: Magnetic switch points are specified as the difference in magnetic fields at the two Hall elements.
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C.
* Complete part number includes the prefix 'A' and a suffix to identify operating temperature range and package style. (see selection guide).

TYPICAL OPERATING CHARACTERISTICS



Dwg. GH-033



Dwg. GH-031

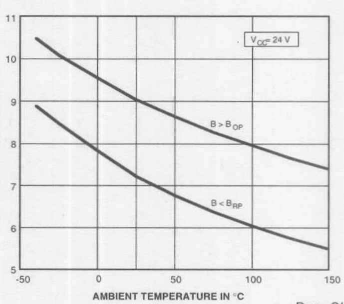


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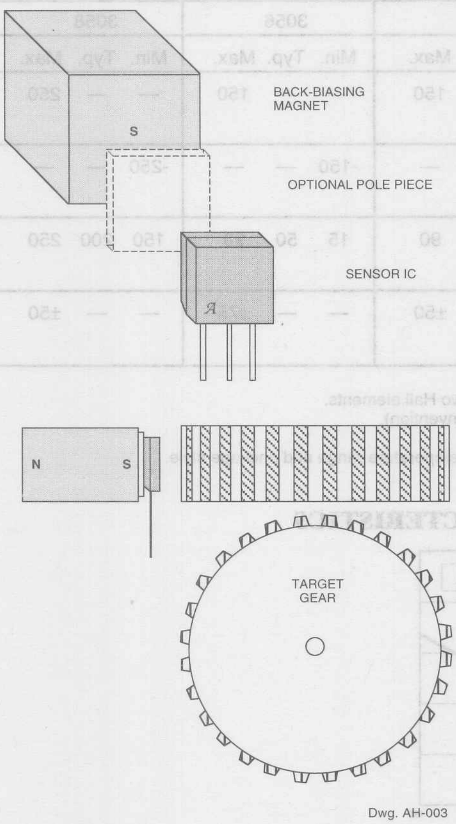
Figure 1
TYPICAL GEAR-TOOTH SENSING APPLICATION



APPLICATIONS INFORMATION

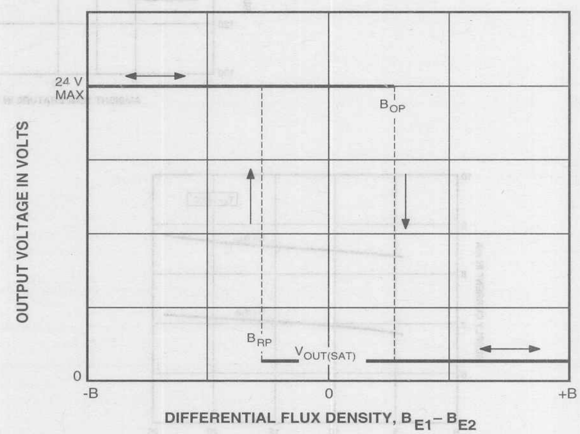
A gear-tooth sensing system consists of the sensor IC, a back-biasing magnet, an optional pole piece, and a target (Figure 1). The system requirements are usually specified in terms of the effective working air gap between the package and the target (gear teeth), the number of switching events per rotation of the target, temperature and speed ranges, minimum pulse duration or duty cycle, and switch point accuracy. Careful choice of the sensor IC, magnet material and shape, target material and shape, and assembly techniques enables large working air gaps and high switch-point accuracy over the system operating temperature range.

Naming Conventions. With a south pole in front of the branded surface of the sensor, a north pole behind the sensor, the field at the sensor is defined as positive. As used here, negative flux densities are defined as less than zero (algebraic convention), e.g., -100 G is less than -50 G.

Magnet Biasing. In order to sense moving non-magnetized ferrous targets, these devices must be back-biased by mounting the unbranded side on a small permanent magnet. Either magnetic pole (north or south) can be used.

The devices can also be used without a back-biasing magnet. In this configuration, the sensor can be used to detect a rotating ring magnet such as those found in brushless dc motors or in speed sensing applications. Here, the sensor detects the magnetic field gradient created by the magnetic poles.

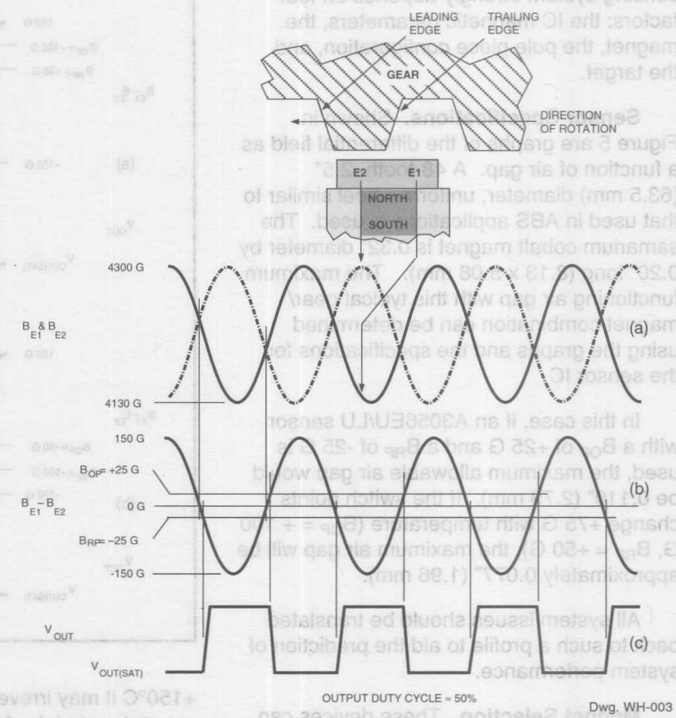
Figure 2
TYPICAL TRANSFER CHARACTERISTIC



Sensor Operation. The A3046EU/LU, A3056EU/LU, and A3058EU/LU sensor ICs each contain two integrated Hall transducers (E1 and E2) that are used to sense a magnetic field differential across the face of the IC (see SENSOR LOCATION drawing). Referring to Figure 2, the trigger switches the output ON (output LOW) when $B_{E1} - B_{E2} > B_{OP}$ and switches the output OFF (output HIGH) when $B_{E1} - B_{E2} < B_{RP}$. The difference between B_{OP} and B_{RP} is the hysteresis of the device.

Figure 3 relates the output state of a back-biased sensor IC, with switching characteristics shown in Figure 2, to the target gear profile and position. Assume a north pole back-bias configuration (equivalent to south pole at the face of the device). The motion of the gear produces a phase-shifted field at E1 and E2 (Figure 3 (a)); internal conditioning circuitry subtracts the field at the two elements (Figure 3 (b)); and the Schmitt trigger at the output of the conditioning circuitry switches at the pre-determined thresholds (B_{OP} and B_{RP}). As shown (Figure 3 (c)), the IC output is LOW whenever sensor E1 sees a (ferrous) gear tooth and sensor E2 faces air. The output is HIGH when sensor E1 sees air and sensor E2 sees the ferrous target.

Figure 3
GEAR-TOOTH SENSOR OPERATION



A gear-tooth sensor can be configured (see ASSEMBLY TECHNIQUES) to operate as a latch, a (positive) switch, or a negative switch. Note the change in duty cycle in each of the cases (Figure 4).

A **latch** is a device where the operate point is greater than zero gauss and the release point is less than zero gauss. With the configuration shown in Figure 3, such a device will switch ON on the leading edge and OFF on the trailing edge of the target tooth.

A **(positive) switch** is a device where both the operate and release points are greater than zero gauss (positive values). In the configuration shown in Figure 3, such a device will switch ON and then switch OFF on the leading or rising edge of the target tooth (Figure 4 (a)).

A **negative switch** is a device where both the operate and release points are less than zero gauss (negative values). In the configuration shown in Figure 3, such a device will switch OFF and then switch ON on the trailing or falling edge of the target tooth (Figure 4 (b)).

Speed sensors can use any of the three sensor configurations described. Timing sensors, however, must use a latch to guarantee dual-edge detection. Latches are most easily made using the A3058EU or A3058LU device types.

SYSTEM ISSUES

Optimal performance of a gear-tooth sensing system strongly depends on four factors: the IC magnetic parameters, the magnet, the pole piece configuration, and the target.

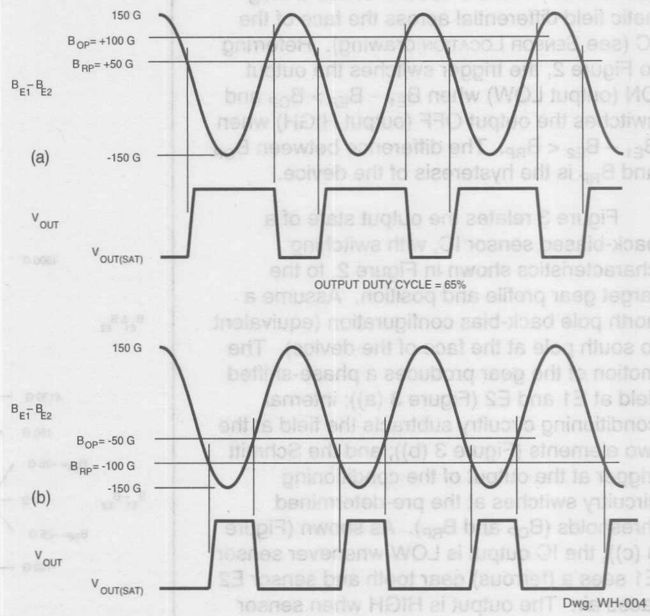
Sensor Specifications. Shown in Figure 5 are graphs of the differential field as a function of air gap. A 48-tooth, 2.5" (63.5 mm) diameter, uniform wheel similar to that used in ABS applications is used. The samarium cobalt magnet is 0.32" diameter by 0.20" long (8.13 x 5.08 mm). The maximum functioning air gap with this typical gear/ magnet combination can be determined using the graphs and the specifications for the sensor IC.

In this case, if an A3056EU/LU sensor with a B_{OP} of +25 G and a B_{RP} of -25 G is used, the maximum allowable air gap would be 0.110" (2.79 mm). If the switch points change +75 G with temperature (B_{OP} = + 100 G, B_{RP} = +50 G), the maximum air gap will be approximately 0.077" (1.96 mm).

All system issues should be translated back to such a profile to aid the prediction of system performance.

Magnet Selection. These devices can be used with a wide variety of commercially available permanent magnets. The selection of the magnet depends on the operational and environmental requirements of the sensing system. For systems that require high accuracy and large working airgaps or an extended temperature range, the usual magnet material of choice is rare earth samarium cobalt (SmCo). This magnet material has a high energy product and can operate over an extended temperature range. For systems that require low-cost solutions for an extended temperature range, Alnico-8 can be used. Due to its relatively low energy product, smaller operational airgaps can be expected. At this time, neodymium iron boron (NeFeB) is not a proven high-temperature performer; at temperatures above +150°C it may irreversibly lose magnetic strength. Of these three magnet materials, Alnico-8 is the least expensive by volume and SmCo is the most expensive.

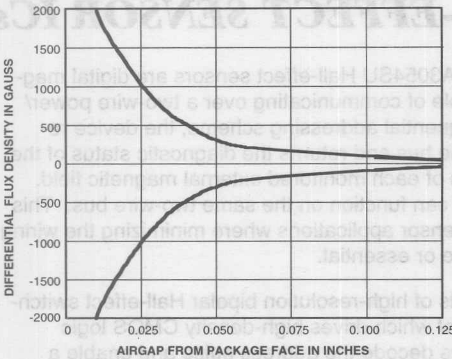
Figure 4
POSITIVE AND NEGATIVE SWITCH OPERATION



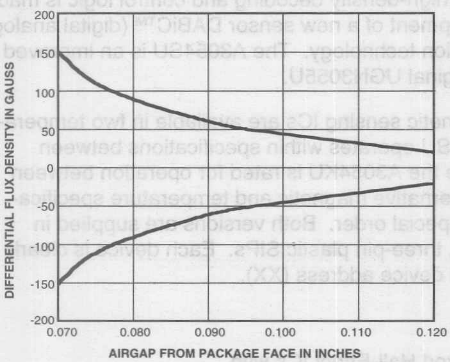
Either cylindrical- or cube-shaped magnets can be used, as long as the magnet pole face at least equals the facing surface(s) of the IC package and the pole piece. Choose the length of the magnet to obtain a high length-to-width ratio, up to 0.75:1 for rare earths, or 1.5:1 for Alnico-8. Any added magnet length may incrementally improve the allowable maximum air gap.

Magnets, in general, have a non-uniform magnetic surface profile. The flux across the face of a magnet can vary by as much as 5% of the average field over a 0.10" (2.5 mm) region. If a Hall sensor is placed directly on a magnet face, the non-uniformity can appear to shift the operating parameters of the sensor. For example, if a device is placed on a 3000 G magnet with ±2% face offsets, each of the operating points might be shifted by ±60 G. When offsets are present, the operating characteristics may be greatly altered.

Figure 5
DIFFERENTIAL FLUX DENSITY

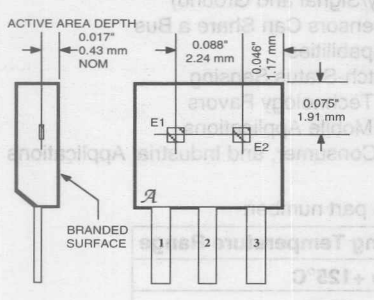


Dwg. GH-035



Dwg. GH-036

SENSOR LOCATION



Dwg. MH-002-8C

Pole Piece Design. A pole piece may be used at the face of the magnet to smooth out the magnet-face offsets. A 0.020" (0.51 mm) thick, soft-iron pole piece will bring the field non-uniformity down to the ±1%-to-±3% range. Note that pole pieces will minimize but not eliminate the non-uniformity in the magnet face field. Front pole pieces will almost always result in a reduced maximum air gap.

Ferrous Targets. The best ferrous targets are made of cold-rolled low-carbon steel. Sintered-metal targets are also usable, but care must be taken to ensure uniform material composition and density.

The teeth or slots of the target should be cut with a slight angle so as to minimize the abruptness of transition from metal to air as the target passes by the sensor. Sharp transitions will result in magnetic overshoots that can result in false triggering.

Gear teeth larger than 0.10" (2.54 mm) wide and at least 0.10" (2.54 mm) deep provide reasonable working air gaps and adequate change in magnetic field for reliable switching. Generally, larger teeth and slots allow a larger air gap. A gear tooth width approximating the spacing between sensors (0.088" or 2.24 mm) requires special care in the system design and assembly techniques.

ASSEMBLY TECHNIQUES

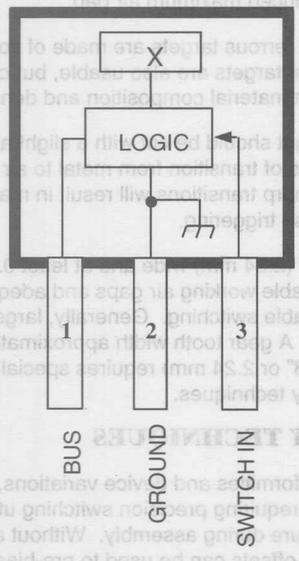
Due to magnet face non-uniformities and device variations, it is recommended that applications requiring precision switching utilize a mechanical optimization procedure during assembly. Without a pole piece, the inherent magnet face offsets can be used to pre-bias the magnetic circuit to obtain any desired operating mode. This is achieved by physically changing the relative position of the magnet behind the sensor to achieve the desired system performance objective. For example, with a rotating ABS gear, the objective might be a 50% duty cycle at maximum air gap. Similar objectives can be set for ignition (crank and cam position) sensing systems.

Non-precision speed sensing applications do not require optimization. For applications where mechanical optimization is not feasible, non-zero speed devices such as the UGN/UGS3059KA ac-coupled gear-tooth sensor are available.

3054

27680.1

MULTIPLEXED TWO-WIRE HALL-EFFECT SENSOR ICs



Dwg. PH-005

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{BUS} . . . . **18 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Operating Temperature Range, T_A
A3054KU . . . . **-40°C to +125°C**
A3054SU . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**
Package Power Dissipation,
P_D . . . . **635 mW**

The A3054KU and A3054SU Hall-effect sensors are digital magnetic sensing ICs capable of communicating over a two-wire power/signal bus. Using a sequential addressing scheme, the device responds to a signal on the bus and returns the diagnostic status of the IC, as well as the status of each monitored external magnetic field. As many as 30 sensors can function on the same two-wire bus. This IC is ideal for multiple sensor applications where minimizing the wiring harness size is desirable or essential.

Each device consists of high-resolution bipolar Hall-effect switching circuitry, the output of which drives high-density CMOS logic stages. The logic stages decode the address pulse and enable a response at the appropriate address. The combination of magnetic-field or switch-status sensing, low-noise amplification of the Hall-transducer output, and high-density decoding and control logic is made possible by the development of a new sensor DABiC™ (digital analog bipolar CMOS) fabrication technology. The A3054SU is an improved replacement for the original UGN3055U.

These unique magnetic sensing ICs are available in two temperature ranges; the A3054SU operates within specifications between -20°C and +85°C, while the A3054KU is rated for operation between -40°C and +125°C. Alternative magnetic and temperature specifications are available on special order. Both versions are supplied in 0.060" (1.54 mm) thick, three-pin plastic SIPs. Each device is clearly marked with a two-digit device address (XX).

FEATURES

- Complete Multiplexed Hall-Effect ICs with Simple Sequential Addressing Protocol
- Allows Power and Communication Over a Two-Wire Bus (Supply/Signal and Ground)
- Up to 30 Hall-Effect Sensors Can Share a Bus
- Sensor Diagnostic Capabilities
- Magnetic-Field or Switch-Status Sensing
- Low Power of DABiC Technology Favors Battery-Powered and Mobile Applications
- Ideal for Automotive, Consumer, and Industrial Applications

Always order by complete part number:

Part Number	Operating Temperature Range
A3054KU-XX	-40°C to +125°C
A3054SU-XX	-20°C to +85°C

where XX = address (01, 02, … 29, 30).

ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits Min	Limits Typ	Limits Max	Units
Power Supply Voltage	V_{BUS}		—	—	15	V
Signal Current	I_S	DUT Addressed, B > 300 G	12	15	20	mA
Quiescent Current	I_{QL}	V_{BUS} = 6 V	—	1.5	2.5	mA
	I_{QH}	V_{BUS} = 9 V	—	1.4	2.5	mA
	ΔI_Q	$I_{QL} - I_{QH}$	—	100	300	µA
Address Range	Addr	Factory Specified	1	—	30	—
Clock Thresholds	V_{CLH}	LOW to HIGH	—	—	8.5	V
	V_{CHL}	HIGH to LOW	6.5	—	—	V
	V_{CHYS}	Hysteresis	—	0.8	—	V
Max. Clock Frequency*	f_{CLK}	50% Duty Cycle	2.5	—	—	kHz
Address LOW Voltage	V_L		V_{RST}	6.0	V_{CHL}	V
Address HIGH Voltage	V_H		V_{CLH}	9.0	V_{BUS}	V
Reset Voltage	V_{RST}		2.5	3.5	5.5	V
Propagation Delay*	t_{plh}	LOW to HIGH	10	20	30	µs
	t_{phl}	HIGH to LOW	—	5.0	10	µs
Pin 3-2 Resistance	R_{SWH}	DUT Addressed, B < 5 G	—	50	—	kΩ
	R_{SWL}	DUT Addressed, B > 300 G	—	200	—	Ω
Pin 3-2 Output Voltage	V_{SWH}	DUT Addressed, B < 5 G	—	3.9	—	V
	V_{SWL}	DUT Addressed, B> 300 G	—	30	—	mV

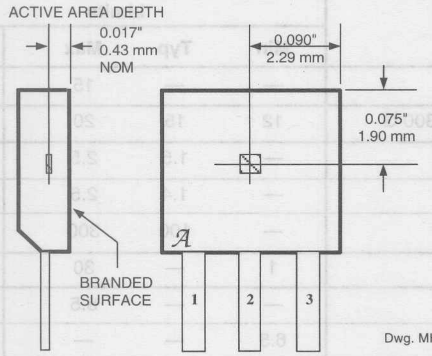
MAGNETIC CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Magnetic Threshold†	B_{OP}	Turn-On	50	150	300	G
	B_{RP}	Turn-Off	5.0	100	295	G
Hysteresis	B_{HYS}	$B_{OP} - B_{RP}$	5.0	50	—	G

Typical Data is at T_A = +25°C and is for design information only.
*This parameter, although guaranteed, is not production tested.
†Alternative magnetic switch point specifications are available on special order. Please contact the factory

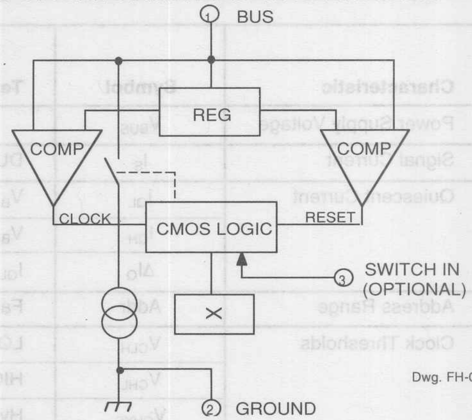
SENSOR LOCATION

(±0.005” [0.13 mm] die placement)



Dwg. MH-002-10

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-009

DEFINITION OF TERMS

Sensor Address

Each bus sensor has a factory-specified predefined address. At present, allowable sensor addresses are integers from 01 to 30.

LOW-to-HIGH Clock Threshold (V_{CLH})

Minimum voltage required during the positive-going transition to increment the bus address and trigger a diagnostic response from the bus sensors. This is also the maximum threshold of the on-chip comparator that monitors the supply voltage, V_{BUS}.

HIGH-to-LOW Threshold (V_{HL})

Maximum voltage required during the negative-going transition to trigger a *signal* current response from the bus sensors. This is also the maximum threshold of the on-chip comparator that monitors the supply voltage, V_{BUS}.

Bus HIGH Voltage (V_H)

Bus HIGH voltage during addressing. Voltage should be greater than V_{CLH}.

Address LOW Voltage (V_L)

Bus LOW voltage during addressing. Voltage should be greater than V_{RST} and less than V_{CHL}.

Bus Reset Voltage (V_{RST})

Voltage level while resetting sensors.

Sensor Quiescent Current Drain (I_Q)

The current drain of bus sensors when active but not addressed. I_{QH} is the quiescent current drain when the sensor is not addressed and is at V_H I_{QL} is the quiescent current drain when the sensor is not addressed and is at V_L. Note that I_{QL} is greater than I_{QH}.

Diagnostic Phase

Period on the bus when the address voltage is at V_H. During this period, a correctly addressed sensor responds by increasing its current drain on the bus. This response from the sensor is called the **diagnostic response** and the bus current *increase* is called the **diagnostic current.**

Signal Phase

Period on the bus when the address voltage is at V_L. During this period, a correctly addressed sensor that detects a magnetic field greater than the magnetic operate point, B_{OP}, responds by maintaining a current drain of I_S on the bus. This response from the sensor is called the **signal response** and the bus current is called the **signal current.**

Sensor Address Response Current (I_S)

Sensor current during the *diagnostic* and the *signal* responses of the bus sensor. This is accomplished by enabling an internal constant-current source.

ADDRESSING PROTOCOL

Magnetic Operate Point (B_{OP})

Minimum magnetic field required to switch ON the Hall amplifier and switching circuitry of the addressed sensor. This circuitry is only active when the sensor is addressed.

Magnetic Release Point (B_{RP})

Magnetic field required to switch OFF the Hall amplifier and switching circuitry after the output has been switched ON. When a device is deactivated by changing the bus address, all magnetic memory is lost.

Magnetic Hysteresis (B_{HYS})

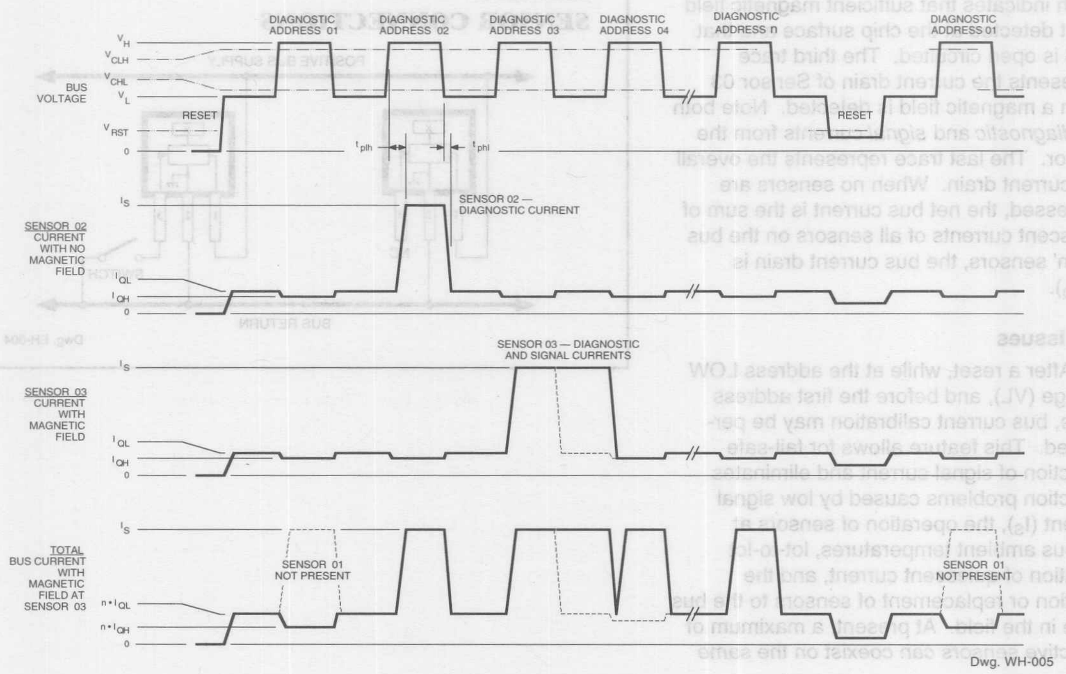
Difference between the B_{OP} and B_{RP} magnetic field thresholds.

A device may be addressed by changing the supply voltage as shown in Figure 1. A preferred addressing protocol is as follows: the bus supply voltage is brought low (<2.5 V) so that all devices on the bus are reset. The voltage is then raised to the address LOW voltage (V_L) and the bus quiescent current is measured. The bus is then toggled between V_L and V_H (address HIGH voltage), with each positive transition representing an increment in the bus address. After each voltage transition, the bus current may be monitored to check for diagnostic and signal responses from sensor ICs.

Sensor Addressing

When a sensor detects a bus address equal to its factory-programmed address, it responds with an increase in its supply current drain (I_S) during the next HIGH portion

FIGURE 1
BUS TIMING



Dwg. WH-005

ofthe address cycle. This response may be used as an indication that the sensor is "alive and well" on the bus and is called the *diagnostic* response. If the sensor detects an ambient magnetic field, it continues with I_S during the low portion of the address cycle. This response from the sensor is called the *signal* response. When the next positive (address) transition is detected, the sensor becomes disabled, and its contribution to the bus signal current returns to I_Q.

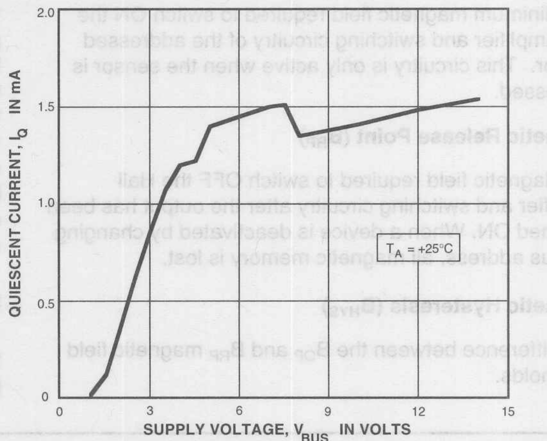
Bus Current

Figure 1 shows the addressing protocol. The top trace represents the bus voltage transitions as controlled by the bus driver (see Applications Notes for an optimal bus driver schematic). The second trace represents the bus current contribution of Sensor 02. The *diagnostic* response from the sensor indicates that it detected its address on the bus. However, no *signal* current is shown, which indicates that sufficient magnetic field is not detected at the chip surface and that pin 3 is open circuited. The third trace represents the current drain of Sensor 03 when a magnetic field is detected. Note both the *diagnostic* and *signal* currents from the sensor. The last trace represents the overall bus current drain. When no sensors are addressed, the net bus current is the sum of quiescent currents of all sensors on the bus (for 'n' sensors, the bus current drain is $n \bullet I_Q$).

Bus Issues

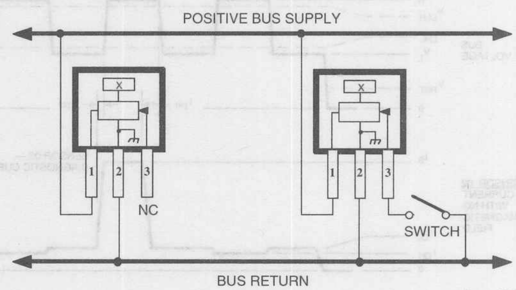
After a reset, while at the address LOW voltage (VL), and before the first address pulse, bus current calibration may be performed. This feature allows for fail-safe detection of signal current and eliminates detection problems caused by low signal current (I_S), the operation of sensors at various ambient temperatures, lot-to-lot variation of quiescent current, and the addition or replacement of sensors to the bus while in the field. At present, a maximum of 30 active sensors can coexist on the same

TYPICAL DEVICE QUIESCENT CURRENT



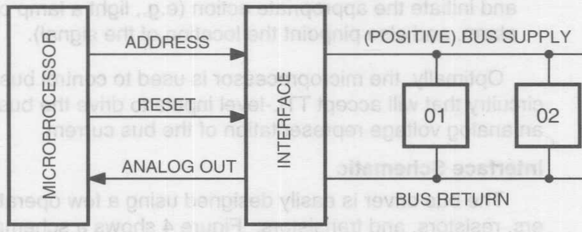
Dwg. GH-045

FIGURE 2
SENSOR CONNECTIONS



Dwg. EH-004

FIGURE 3
BUS INTERCONNECTION



bus, each with a different address. Address 31 is designed to be inactive to allow for further address expansion of the bus (to 62 maximum addresses). In order to repeat the address cycle, the bus must be reset, as shown in Figure 1, by bringing the supply voltage to below V_{RST}. Sensors have been designed not to 'wrap-around'.

Magnetic Sensing

The sensor IC has been designed to respond to an external magnetic field whose magnetic strength is greater than B_{OP}. It accomplishes this by amplifying the output of an on-chip Hall transducer and applying it to a threshold detector. In order that bus current is kept to a minimum, the transducer and amplification circuitry is kept powered down until the sensor is addressed. Hence, the magnetic status is evaluated only when the sensor is addressed.

External Switch Sensing

Pin 3 of the IC may be used to detect the status of an external switch when magnetic field sensing is not desired (and in the absence of a magnetic field). The allowable states for the switch are 'open' or 'closed' (shorted to sensor ground).

APPLICATIONS NOTES

Magnetic Actuation

The left side of Figure 2 shows the wiring of an A3054KU or A3054SU when used as a magnetic threshold detector. Pin 1 of the sensor is wired to the positive terminal of the bus, pin 2 is connected to the bus negative terminal, and *pin 3 has no connection.*

Mechanical Actuation

The right side of Figure 2 shows the wiring of an A3054KU or A3054SU when used to detect the status of a mechanical switch. In this case, pin 3 is connected to the switch. The other side of the switch is connected to the bus return (negative bus supply or ground). When the mechanical switch is closed, and the correct bus address is detected by the IC, the sensor responds with a signal current. If the switch is open, only the diagnostic current is returned.

Bus Configuration

A maximum of 30 individually addresable sensors may be connected across the same two-wire bus as shown in Figure 3. It is recommended that the sensors use a dedicated digital ground wire to minimize the effects of changing ground potential (as in the case of chassis ground in the automotive industry).

The bus was not designed to require two-wire twisted pair wiring to the sensors. However, in areas of extreme electromagnetic interference, it may be advisable to install a small bypass capacitor (0.01 µF for example) between the supply and ground terminals of each sensor instead of using the more expensive wiring.

Bus Driver

It is recommended that the bus be controlled by microprocessor-based hardware for the following reasons:

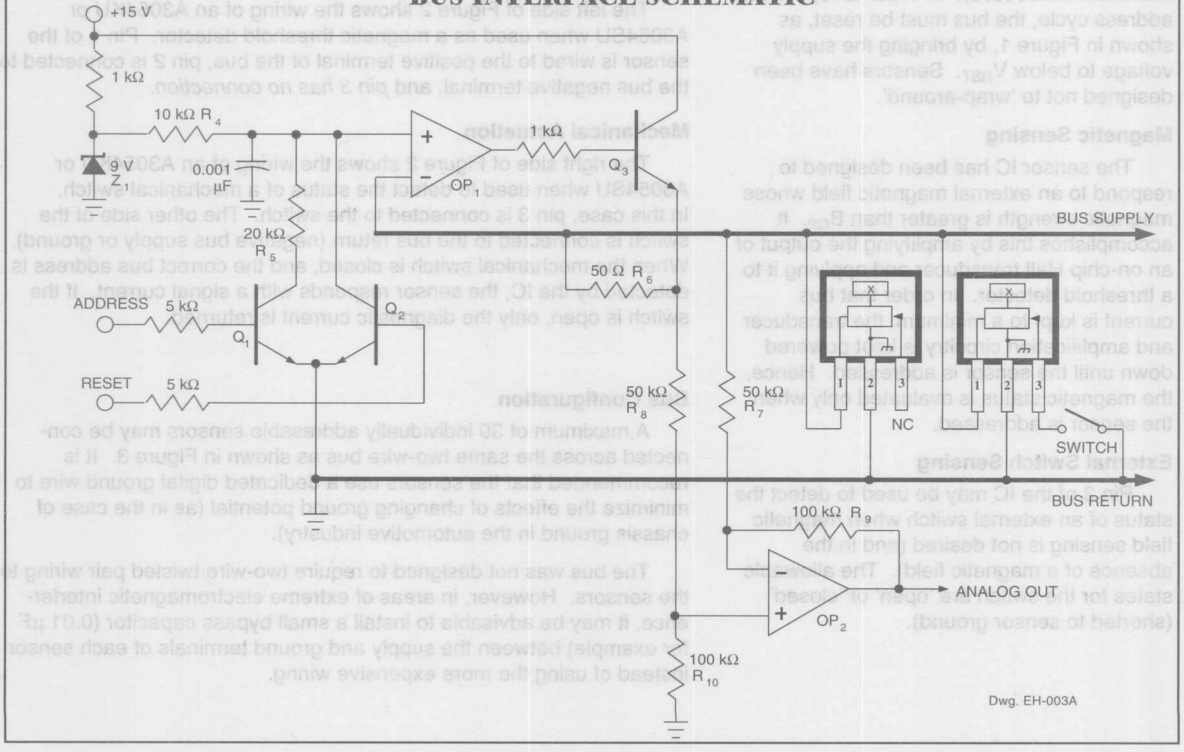
- Sensor address information may be stored in ROM in the form of a look-up table.
- Bus faults can be pinpointed by the microprocessor by comparing the diagnostic response to the expected response in the ROM look-up table.
- The microprocessor, along with an A/D converter, can also be used to self calibrate the quiescent currents in the bus and hence be able to easily detect a signal response.
- The microprocessor can also be used to filter out random line noise by digitally filtering the bus responses.
- The microprocessor can easily keep track of the signal responses and initiate the appropriate action (e.g., light a lamp or sound an alarm, and also pinpoint the location of the signal).

Optimally, the microprocessor is used to control bus-driving circuitry that will accept TTL-level inputs to drive the bus and will return an analog voltage representation of the bus current.

Interface Schematic

The bus driver is easily designed using a few operational amplifiers, resistors, and transistors. Figure 4 shows a schematic of a recommended bus driver circuit that is capable of providing 6 V to 9 V transitions, resetting the bus, and providing an analog measurement of the bus current for the A/D input of the microprocessor.

FIGURE 4
BUS INTERFACE SCHEMATIC



In Figure 4, the ADDRESS input provides a TTL-compatible input to control the bus supply. A HIGH (5 V) input switches Q_1 ON and sets the bus voltage to 6 V through the resistor divider R_4, R_5, and Zener Z_1. A LOW input switches Q_1 OFF and sets the bus voltage to 9 V (Z_1). This voltage is fed into the positive input of the operational amplifier OP_1 and is buffered and made available at BUS SUPPLY (or sensor supply). Bus reset control is also available in the form of a TTL-compatible input. When the RESET input is HIGH, Q_2 is switched ON and the positive input of the operational amplifier is set to the saturation voltage of the transistor (approximately 0 V). This resets the bus.

A linear reading of the bus current is made possible by amplifying the voltage generated across R_6 (which is $I_{BUS} \bullet R_6$). The amplifier, OP_2, is a standard differential amplifier of gain R_9/R_7 (provided that $R_7 = R_8$, $R_9 = R_{10}$). The gain of the total transim-pedance amplifier is given by:

$$V_{OUT} = I_{BUS} \bullet R_6 \bullet R_9/R_7$$

This voltage is available at the ANALOG OUT terminal.

Bus Control Software

The processing of the bus current (available at ANALOG OUT) is best done by feeding it into the A/D input of a microprocessor. If the flexibility provided by a microprocessor is not desired, this signal could be fed into threshold detection circuitry; e.g., comparator, and the output used to drive a display.

Related References

1. G. AVERY, "Two-Terminal HallSensor," *ASSIGNEE: Sprague Electric Company, North Adams, MA, United States. Patent number 4,374,333; Feb. 1983.*

2. T. WROBLEWSKI and F. MEISTERFIELD, "Switch Status Monitoring System, Single-Wire Bus, Smart Sensor Arrangement There Of," *ASSIGNEE: Chrysler Motor Corporation, Highland Park, MI, United States. Patent number 4,677,308; June 1987.*

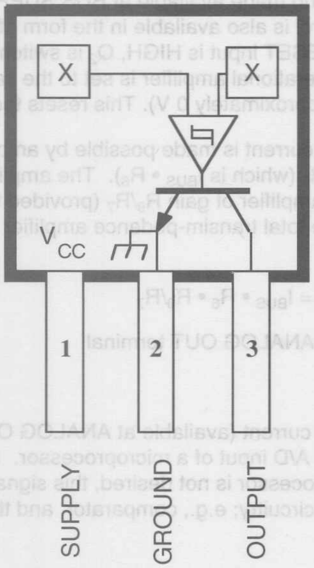
3056 AND 3058

HALL-EFFECT GEAR-TOOTH SENSORS–ZERO SPEED

The A3056EU/LU and A3058EU/LU Hall effect gear-tooth sensors are monolithic integrated circuits that switch in response to differential magnetic fields created by ferrous targets. These devices are ideal for use in gear-tooth-based speed, position, and timing applications and operate down to zero rpm over a wide range of air gaps and temperatures. When combined with a back-biasing magnet and proper assembly techniques, devices can be configured to give 50% duty cycle or to switch on either leading, trailing, or both edges of a passing gear tooth or slot.

The six devices differ only in their magnetic switching values and operating temperature ranges. The low hysteresis of the A3056EU and A3056LU makes them perfectly suited for ABS (anti-lock brake system) or speed sensing applications where maintaining large air gaps is important. The high hysteresis of the A3058EU and A3058LU, with their excellent temperature stability, makes them especially suited to ignition timing applications where switch-point accuracy (and latching requirements) is extremely important.

Complete technical information on these devices is included with the A3046EU/LU.



Dwg. No. PH-012

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS

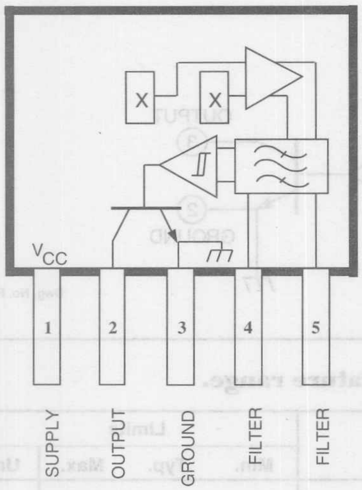
Supply Voltage, V_{CC} . . . . **28 V**
Reverse Battery Voltage,
V_{RCC} . . . . **-30 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . **28 V**
Reverse Output Voltage, V_{OUT} . . . . . **-0.5 V**
Output Current, I_{OUT} . . . . **25 mA**
Package Power Dissipation, P_D . . **500 mW**
Operating Temperature Range, T_A
Suffix "EU" . . . . **-40°C to +85°C**
Suffix "LU" . . . . **-40°C to +150°C**
Storage Temperature Range,
T_S . . . . **-65°C to +170°C**

BENEFITS

- Senses Ferrous Targets Down to Zero RPM
- Defined Power-Up State (3058 only)
- Large Effective Air Gap
- Wide Operating Temperature Range
- Operation from Unregulated Supply
- High-Speed Operation
- Output Compatible With All Logic Families
- Reverse Battery Protection
- Solid-State Reliability
- Resistant to Physical Stress

3059 AND 3060

HALL-EFFECT GEAR-TOOTH SENSORS —AC COUPLED



Dwg. No. PH-011

Pinning is shown viewed from branded side.

The UGN/UGS3059KA and UGN/UGS3060KA ac-coupled Hall-effect gear-tooth sensors are monolithic integrated circuits that switch in response to changing differential magnetic fields created by moving ferrous targets. These devices are ideal for use in non-zero-speed, gear-tooth-based speed, position, and timing applications such as in anti-lock braking systems, transmissions, and crankshafts.

Both devices, when coupled with a back-biasing magnet, can be configured to turn ON or OFF with the leading or trailing edge of a gear-tooth or slot. Changes in fields on the magnet face caused by a moving ferrous mass are sensed by two integrated Hall transducers and are differentially amplified by on-chip electronics. This differential sensing design provides immunity to radial vibration within the devices' operating air gaps. Steady-state magnet and system offsets are eliminated using an on-chip differential band-pass filter. This filter also provides relative immunity to interference from RF and electromagnetic sources. The on-chip temperature compensation and Schmitt trigger circuitry minimizes shifts in effective working air gaps and switch points over temperature, allowing operation to low frequencies over a wide range of air gaps and temperatures.

Each Hall-effect digital Integrated circuit includes a voltage regulator, two quadratic Hall-effect sensing elements, temperature compensating circuitry, a low-level amplifier, band-pass filter, Schmitt trigger, and an open-collector output driver. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The output stage can easily switch 20 mA over the full frequency response range of the sensor and is compatible with bipolar and MOS logic circuits.

The two devices provide a choice of operating temperature ranges. Both devices are packaged in a 5-pin plastic SIP.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

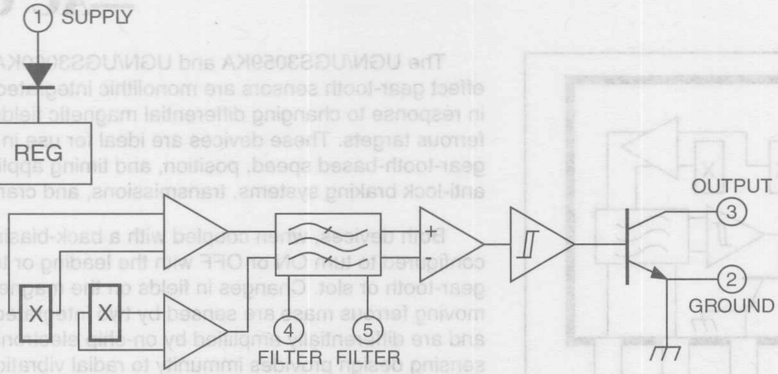
Supply Voltage, V_{CC} .... 24 V
Reverse Battery Voltage, V_{RCC} .... -30 V
Magnetic Flux Density, B .... Unlimited
Output OFF Voltage, V_{OUT} .... 24 V
Output Current, I_{OUT} .... 25 mA
Package Power Dissipation,
P_D .... 500 mW
Operating Temperature Range, T_A
Prefix 'UGN' .... -20°C to +85°C
Prefix 'UGS' .... -40°C to +125°C
Storage Temperature Range,
T_S .... -65°C to +150°C

FEATURES

- Senses Motion of Ferrous Targets Such as Gears
- Wide Operating Temperature Range
- Operation to 30 kHz
- Resistant to RFI, EMI
- Large Effective Air Gap
- 4.5 V to 24 V Operation
- Output Compatible With All Logic Families
- Reverse Battery Protection
- Resistant to Physical Stress

Always order by complete part number, e.g., UGS3060KA.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FH-008

ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	130	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	—	10	µA
Supply Current	I_{CC}	V_{CC} = 18 V, B < B_{RP}	—	11	20	mA
High-Frequency Cutoff	f_{coh}	-3 dB	30	—	—	kHz
Output Rise time	t_r	V_{OUT} = 12 V, R_L = 820 Ω	—	0.04	0.2	µs
Output Fall time	t_f	V_{OUT} = 12 V, R_L = 820 Ω	—	0.18	0.3	µs

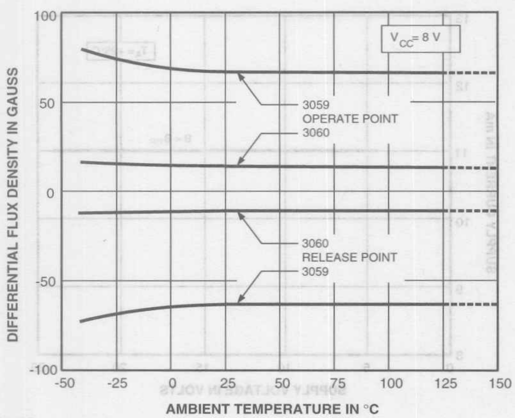
MAGNETIC CHARACTERISTICS over operating temperature and supply voltage ranges

Characteristic	Test Conditions	Part Numbers* 3059 Min.	3059 Typ.	3059 Max.	3060 Min.	3060 Typ.	3060 Max.
Operate Point, B_{OP}	Output switches OFF to ON	10	65	100	5.0	15	35
Release Point, B_{RP}	Output switches ON to OFF	-100	-65	-10	-35	-15	-5.0
Hysteresis, B_{hys}	B_{OP} - B_{RP}	—	130	—	—	30	—

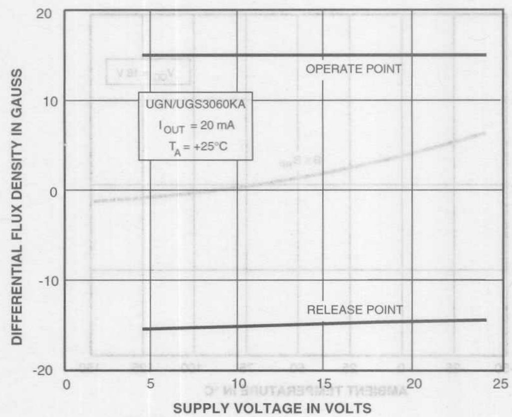
NOTES: * Complete part number includes a prefix to identify operating temperature range (UGN or UGS) and the package suffix KA.
Magnetic switch points are specified as the difference in magnetic fields at the two Hall elements.
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = 25°C and V_{CC} = 12 V.

TYPICAL OPERATING CHARACTERISTICS

SWITCH POINTS

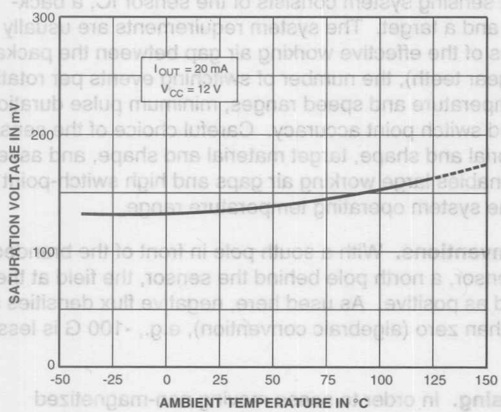


GH-056

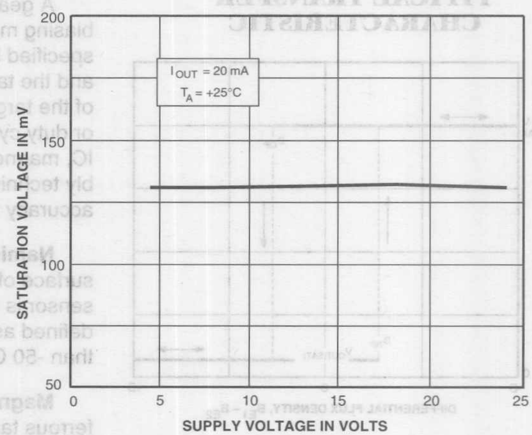


GH-057

OUTPUT SATURATION VOLTAGE



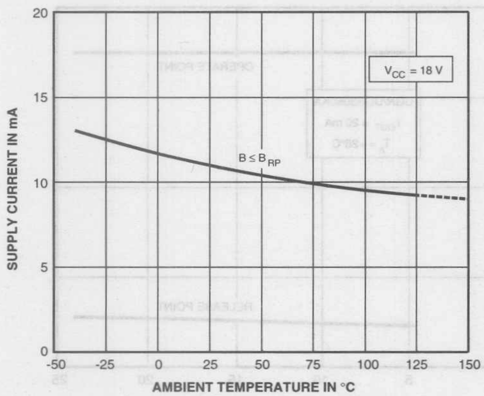
GH-029-1



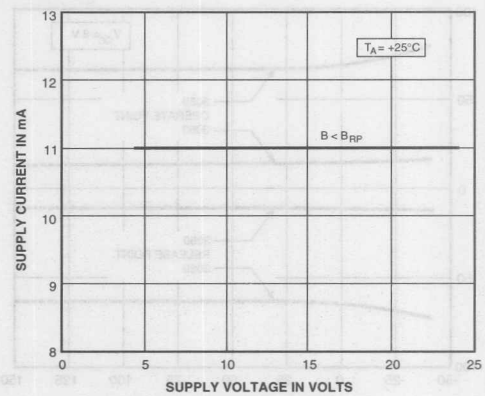
GH-055

TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT



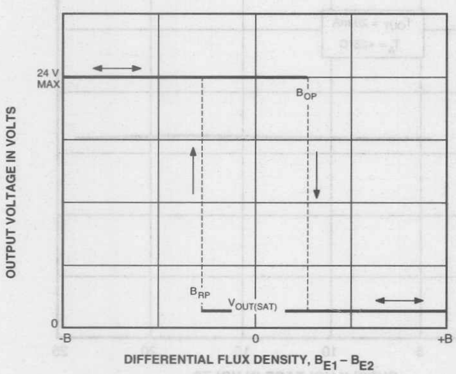
GH-028-1



GH-031-1

FIGURE 1

TYPICAL TRANSFER CHARACTERISTIC



Dwg. GH-034

APPLICATIONS INFORMATION

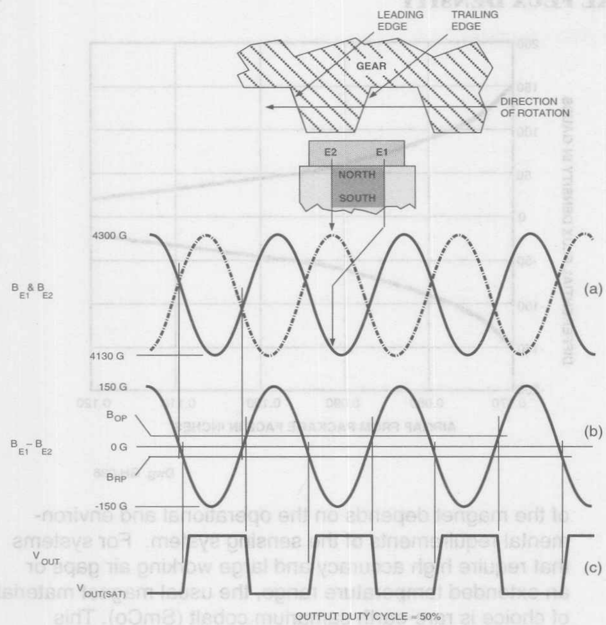
A gear-tooth sensing system consists of the sensor IC, a back-biasing magnet, and a target. The system requirements are usually specified in terms of the effective working air gap between the package and the target (gear teeth), the number of switching events per rotation of the target, temperature and speed ranges, minimum pulse duration or duty cycle, and switch point accuracy. Careful choice of the sensor IC, magnet material and shape, target material and shape, and assembly techniques enables large working air gaps and high switch-point accuracy over the system operating temperature range.

Naming Conventions. With a south pole in front of the branded surface of the sensor, a north pole behind the sensor, the field at the sensor is defined as positive. As used here, negative flux densities are defined as less than zero (algebraic convention), e.g., -100 G is less than -50 G.

Magnet Biasing. In order to sense moving non-magnetized ferrous targets, these devices must be back-biased by mounting the unbranded side on a small permanent magnet. Either magnetic pole (north or south) can be used.

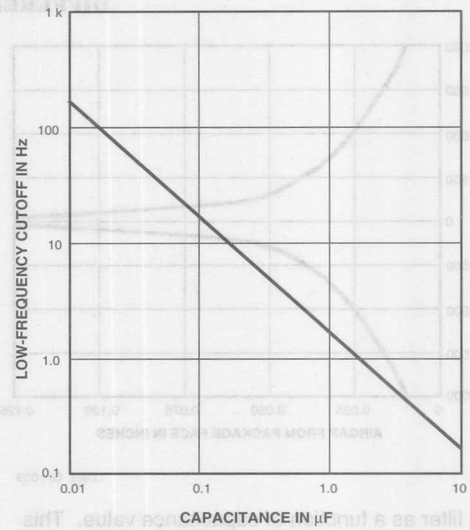
The devices can also be used without a back-biasing magnet. In this configuration, the sensor can be used to detect a rotating ring magnet such as those found in brushless dc motors or in speed sensing applications. Here, the sensor detects the magnetic field gradient created by the magnetic poles.

Figure 2



Dwg. WH-003-1

Figure 3



Dwg. GH-025

Sensor Operation. These sensor ICs each contain two integrated Hall transducers (E1 and E2) that are used to sense a magnetic field differential across the face of the IC (see Sensor Location drawing). Referring to Figure 1, the trigger switches the output ON (output LOW) when B_{E1} - B_{E2} < B_{OP} and switches the output OFF (output HIGH) when B_{E1} - B_{E2} < B_{RP}. The difference between B_{OP} and B_{RP} is the hysteresis of the device.

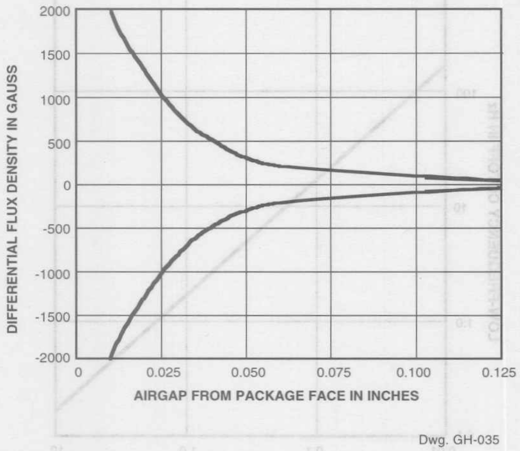
Figure 2 relates the output state of a back-biased sensor IC, with switching characteristics shown in Figure 1, to the target gear profile and position. Assume a north pole back-bias configuration (equivalent to a south pole at the face of the device). The motion of the gear produces a phase-shifted field at E1 and E2 (Figure 2(a)); internal conditioning circuitry subtracts the fields at the two elements (Figure 2(b)); this differential field is band-pass filtered to remove dc offset components and then fed into a Schmitt trigger; the Schmitt trigger switches the output transistor at the thresholds B_{OP} and B_{RP}. As shown (Figure 2(c)), the IC output is LOW whenever sensor E1 sees a (ferrous) gear tooth and sensor E2 faxes air. The output is HIGH when sensor E1 sees air and sensor E2 sees the ferrous target.

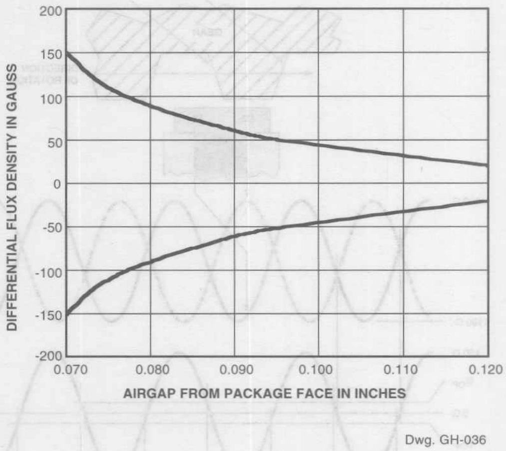
AC-Coupled Operation. Steady-state magnet and system offsets are eliminated using an on-chip differential band-pass filter. The lower frequency cut-off of this patented filter is set using an external capacitor the value of which can range from 0.01 µF to 10 µF. The high-frequency cut-off of this filter is set at 30 kHz by an internal integrated capacitor.

The differential structure of this filter enables the IC to reject single-ended noise on the ground or supply line and, hence, makes it resistant to radio-frequency and electromagnetic interference typically seen in hostile remote sensing environments. This filter configuration also increases system tolerance to capacitor degradation at high temperatures, allowing the use of an inexpensive external ceramic capacitor.

Low-Frequency Operation. Low-frequency operation of the sensor is set by the value of an external capacitor. Figure 3 provides the low-frequency cut-off (-3 dB point) of

Figure 4
DIFFERENTIAL FLUX DENSITY





the filter as a function of capacitance value. This information should be used with care. The graph assumes a perfect sinusoidal magnetic signal input. In reality, when used with gear teeth, the teeth create transitions in the magnetic field that have a much higher frequency content than the basic rotational speed of the target. This allows the device to sense speeds much lower than those indicated by the graph for a given capacitor value.

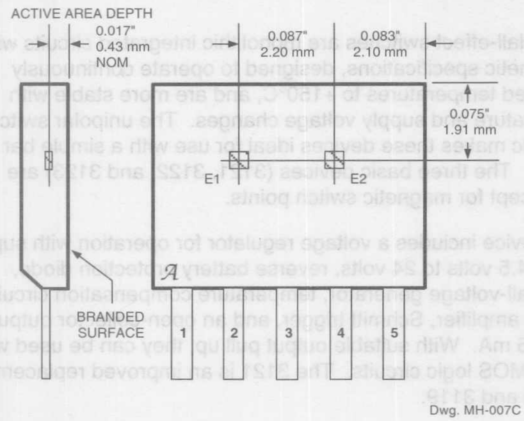
Capacitor Characteristics. The major requirement for the external capacitor is its ability to operate in a bipolar (non-polarized) mode. Another important requirement is the low leakage current of the capacitor (equivalent parallel resistance should be greater than 500kΩ). To maintain proper operation with frequency, capacitor values should be held to within ±30% over the operating temperature range. Available non polarized capacitors include ceramic, polyester, and some tantalum types. For low-cost operation, ceramic capacitors with temperature codes Z5S, Y5S, X5S, or X7S (depending on operating temperature range) or better are recommended. The commonly available Z5U temperature code should not be used in this application.

Magnet Selection. The UGx3059KA or UGx3060KA can be used with a wide variety of commercially available permanent magnets. The selection of the magnet depends on the operational and environmental requirements of the sensing system. For systems that require high accuracy and large working air gaps or an extended temperature range, the usual magnet material of choice is rare-earth samarium cobalt (SmCo). This magnet material has a high energy product and can operate over an extended temperature range. For systems that require low-cost solutions for an extended temperature range, AlNiCo 8 can be used. Due to its relatively low energy product, smaller operational air gaps can be expected. Neodymium iron boron (NeFeB) can be used over moderate temperature ranges when large working air gaps are required. Of these three magnet materials, AlNiCo 8 is the least expensive by volume and SmCo is the most expensive.

System Issues. Optimal performance of a gear-tooth sensing system strongly depends on four factors: the IC magnetic parameters, the magnet, the pole piece configuration, and the target.

Sensor Specifications. Shown in Figure 4 are graphs of the differential field as a function of air gap. A 48-tooth, 2.5" (63.5 mm) diameter, uniform target similar to that used in ABS applications is used. The samarium cobalt magnet is 0.32" diameter by 0.20" long (8.13 x 5.08 mm). The maximum functioning air gap with this typical gear/magnet combination can be determined using the graphs and specifications for the sensor IC.

Figure 5
SENSOR LOCATIONS
(±0.005" [0.13 mm] die placement)



In this case, if a UGx3060KA sensor with a B_{OP} of 15 G and a B_{RP} of -15 G is used, the maximum allowable air gap would be approximately 0.120". If the worst case switch points of B_{OP}= 30 G and B_{RP}-30 for the A3060 were used, the maximum air gap would be approximately 0.105".

All system issues should be translated back to such a profile to aid the prediction of system performance.

Ferrous Targets. The best ferrous targets are made of cold-rolled low-carbon steel. Sintered-metal targets are also usable, but care must be taken to ensure uniform material composition and density.

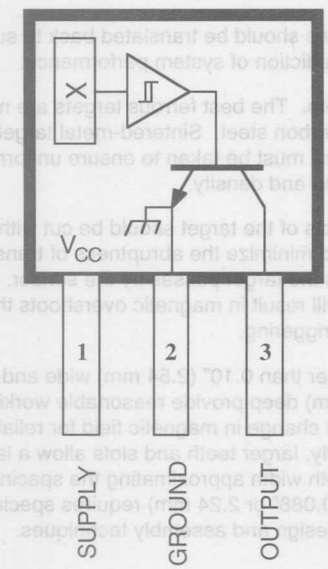
The teeth or slots of the target should be cut with a slight angle so as to minimize the abruptness of transition from metal to air as the target passes by the sensor. Sharp transitions will result in magnetic overshoots that can result in false triggering.

Gear teeth larger than 0.10" (2.54 mm) wide and at least 0.10" (2.54 mm) deep provide reasonable working air gaps and adequate change in magnetic field for reliable switching. Generally, larger teeth and slots allow a larger air gap. A gear tooth width approximating the spacing between sensors (0.088" or 2.24 mm) requires special care in the sytem design and assembly techniques.

3121, 3122, AND 3123

27621.4*

HALL-EFFECT SWITCHES FOR HIGH-TEMPERATURE OPERATION



Dwg. No. PH-003A

Pinning is shown viewed from branded side.

These Hall-effect switches are monolithic integrated circuits with tighter magnetic specifications, designed to operate continuously over extended temperatures to +150°C, and are more stable with both temperature and supply voltage changes. The unipolar switching characteristic makes these devices ideal for use with a simple bar or rod magnet. The three basic devices (3121, 3122, and 3123) are identical except for magnetic switch points.

Each device includes a voltage regulator for operation with supply voltages of 4.5 volts to 24 volts, reverse battery protection diode, quadratic Hall-voltage generator, temperature compensation circuitry, small-signal amplifier, Schmitt trigger, and an open-collector output to sink up to 25 mA. With suitable output pull up, they can be used with bipolar or CMOS logic circuits. The 3121 is an improved replacement for the 3113 and 3119.

The first character of the part number suffix determines the device operating temperature range; suffix 'E–' is for the automotive and industrial temperature range of -40°C to +85°C, suffix 'L–' is for the automotive and military temperature range of -40°C to +150°C. Four package styles provide a magnetically optimized package for most applications. Suffix '-LL' is a long-leaded version of suffix '–LT', a miniature SOT-89/TO-243AA transistor package for surface-mount applications; suffix '–U' is a three-lead plastic mini-SIP while suffix '–UA' is a three-lead ultra-mini-SIP.

ABSOLUTE MAXIMUM RATINGS at T_A=+25°C

Supply Voltage, V_{CC} .... **30 V**
Reverse Battery Voltage, V_{RCC} .... **-30 V**
Magnetic Flux Density, B .... **Unlimited**
Output OFF Voltage, V_{OUT} .... **28 V**
Reverse Output Voltage, V_{OUT} .... **-0.5 V**
Continuous Output Current, I_{OUT} ..... **25 mA**
Operating Temperature Range, T_A
 Suffix 'E–' .... **-40°C to +85°C**
 Suffix 'L–' .... **-40°C to +150°C**
Storage Temperature Range,
 T_S .... **-65°C to +170°C**

FEATURES and BENEFITS

- Superior Temp. Stability for Automotive or Industrial Applications
- 4.5 V to 24 V Operation … Needs Only An Unregulated Supply
- Open-Collector 25 mA Output … Compatible with Digital Logic
- Reverse Battery Protection
- Activate with Small, Commercially Available Permanent Magnets
- Solid-State Reliability
- Small Size
- Resistant to Physical Stress

Always order by complete part number, e.g., $\boxed{\text{A3121ELL}}$.

ELECTRICAL CHARACTERISTICS over operating temperature range, at V_{CC} = 12 V.

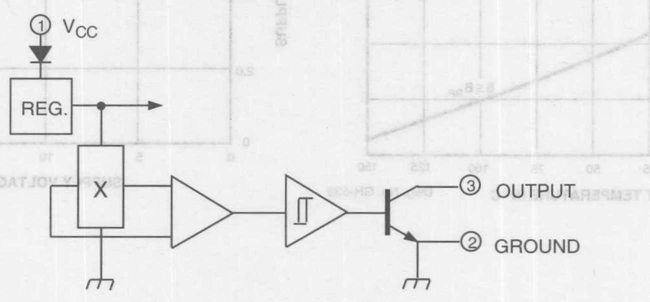
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	140	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	<1.0	10	µA
Supply Current	I_{CC}	B < B_{RP} (Output OFF)	—	4.6	9.0	mA
Output Rise Time	t_r	R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

MAGNETIC CHARACTERISTICS in gauss over operating supply voltage range.

Characteristic	Part Numbers*								
	A3121			A3122			A3123		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max
B_{OP} at T_A = 25°C	250	350	450	280	340	400	250	345	440
over operating temp. range	220	350	500	260	340	430	230	345	470
B_{RP} at T_A = 25°C	125	245	380	140	235	330	180	240	300
over operating temp. range	80	245	410	120	235	360	160	240	330
B_{hys} at T_A = 25°C	70	105	140	70	105	140	70	105	140
over operating temp. range	60	105	150	70	105	140	70	105	140

NOTES: Typical values are at T_A = +25°C and V_{CC} = 12 V.
B_{OP} = operate point (output turns ON); B_{RP} = release point (output turns OFF); B_{hys} = hysteresis (B_{OP} - B_{RP}).
*Complete part number includes a suffix to identify operating temperature range (E- or L-) and package type (-LL, -LT, -U, or -UA).

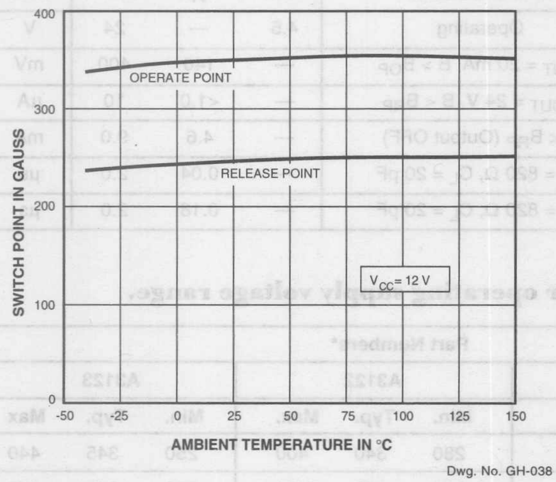
FUNCTIONAL BLOCK DIAGRAM



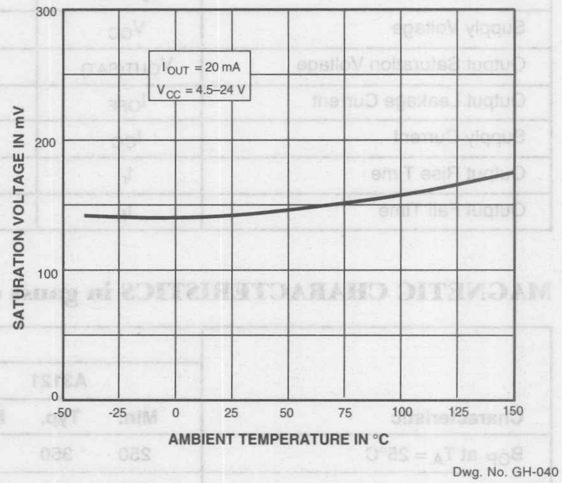
Dwg. No. FH-005-2

TYPICAL OPERATING CHARACTERISTICS

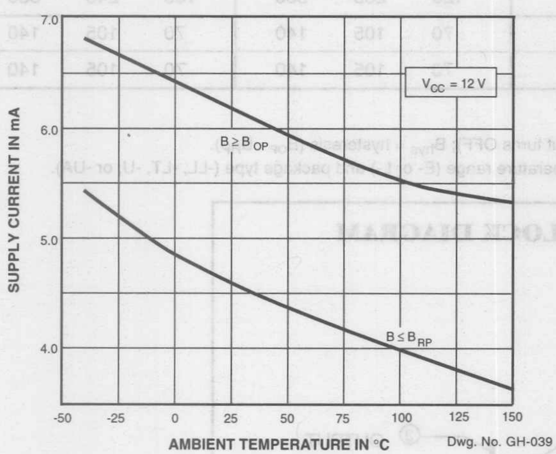
SWITCH POINTS



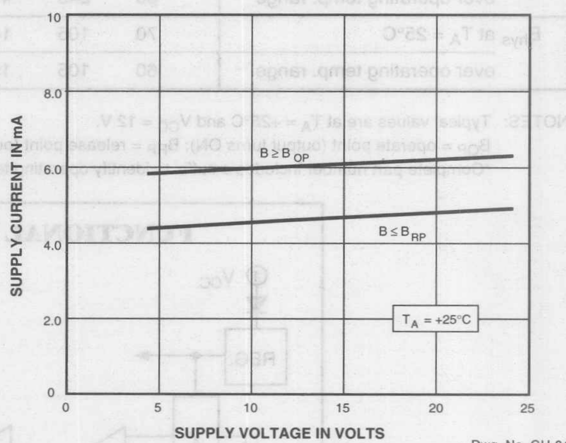
OUTPUT SATURATION VOLTAGE



SUPPLY CURRENT



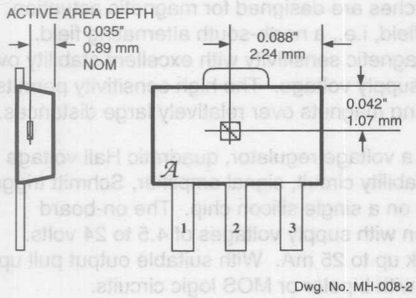
SUPPLY CURRENT



* Complete part number includes a suffix denoting operating temperature range (E- or L-) and package type (-LL, -LT, -U, or -UA).

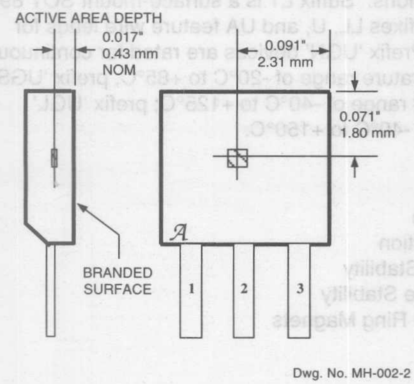
SENSOR LOCATIONS

Suffix "LL" and "LT"



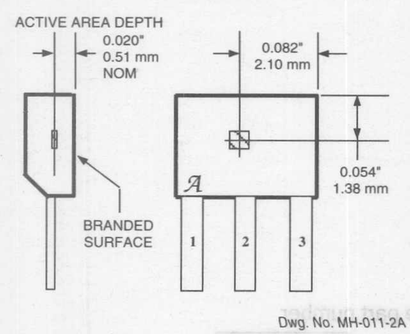
Dwg. No. MH-008-2

Suffix "U"



Dwg. No. MH-002-2

Suffix "UA"



Dwg. No. MH-011-2A

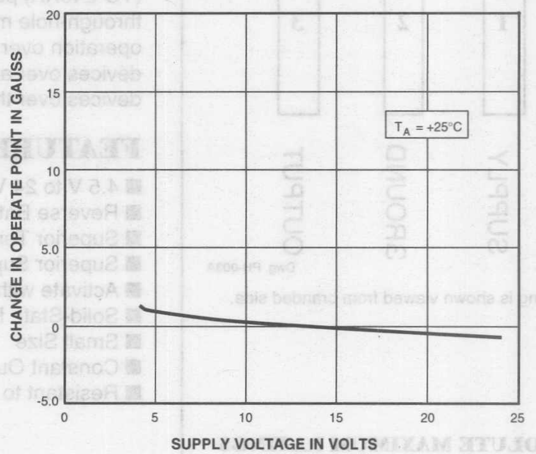
OPERATION

The output of these devices (pin 3) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{OP}). At this point, the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced to below the release point threshold (B_{RP}), the device output goes high. The difference in the magnetic operate and release points is called the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

APPLICATIONS INFORMATION

Hall effect applications information is available in the "Hall-Effect IC Applications Guide".

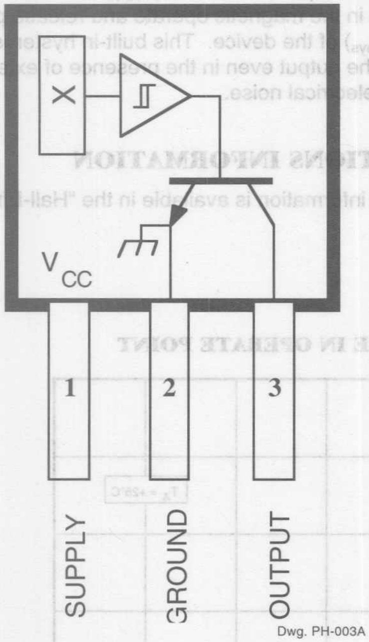
CHANGE IN OPERATE POINT



Dwg. No. GH-042

3132 AND 3133

ULTRA-SENSITIVE BIPOLAR HALL-EFFECT SWITCHES



Pinning is shown viewed from branded side.

These Hall-effect switches are designed for magnetic actuation using a bipolar magnetic field, i.e., a north-south alternating field. They combine extreme magnetic sensitivity with excellent stability over varying temperature and supply voltage. The high sensitivity permits their use with multi-pole ring magnets over relatively large distances.

Each device includes a voltage regulator, quadratic Hall voltage generator, temperature stability circuit, signal amplifier, Schmitt trigger, and open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 24 volts. The switch output can sink up to 25 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The four package styles available provide a magnetically optimized package for most applications. Suffix LT is a surface-mount SOT 89 (TO-243AA) package; suffixes LL, U, and UA feature wire leads for through-hole mounting. Prefix 'UGN' devices are rated for continuous operation over the temperature range of -20°C to +85°C; prefix 'UGS' devices over an extended range of -40°C to +125°C; prefix 'UGL' devices over the range of -40°C to +150°C.

FEATURES

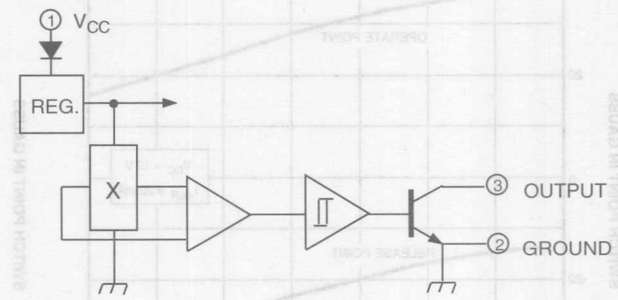
- 4.5 V to 24 V Operation
- Reverse Battery Protection
- Superior Temperature Stability
- Superior Supply Voltage Stability
- Activate with Multi-Pole Ring Magnets
- Solid-State Reliability
- Small Size
- Constant Output Amplitude
- Resistant to Physical Stress

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	**25 V**
Reverse Battery Voltage, V_{RCC}	**-35 V**
Magnetic Flux Density, B	**Unlimited**
Output OFF Voltage, V_{OUT}	**25 V**
Continuous Output Current, I_{OUT}	**25 mA**
Operating Temperature Range, T_A	
Prefix UGL	**-40°C to +150°C**
Prefix UGN	**-20°C to +85°C**
Prefix UGS	**-40°C to +125°C**
Storage Temperature Range, T_S	**-65°C to +150°C**

Always order by complete part number including prefix and suffix, e.g., **UGN3132LL**.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FH-005-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B ≥ B_{OP}	—	145	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B ≤ B_{RP}	—	<1.0	10	µA
Supply Current	I_{CC}	V_{CC} = 24 V, B ≤ B_{RP}	—	4.3	9.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

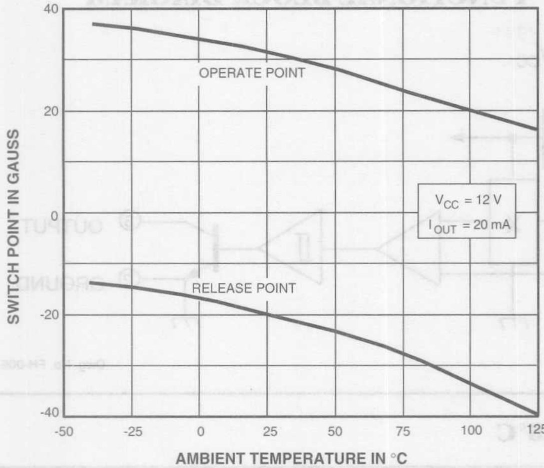
MAGNETIC CHARACTERISTICS over operating temperature and voltage range.

Characteristic	Symbol	Device Type*	Limits			Units
			Min.	Typ.	Max.	
Operate Point	B_{OP}	3132	—	32	95	G
		3133	—	32	75	G
Release Point	B_{RP}	3132	-95	-20	—	G
		3133	-75	-20	—	G
Hysteresis	B_{hys}	Both	30	52	—	G

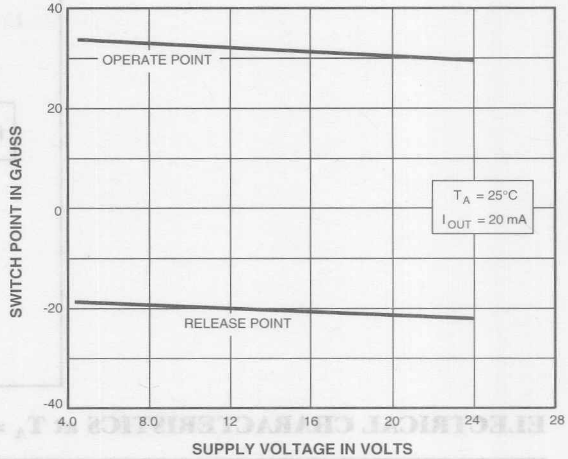
NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention.)
Typical values are at T_A = +25°C and V_{CC} = 12 V.

* Complete part number includes a prefix denoting operating temperature range (UGL, UGN, or UGS) and a suffix denoting package type (LL, LT, U, or UA).

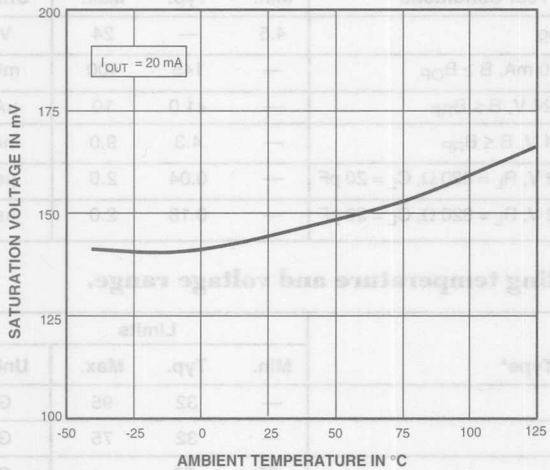
TYPICAL CHARACTERISTICS



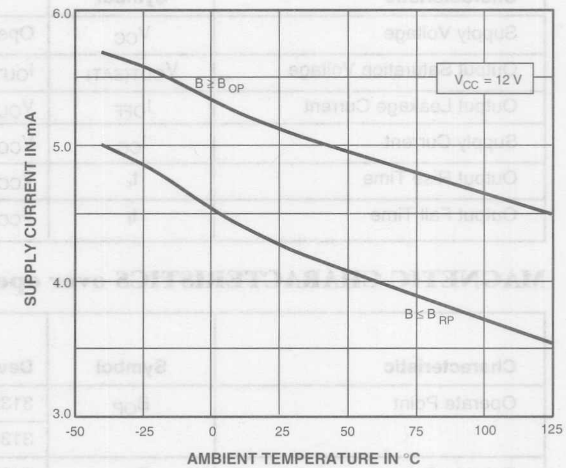
Dwg. No. GH-022



Dwg. No. GH-021



Dwg. No. GH-024

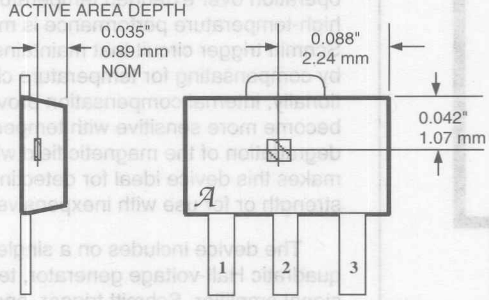


Dwg. No. GH-023

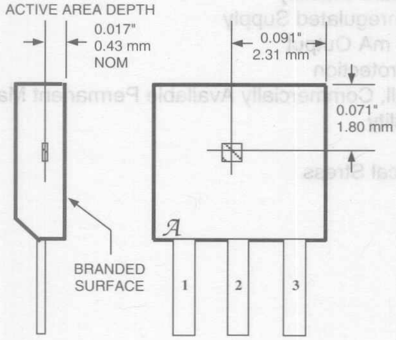
SENSOR LOCATIONS

(±0.005" [0.13mm] die placement)

SUFFIX "LL" & SUFFIX "LT"

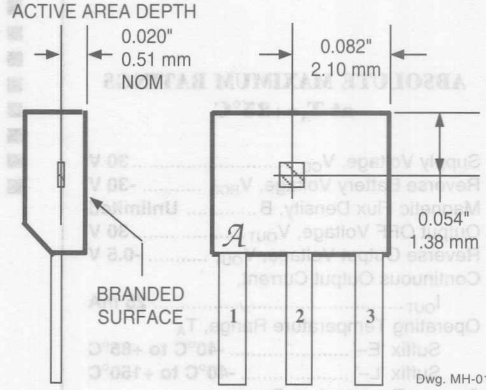


SUFFIX "U"



Dwg. MH-002-2

SUFFIX "UA"

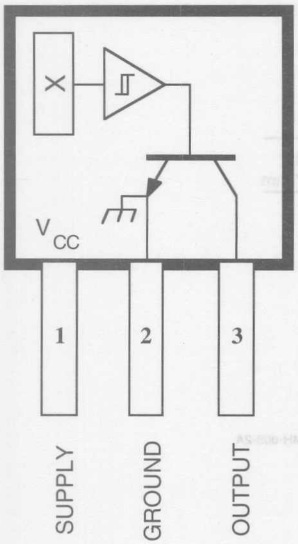


Dwg. MH-011-2A

3134

27631.4

BIPOLAR HALL-EFFECT SWITCH FOR HIGH-TEMPERATURE OPERATION



Dwg. PH-003A

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A=+25°C

Supply Voltage, V_{CC} .... **30 V**
Reverse Battery Voltage, V_{RCC} .... **-30 V**
Magnetic Flux Density, B .... **Unlimited**
Output OFF Voltage, V_{OUT} .... **30 V**
Reverse Output Voltage, V_{OUT} .... **-0.5 V**
Continuous Output Current,
I_{OUT} .... **25 mA**
Operating Temperature Range, T_A
Suffix 'E–' .... **-40°C to +85°C**
Suffix 'L–' .... **-40°C to +150°C**
Storage Temperature Range,
T_S .... **-65°C to +170°C**

This low-hysteresis bipolar Hall-effect switch is an extremely temperature-stable and stress-resistant sensor especially suited for operation over extended temperature ranges to +150°C. Superior high-temperature performance is made possible through a novel Schmitt trigger circuit that maintains operate and release point stability by compensating for temperature changes in the Hall element. Additionally, internal compensation provides magnetic switch points that become more sensitive with temperature, hence offsetting the usual degradation of the magnetic field with temperature. Its low hysteresis makes this device ideal for detecting small changes in magnetic field strength or for use with inexpensive magnets.

The device includes on a single silicon chip a voltage regulator, quadratic Hall-voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and a buffered open-collector output to sink up to 25 mA. The on-board regulator permits operation with supply voltages of 3.8 to 24 volts.

The first character of the part number suffix determines the device operating temperature range; suffix 'E–' is for -40°C to +85°C and 'L–' is -40°C to +150°C. Four package styles provide a magnetically optimized package for most applications. Suffix '–LL' is a long-leaded version of suffix '–LT', a miniature SOT-89/TO-243AA transistor package for surface-mount applications; suffix '–U' is a three-lead plastic mini-SIP while suffix '–UA' is a three-lead ultra-mini-SIP.

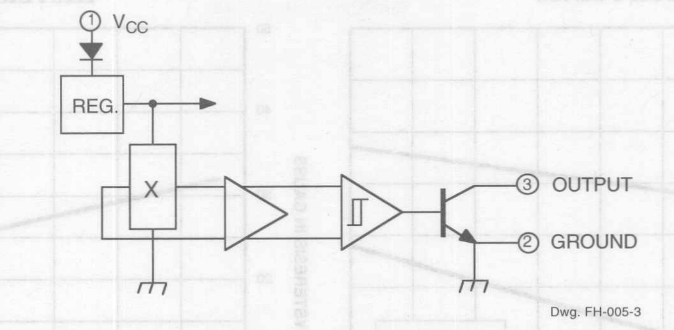
FEATURES

- Superior Temperature Stability
- Operation From Unregulated Supply
- Open-Collector 25 mA Output
- Reverse Battery Protection
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability
- Small Size
- Resistant to Physical Stress

Always order by complete part number, e.g., **A3134ELL**.

3134
LOW-HYSTERESIS BIPOLAR HALL-EFFECT SWITCH FOR HIGH-TEMPERATURE OPERATION

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS over operating temperature range, at V_{CC} = 12 V.

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	3.8	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	0.05	1.0	µA
Supply Current	I_{CC}	B < B_{RP} (Output OFF)	—	3.2	8.0	mA
		B > B_{OP} (Output ON)	—	5.0	—	mA
Output Rise Time	t_r	R_L = 820 Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

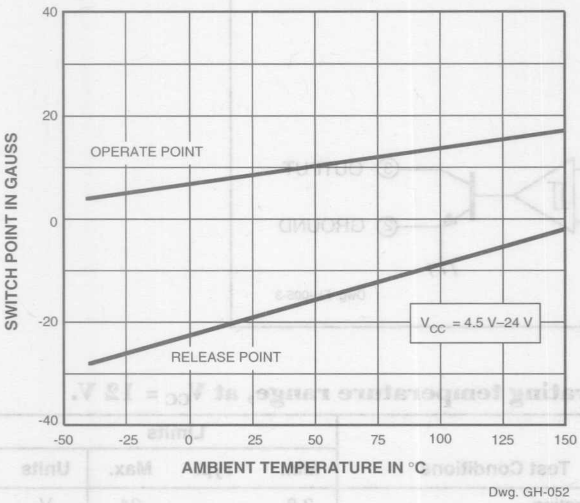
MAGNETIC CHARACTERISTICS over operating supply voltage range.

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Operate Point	B_{OP}	at T_A = +25°C	-30	8.5	45	G
		Over Oper. Temp. Range	-30	–	50	G
Release Point	B_{RP}	at T_A = +25°C	-40	-19	20	G
		Over Oper. Temp. Range	-40	–	30	G
Hysteresis	B_{hys}	at T_A = +25°C	15	27	45	G
		Over Oper. Temp. Range	10	–	50	G

NOTES: B_{OP} = operate point (output turns ON); B_{RP} = release point (output turns OFF); B_{hys} = hysteresis (B_{OP} - B_{RP}).
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C and V_{CC} = 12 V.

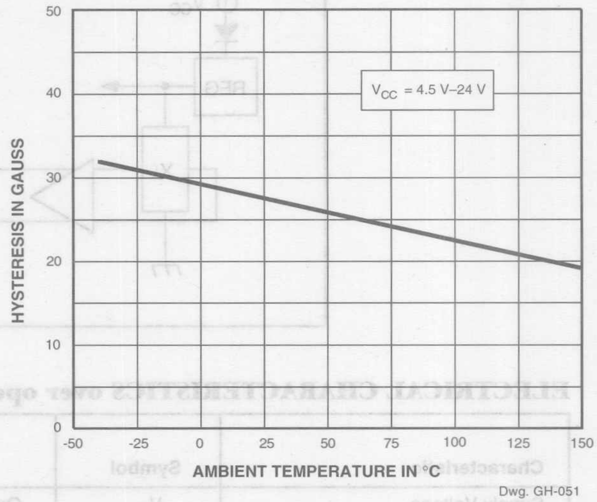
TYPICAL OPERATING CHARACTERISTICS

SWITCH POINTS



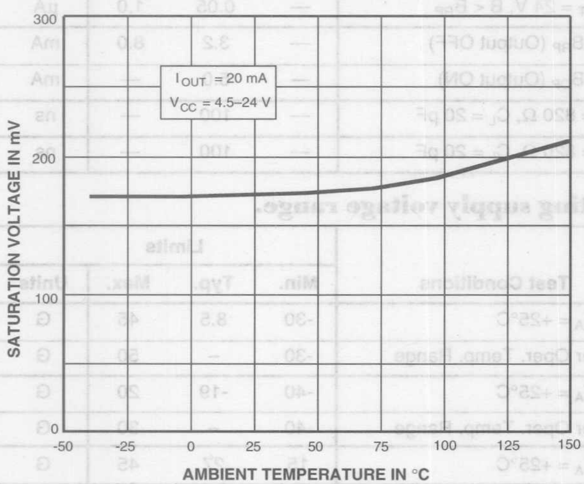
Dwg. GH-052

HYSTERESIS



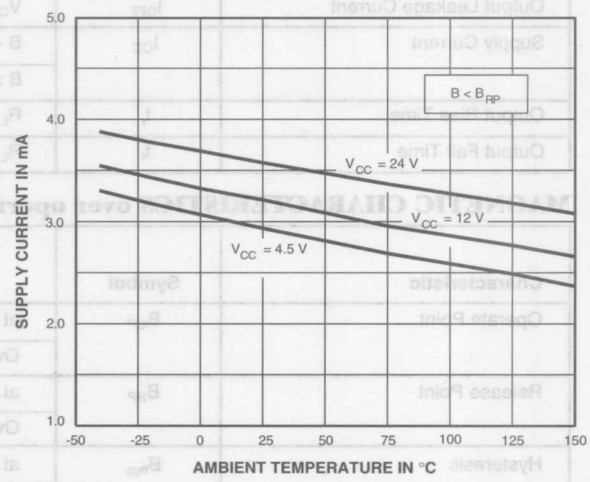
Dwg. GH-051

OUTPUT SATURATION VOLTAGE



Dwg. GH-029

SUPPLY CURRENT

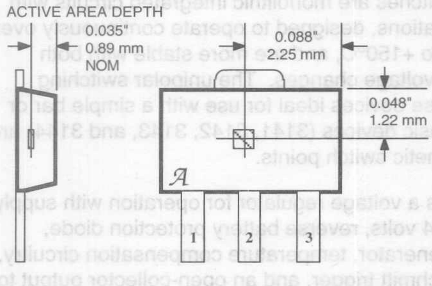


Dwg. GH-058

SENSOR LOCATIONS

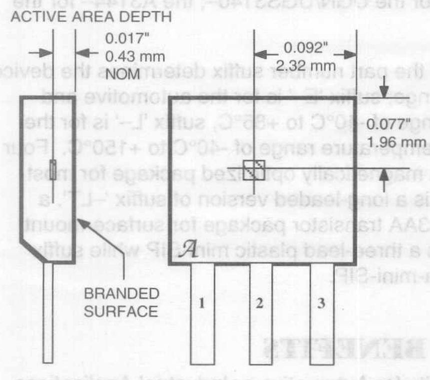
(±0.005" [0.13 mm] die placement)

Suffix "LL" and "LT"



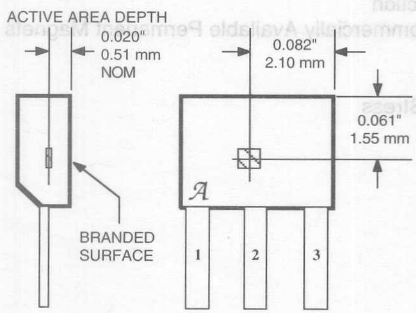
Dwg. MH-008-4A

Suffix "U"



Dwg. MH-002-7A

Suffix "UA"



Dwg. MH-011-4A

APPLICATIONS INFORMATION

Hall effect applications information is available in the "Hall-Effect IC Applications Guide".

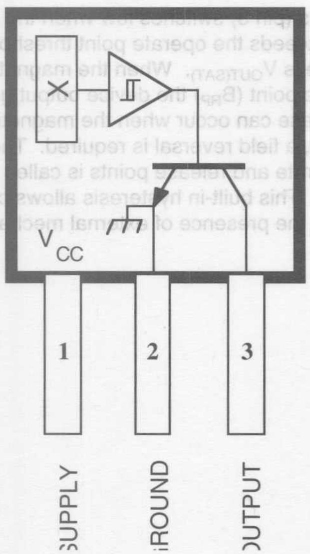
OPERATION

The output of these devices (pin 3) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{OP}). At this point, the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced to below the release point (B_{RP}) the device output goes high. Note especially that release can occur when the magnetic field is removed but to ensure release, a field reversal is required. The difference in the magnetic operate and release points is called the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

3141 THRU 3144

27621.6

SENSITIVE HALL-EFFECT SWITCHES FOR HIGH-TEMPERATURE OPERATION



Dwg. PH-003A

Pinning is shown viewed from branded side.

These Hall-effect switches are monolithic integrated circuits with tighter magnetic specifications, designed to operate continuously over extended temperatures to +150°C, and are more stable with both temperature and supply voltage changes. The unipolar switching characteristic makes these devices ideal for use with a simple bar or rod magnet. The four basic devices (3141, 3142, 3143, and 3144) are identical except for magnetic switch points.

Each device includes a voltage regulator for operation with supply voltages of 4.5 volts to 24 volts, reverse battery protection diode, quadratic Hall-voltage generator, temperature compensation circuitry, small-signal amplifier, Schmitt trigger, and an open-collector output to sink up to 25 mA. With suitable output pull up, they can be used with bipolar or CMOS logic circuits. The A3141– and A3142– are improved replacements for the UGN/UGS3140–; the A3144– for the UGN/UGS3120–.

The first character of the part number suffix determines the device operating temperature range; suffix 'E–' is for the automotive and industrial temperature range of -40°C to +85°C, suffix 'L–' is for the automotive and military temperature range of -40°C to +150°C. Four package styles provide a magnetically optimized package for most applications. Suffix '-LL' is a long-leaded version of suffix '–LT', a miniature SOT-89/TO-243AA transistor package for surface-mount applications; suffix '–U' is a three-lead plastic mini-SIP while suffix '–UA' is a three-lead ultra-mini-SIP.

ABSOLUTE MAXIMUM RATINGS at T_A=+25°C

Supply Voltage, V_{CC}	**28 V**
Reverse Battery Voltage, V_{RCC}	**-35 V**
Magnetic Flux Density, B	**Unlimited**
Output OFF Voltage, V_{OUT}	**28 V**
Reverse Output Voltage, V_{OUT}	**-0.5 V**
Continuous Output Current, I_{OUT}	**25 mA**
Operating Temperature Range, T_A	
Suffix 'E–'	**-40°C to +85°C**
Suffix 'L–'	**-40°C to +150°C**
Storage Temperature Range, T_S	**-65°C to +170°C**

FEATURES and BENEFITS

- Superior Temp. Stability for Automotive or Industrial Applications
- 4.5 V to 24 V Operation … Needs Only An Unregulated Supply
- Open-Collector 25 mA Output … Compatible with Digital Logic
- Reverse Battery Protection
- Activate with Small, Commercially Available Permanent Magnets
- Solid-State Reliability
- Small Size
- Resistant to Physical Stress

Always order by complete part number, e.g., **A3141ELL**.

ELECTRICAL CHARACTERISTICS at V_{CC} = 8 V over operating temperature range.

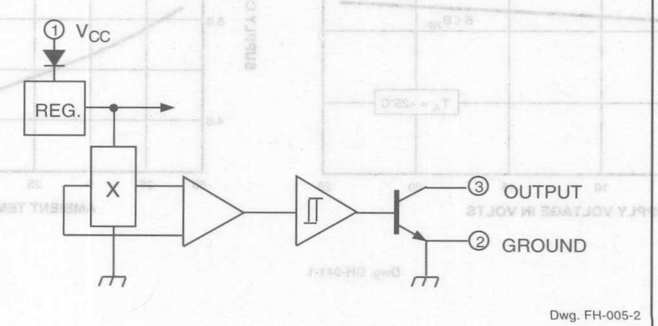
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	<1.0	10	µA
Supply Current	I_{CC}	B < B_{RP} (Output OFF)	—	4.4	9.0	mA
Output Rise Time	t_r	R_L = 820 Ω, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	R_L = 820 Ω, C_L = 20 pF	—	0.18	2.0	µs

MAGNETIC CHARACTERISTICS in gauss over operating supply voltage range.

		Part Numbers*											
		A3141–			A3142–			A3143–			A3144–		
Characteristic		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
B_{OP}	at T_A = 25°C	50	100	160	130	180	230	220	280	340	70	—	350
	over operating temp. range	30	100	175	115	180	245	205	280	355	35	—	450
B_{RP}	at T_A = 25°C	10	45	130	75	125	175	165	225	285	50	—	330
	over operating temp. range	10	45	145	60	125	190	150	225	300	25	—	430
B_{hys}	at T_A = 25°C	20	55	80	30	55	80	30	55	80	20	55	—
	over operating temp. range	20	55	80	30	55	80	30	55	80	20	55	—

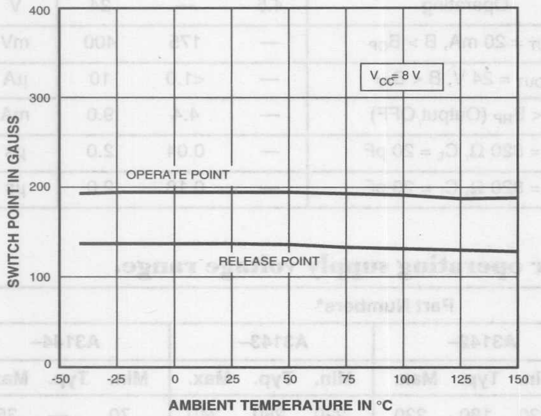
NOTES: Typical values are at T_A = +25°C and V_{CC} = 8 V.
B_{OP} = operate point (output turns ON); B_{RP} = release point (output turns OFF); B_{hys} = hysteresis (B_{OP} - B_{RP}).
*Complete part number includes a suffix to identify operating temperature range (E- or L-) and package type (-LL, -LT, -U, or -UA).

FUNCTIONAL BLOCK DIAGRAM



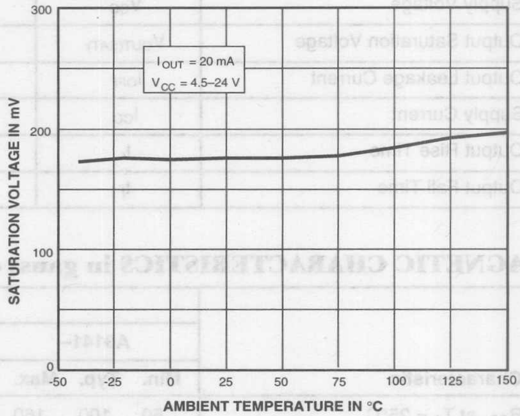
TYPICAL OPERATING CHARACTERISTICS

A3142– SWITCH POINTS



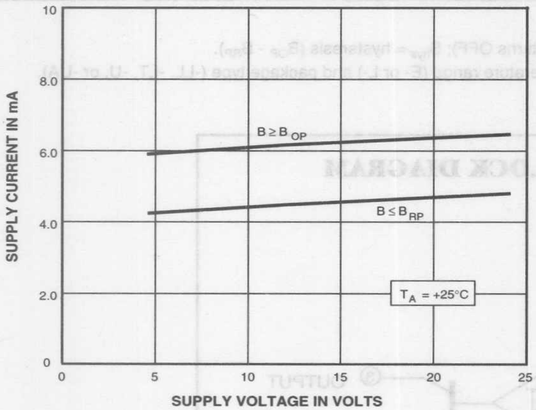
Dwg. GH-044

OUTPUT SATURATION VOLTAGE



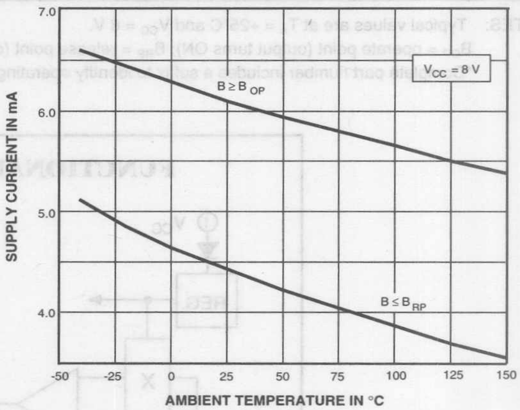
Dwg. GH-040-1

SUPPLY CURRENT



Dwg. GH-041-1

SUPPLY CURRENT

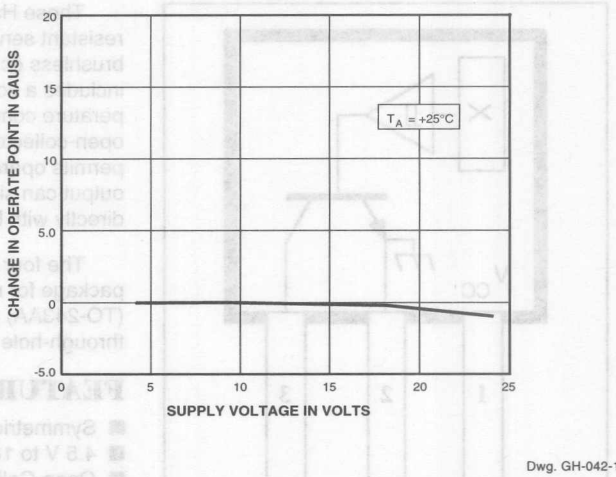


Dwg. GH-039-1

* Complete part number includes a suffix denoting operating temperature range (E- or L-) and package type (-LL, -LT, -U, or -UA).

TYPICAL OPERATING CHARACTERISTICS (cont.)

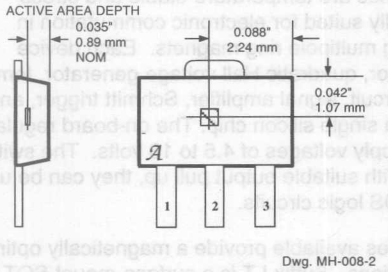
CHANGE IN OPERATE POINT



Dwg. GH-042-1

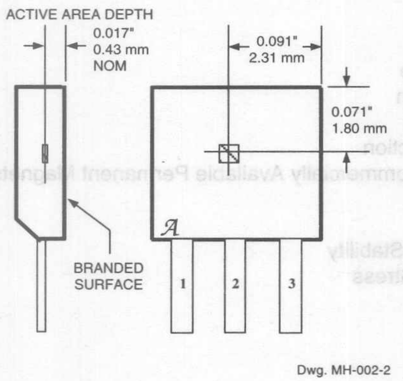
SENSOR LOCATIONS

Suffix "LL" and "LT"



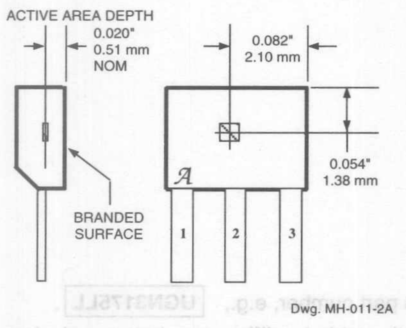
Dwg. MH-008-2

Suffix "U"



Dwg. MH-002-2

Suffix "UA"



Dwg. MH-011-2A

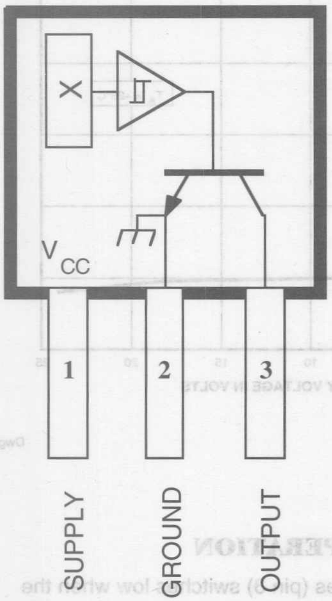
OPERATION

The output of these devices (pin 3) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{OP}). At this point, the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced to below the release point threshold (B_{RP}), the device output goes high. The difference in the magnetic operate and release points is called the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

3175 AND 3177

27609.4

HALL-EFFECT LATCHES



Dwg. No. PH-003A

Pinning is shown viewed from branded side.

These Hall-effect latches are temperature-stable and stress-resistant sensors especially suited for electronic commutation in brushless dc motors using multipole ring magnets. Each device includes a voltage regulator, quadratic Hall voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and an open-collector output on a single silicon chip. The on-board regulator permits operation with supply voltages of 4.5 to 18 volts. The switch output can sink 10 mA. With suitable output pull up, they can be used directly with bipolar or MOS logic circuits.

The four package styles available provide a magnetically optimized package for most applications. Suffix LT is a surface-mount SOT 89 (TO-243AA) package; suffixes LL, U, and UA feature wire leads for through-hole mounting.

FEATURES

- Symmetrical Response
- 4.5 V to 18 V Operation
- Open-Collector Output
- Reverse Battery Protection
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability
- Small Size
- Superior Temperature Stability
- Resistant to Physical Stress

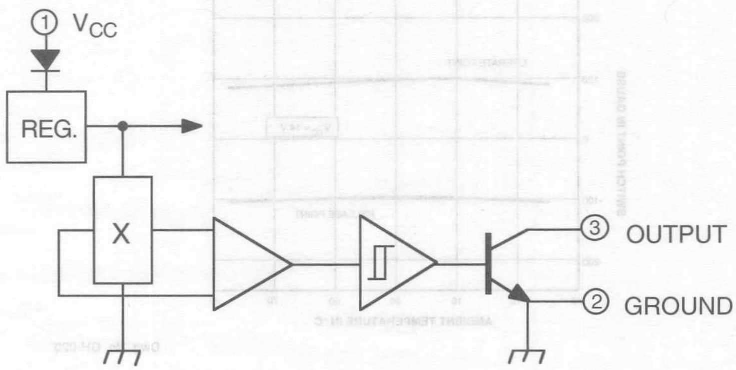
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	**18 V**
Reverse Battery Voltage, V_{RCC}	**-18 V**
Magnetic Flux Density, B	**Unlimited**
Output OFF Voltage, V_{OUT}	**18 V**
Continuous Output Current, I_{OUT}	**15 mA**
Operating Temperature Range, T_A	**-20°C to +85°C**
Storage Temperature Range, T_S	**-65°C to +150°C**

Always order by complete part number, e.g., **UGN3175LL**.

See Magnetic Characteristics table for differences between devices.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FH-005-2

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 18 V (unless otherwise noted).

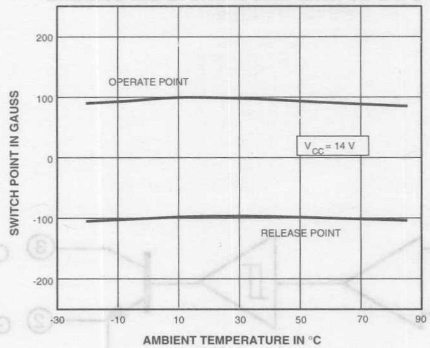
Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	18	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 18 V, I_{OUT} = 10 mA, B > B_{OP}	—	200	300	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 18 V, B < B_{RP}	—	0.05	5.0	µA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	5.0	10	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 1.1 kΩ, C_L = 20 pF	—	0.04	2.0	µs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 1.1 kΩ, C_L = 20 pF	—	0.18	2.0	µs

MAGNETIC CHARACTERISTICS in gauss; V_{CC} = 4.5 V to 18 V.

Characteristic	Part Number*	T_A = +25°C Min.	Typ.	Max.	T_A = -20°C to +85°C Min.	Typ.	Max.
Operate Point, B_{OP}	UGN3175	25	—	170	15	—	180
	UGN3177	50	—	150	25	—	150
Release Point, B_{RP}	UGN3175	-170	—	-25	-180	—	-15
	UGN3177	-150	—	-50	-150	—	-25
Hysteresis, B_{hys}	UGN3175	100	200	—	80	180	—
	UGN3177	100	200	—	50	180	—

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).
Complete part number includes a suffix denoting package type (LL, LT, U, or UA).

TYPICAL OPERATING CHARACTERISTICS

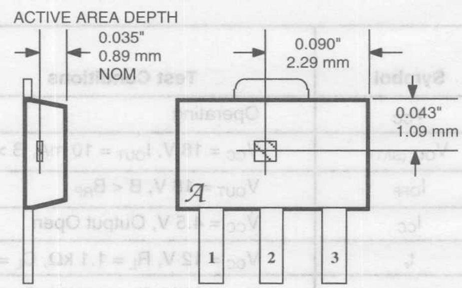


Dwg. No. GH-020

SENSOR LOCATIONS

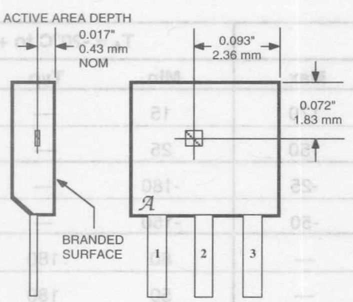
(±0.005" [0.13mm] die placement)

Suffix "LL" & Suffix "LT"



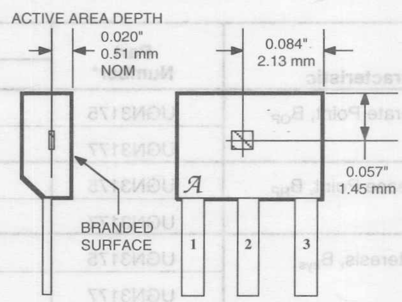
Dwg. No. MH-008-1A

Suffix "U"



Dwg. No. MH-002-3A

Suffix "UA"

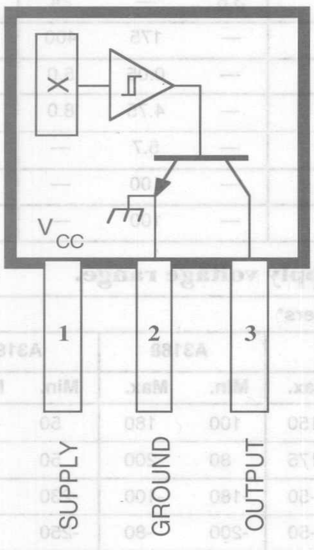


Dwg. No. MH-011A

3185 THRU 3189

27609.2

HALL-EFFECT LATCHES FOR HIGH-TEMPERATURE OPERATION



Dwg. PH-003A

Pinning is shown viewed from branded side.

These Hall-effect latches are extremely temperature-stable and stress-resistant sensors especially suited for operation over extended temperature ranges to +150°C. Superior high-temperature performance is made possible through a novel Schmitt trigger circuit that maintains operate and release point symmetry by compensating for temperature changes in the Hall element. Additionally, internal compensation provides magnetic switch points that become more sensitive with temperature, hence offsetting the usual degradation of the magnetic field with temperature. The symmetry capability makes these devices ideal for use in pulse-counting applications where duty cycle is an important parameter. The five basic devices (3185 through 3189) are identical except for magnetic switch points.

Each device includes on a single silicon chip a voltage regulator, quadratic Hall-voltage generator, temperature compensation circuit, signal amplifier, Schmitt trigger, and a buffered open-collector output to sink up to 25 mA. The on-board regulator permits operation with supply voltages of 3.8 to 24 volts.

The first character of the part number suffix determines the device operating temperature range; suffix 'S–' is for -20°C to +85°C, 'E–' is for -40°C to +85°C, 'K–' is -40°C to +125°C, and 'L–' is -40°C to +150°C. Four package styles provide a magnetically optimized package for most applications. Suffix '—LL' is a long-leaded version of suffix '—LT', a miniature SOT-89/TO-243AA transistor package for surface-mount applications; suffix '–U' is a three-lead plastic mini-SIP while suffix '–UA' is a three-lead ultra-mini-SIP.

ABSOLUTE MAXIMUM RATINGS at T_A=+25°C

Supply Voltage, V_{CC} .... **30 V**
Reverse Battery Voltage, V_{RCC} .... **-30 V**
Magnetic Flux Density, B .... **Unlimited**
Output OFF Voltage, V_{OUT} .... **30 V**
Reverse Output Voltage, V_{OUT} .... **-0.5 V**
Continuous Output Current, I_{OUT} .... **25 mA**
Operating Temperature Range, T_A
Suffix 'S–' .... **-20°C to +85°C**
Suffix 'E–' .... **-40°C to +85°C**
Suffix 'K–' .... **-40°C to +125°C**
Suffix 'L–' .... **-40°C to +150°C**
Storage Temperature Range,
T_S .... **-65°C to +170°C**

FEATURES

- Symmetrical Switch Points
- Superior Temperature Stability
- Operation From Unregulated Supply
- Open-Collector 25 mA Output
- Reverse Battery Protection
- Activate With Small, Commercially Available Permanent Magnets
- Solid-State Reliability
- Small Size
- Resistant to Physical Stress

Always order by complete part number, e.g., **A3185SLL**.

ELECTRICAL CHARACTERISTICS over operating temperature range, at V_{CC} = 12 V.

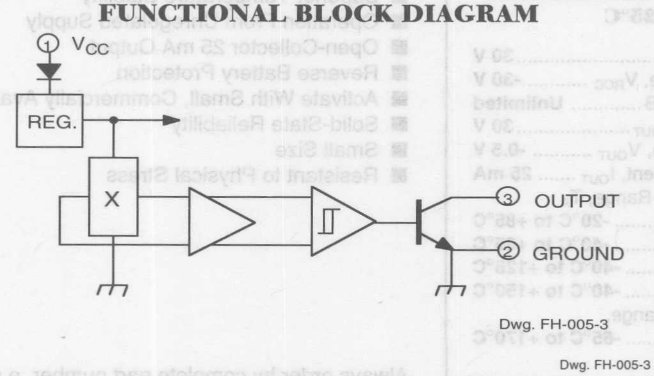
Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	3.8	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	—	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, B < B_{RP}	—	0.05	5.0	µA
Supply Current	I_{CC}	B < B_{RP} (Output OFF)	—	4.75	8.0	mA
		B > B_{OP} (Output ON)	—	5.7	—	mA
Output Rise Time	t_r	R_L = 820 Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

MAGNETIC CHARACTERISTICS in gauss over operating supply voltage range.

	Part Numbers*									
	A3185		A3186		A3187		A3188		A3189	
Characteristic	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
B_{OP} at T_A = 25°C	170	270	70	330	50	150	100	180	50	230
over operating temp range	140	300	30	350	50	175	80	200	50	250
B_{RP} at T_A = 25°C	-270	-170	-330	-70	-150	-50	-180	-100	-230	-50
over operating temp range	-300	-140	-350	-30	-175	-50	-200	-80	-250	-50
B_{hys} at T_A = 25°C	340	540	140	660	100	300	200	360	100	460
over operating temp range	280	600	100	700	100	350	160	400	100	500

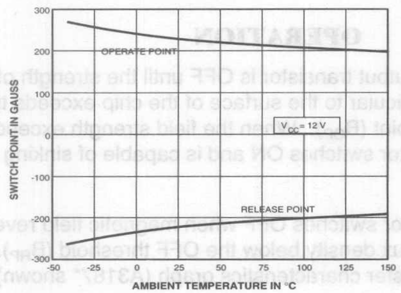
NOTES: B_{OP} = operate point (output turns ON); B_{RP} = release point (output turns OFF); B_{hys} = hysteresis (B_{OP} - B_{RP}).
As used here, negative flux densities are defined as less than zero (algebraic convention).
*Complete part number includes a suffix to identify operating temperature range (E, K, L, or S) and package type (LL, LT, U, or UA).

FUNCTIONAL BLOCK DIAGRAM



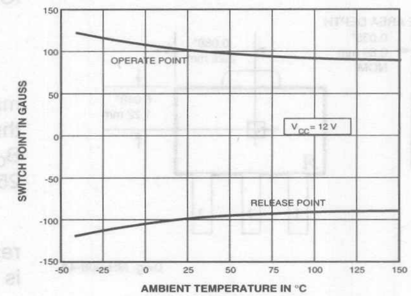
TYPICAL OPERATING CHARACTERISTICS

A3185* SWITCH POINTS



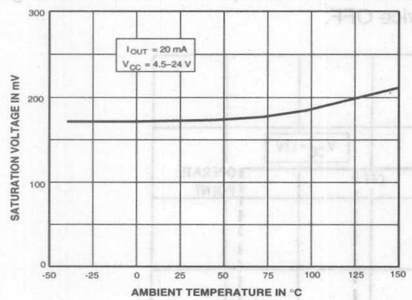
Dwg. GH-026

A3187* SWITCH POINTS



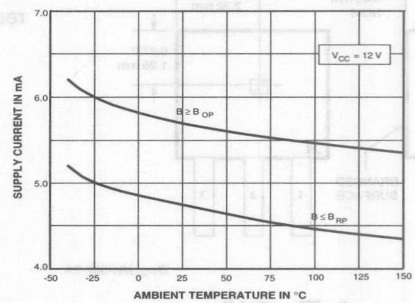
Dwg. GH-027

OUTPUT SATURATION VOLTAGE



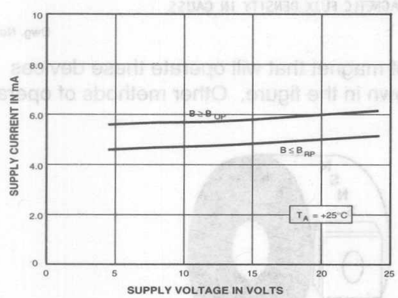
Dwg. GH-029

SUPPLY CURRENT



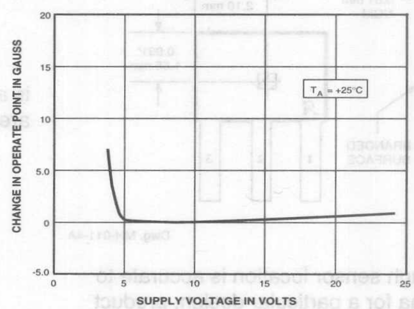
Dwg. GH-028

SUPPLY CURRENT



Dwg. GH-030

OPERATE POINT

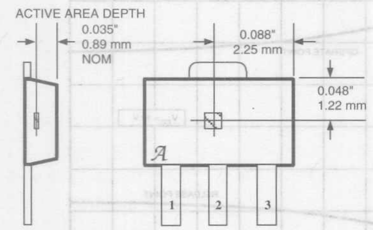


Dwg. GH-037

* Complete part number includes a suffix denoting operating temperature range (E, K, L, or S) and package type (LL, LT, U, or UA).

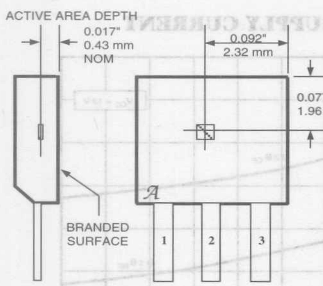
SENSOR LOCATIONS

Suffix "LL" and "LT"



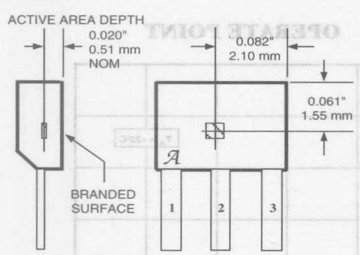
Dwg. MH-008-4A

Suffix "U"



Dwg. MH-002-7A

Suffix "UA"



Dwg. MH-011-4A

Although sensor location is accurate to three sigma for a particular design, product improvements may result in small changes to sensor location.

APPLICATIONS INFORMATION

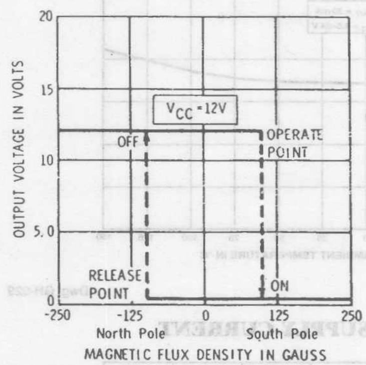
Hall effect applications information is available in the "Hall-Effect IC Applications Guide".

OPERATION

In operation, the output transistor is OFF until the strength of the magnetic field perpendicular to the surface of the chip exceeds the threshold or operate point (B_{OP}). When the field strength exceeds B_{OP}, the output transistor switches ON and is capable of sinking 25 mA of current.

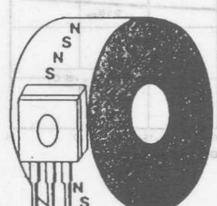
The output transistor switches OFF when magnetic field reversal results in a magnetic flux density below the OFF threshold (B_{RP}). This is illustrated in the transfer characteristics graph (A3187* shown).

Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.



Dwg. No. A-11,739

The simplest form of magnet that will operate these devices is a ring magnet, as shown in the figure. Other methods of operation are possible.

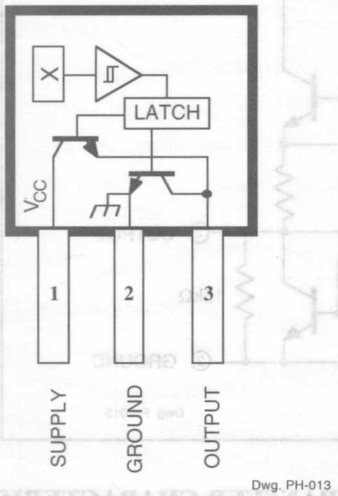


Dwg. No. A-11,899

3195

27609.15

PROTECTED, HIGH-TEMPERATURE, HALL-EFFECT LATCH WITH ACTIVE PULL-DOWN



Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (100 ms) .... **115 V***
(continuous) .... **26 V**
Reverse Battery Voltage,
V_{RCC} (100 ms) .... **-100 V**
(continuous) .... **-30 V**
Magnetic Flux Density, B........... **Unlimited**
Reverse Output Voltage, V_{OUT} .... **-0.5 V**
Continuous Output Current,
I_{OUT} .... **Internally Limited**
Package Power Dissipation,
P_D .... **See Graph**
Junction Temperature, T_J .... **170°C**
Operating Temperature Range, T_A
Suffix "E–" .... **-40°C to +85°C**
Suffix "L–" .... **-40°C to +150°C**
Storage Temperature, T_S .... **170°C**

*Fault condition, internal overvoltage shutdown above 28 V.

These Hall-effect latches are capable of sensing magnetic fields while using an unprotected power supply. The A3195– can provide position and speed information by providing a digital output for magnetic fields that exceed their predefined switch points. These devices operate down to zero speed and have switch points that are designed to be extremely stable over a wide operating temperature and voltage range. The latching characteristics make them ideal for use in pulse counting applications when used with a multi-pole ring magnet.
A 25 mA high-side driver combined with an active pull-down is especially useful for driving capacitive loads. Output short-circuit protection allows for an increased wiring harness fault tolerance. The temperature compensated switch points, the wide operating voltage range, and the integrated protection make these devices ideal for use in automotive applications such as transmission speed sensors and integrated wheel bearing speed sensors.

Each monolithic device contains an integrated Hall-effect transducer, a temperature-compensated comparator, a voltage regulator, and a buffered high-side driver with an active pull-down. Supply protection is made possible by the integration of overvoltage shutdown circuitry that monitors supply fault conditions. Output protection circuitry includes source and sink current current limiting for short circuits to supply or ground.

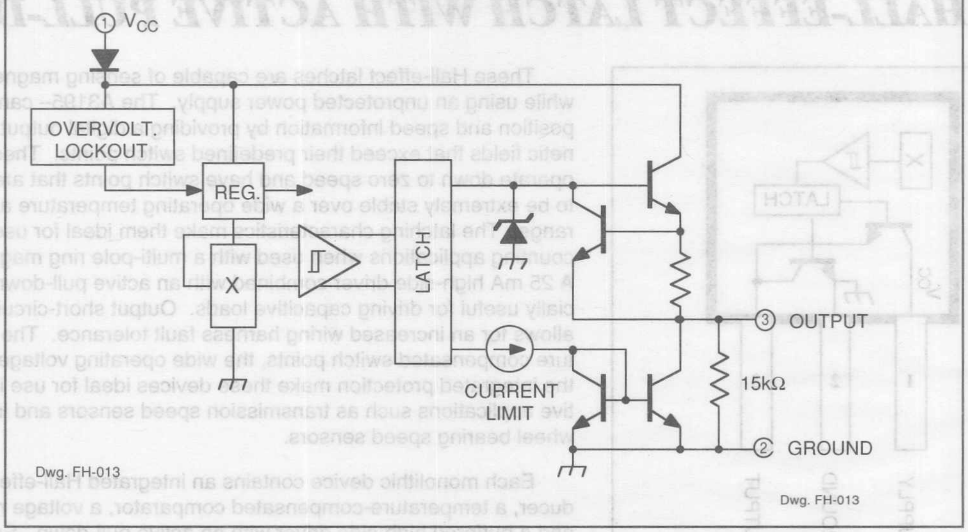
The A3195E– is rated for operation over a temperature range of -40°C to +85°C; the A3195L– is rated for operation over an extended temperature range of -40°C to +150°C. They are supplied in a three-lead SIP (suffix –U) or a surface-mount SOT-89 (suffix –LT).

FEATURES

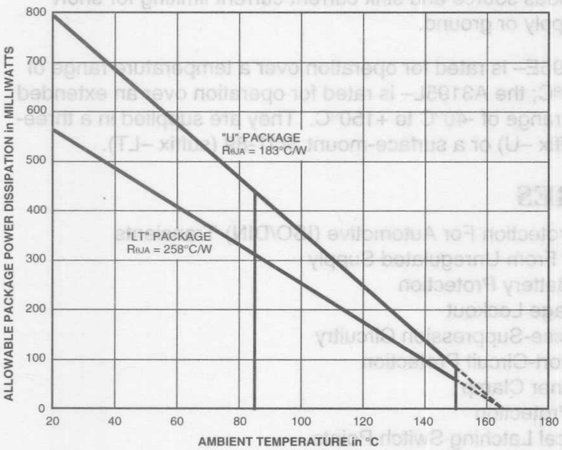
- Internal Protection For Automotive (ISO/DIN) Transients
- Operation From Unregulated Supply
- Reverse Battery Protection
- Undervoltage Lockout
- Supply Noise-Suppression Circuitry
- Output Short-Circuit Protection
- Output Zener Clamp
- Thermal Protection
- Symmetrical Latching Switch Points
- Operable with Multipole Ring Magnets

Always order by complete part number, e.g., **A3195LU**.

FUNCTIONAL BLOCK DIAGRAM

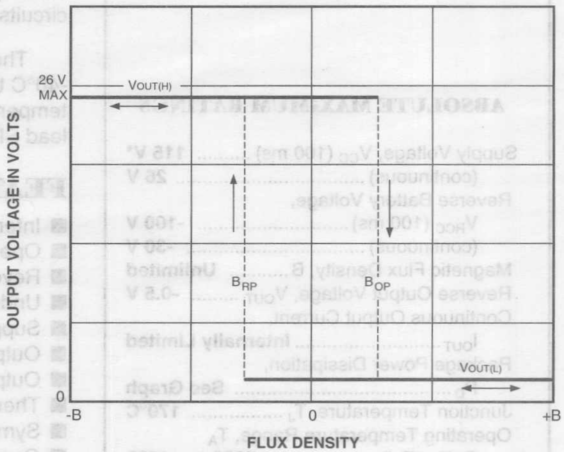


Dwg. FH-013



Dwg. GH-054A

TRANSFER CHARACTERISTICS



Dwg. GH-034-3

ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage	V_{CC}	Operating (but V_{CC} x I_{CC} vs T_A limited)	3.8	12	26	V
Overvoltage Shutdown*	$V_{CC(OV)}$	$B > B_{OP}$	28	—	55	V
Output Voltage, High (Source Voltage)	$V_{OUT(H)}$	$B < B_{RP}$, I_{OUT} = -20 mA	V_{CC} -2	—	V_{CC} -0.3	V
Output Voltage, Low (Sink Voltage)	$V_{OUT(L)}$	$B > B_{OP}$, I_{OUT} <100 µA	—	0.1	0.2	V
		$B > B_{OP}$, I_{OUT} = 5 mA	—	0.25	0.5	V
Output Clamp Voltage	$V_{OUT(CLMP)}$	$B < B_{RP}$, V_{CC} > 26 V, I_{OUT} = 0	15	18	21	V
Output Current Limit	I_{OUTMAX}	$B < B_{RP}$, V_{CC} = 12 V	-26	—	-70	mA
		$B > B_{OP}$, V_{OUT} < 14 V	8.0	—	25	mA
Supply Current	I_{CC}	$B < B_{RP}$, V_{CC} = 18 V, I_{OUT} = 0	—	6.0	9.0	mA
		$B > B_{OP}$, V_{CC} = 18 V, I_{OUT} = 0	—	8.0	12	mA
		V_{CC}= +115 V*	—	8.0	17	mA
Reverse Battery Current*	I_{RCC}	V_{RCC} = -35 V*	—	-0.1	-5.0	mA
		V_{RCC} = -100 V*	—	-0.1	-10	mA
Output Rise Time	t_r	C_L = 20 pF, R_L = 330 Ω	—	0.12	2.0	µs
Output Fall Time	t_f	C_L = 20 pF, R_L = 330 Ω	—	0.30	5.0	µs
Package Thermal Resist.	$R_{\theta JA}$	"LT" Package	—	258	—	°C/W
		"U" Package	—	183	—	°C/W

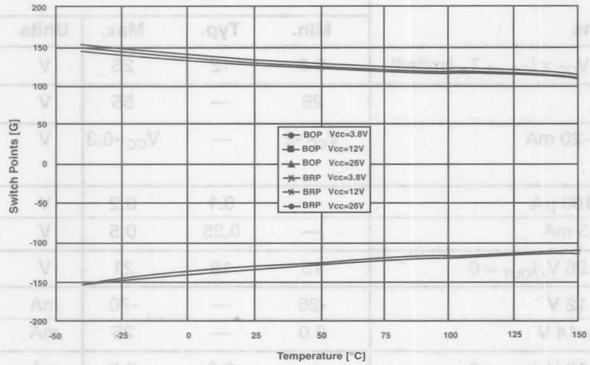
MAGNETIC CHARACTERISTICS over operating voltage (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Operate Point	B_{OP}	T_A = -40°C	60	125	200	G
		T_A = +25°C	50	110	160	G
		T_A = Maximum	40	100	150	G
Release Point	B_{RP}	T_A = -40°C	-200	-125	-60	G
		T_A = +25°C	-160	-110	-50	G
		T_A = Maximum	-150	-100	-40	G
Hysteresis (B_{OP} - B_{RP})	B_{hys}	T_A = -40°C	150	250	—	G
		T_A = +25°C	130	220	—	G
		T_A = Maximum	110	200	—	G

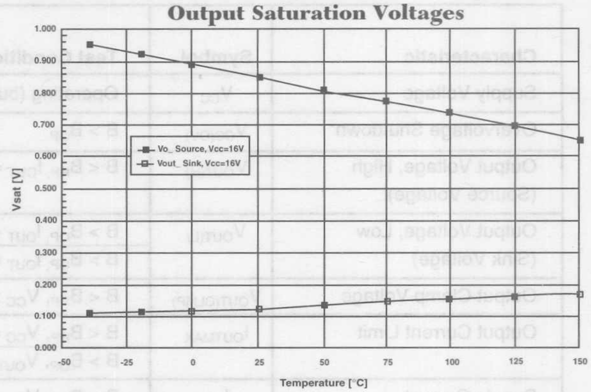
NOTES: Negative current is defined as coming out of (sourcing) the output.
B_{OP} = magnetic operate point (output turns ON); B_{RP} = magnetic release point (output turns OFF).
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C and V_{CC} = 12 V.
* Fault condition. Device is shut down and operation is not possible.

TYPICAL OPERATING CHARACTERISTICS

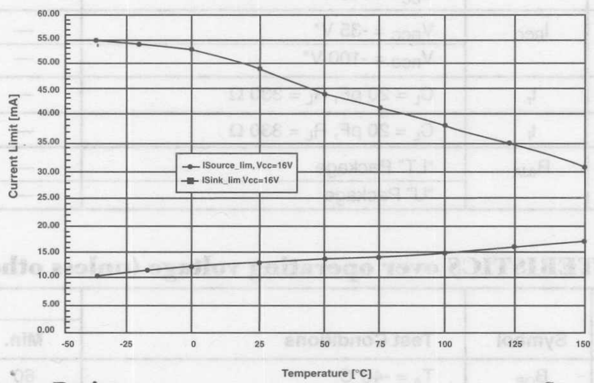
Switch Points



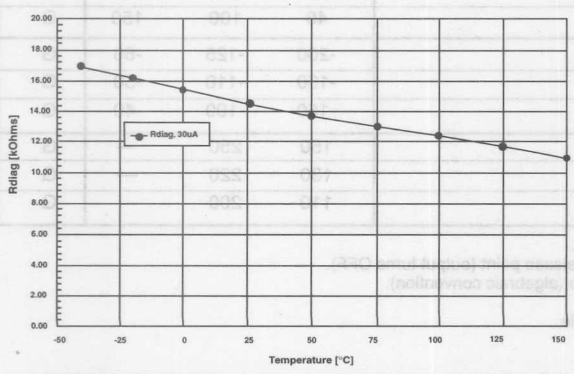
Output Saturation Voltages



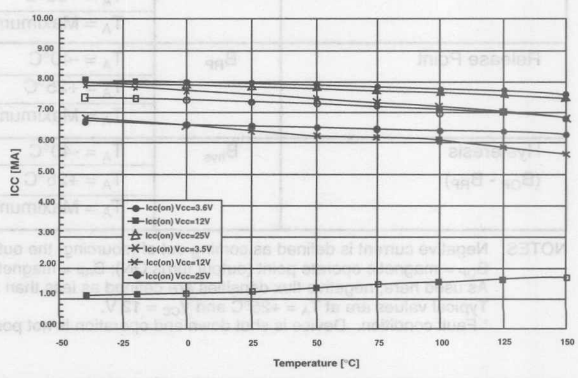
Output Current Limit



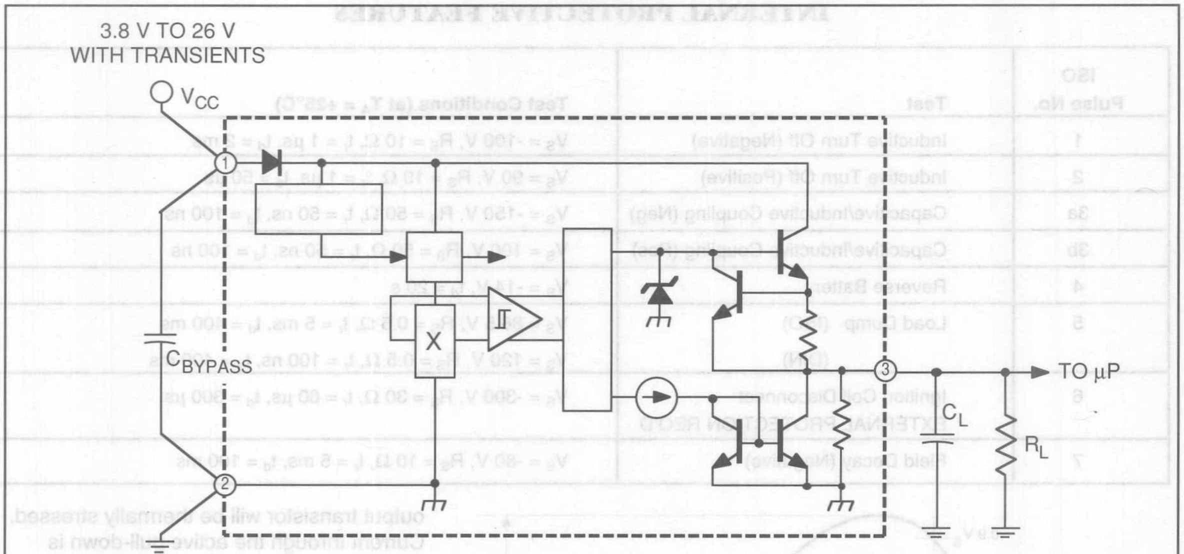
Internal Pull-Down Resistance



Supply Current



3195
PROTECTED, HIGH-TEMPERATURE, ACTIVE PULL-DOWN HALL-EFFECT LATCH



Dwg. EH-007

OPERATION

In operation, the output transistor is OFF until the strength of the magnetic field perpendicular to the surface of the chip exceeds the threshold or operate point (B_{OP}). When the field strength exceeds B_{OP}, the output transistor switches ON (a logic low) and is capable of sinking 35 mA of current.

The output transistor switches OFF (a logic high) when magnetic field reversal results in a magnetic flux density below the OFF threshold (B_{RP}). This is illustrated in the transfer characteristics graph. Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

The switch points increase in sensitivity with increasing temperature to compensate for the typical ferrite magnet temperature characteristic. The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation are possible.

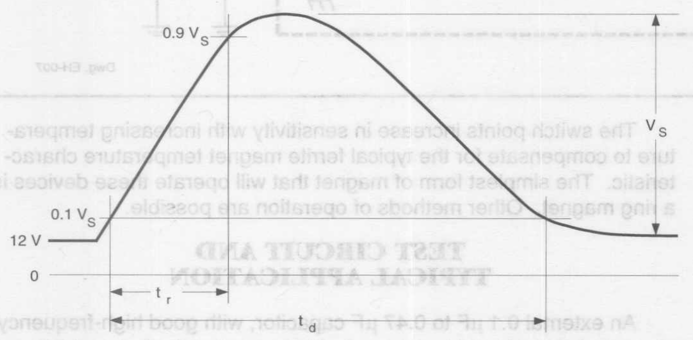
TEST CIRCUIT AND TYPICAL APPLICATION

An external 0.1 µF to 0.47 µF capacitor, with good high-frequency characteristics, should be connected between terminals 1 and 2 to bypass high-voltage noise and reduce EMI susceptibility.

Internal Pull-Down Resistor. An internal pull-down resistor (nominal 15 kΩ) is provided to allow testing of the device without the need for an external load.

INTERNAL PROTECTIVE FEATURES

ISO Pulse No.	Test	Test Conditions (at $T_A = +25°C$)
1	Inductive Turn Off (Negative)	V_S = -100 V, R_S = 10 Ω, t_r = 1 µs, t_d = 2 ms
2	Inductive Turn Off (Positive)	V_S = 90 V, R_S = 10 Ω, t_r = 1 µs, t_d = 50 µs
3a	Capacitive/Inductive Coupling (Neg)	V_S = -150 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
3b	Capacitive/Inductive Coupling (Pos)	V_S = 100 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
4	Reverse Battery	V_S = -14 V, t_d = 20 s
5	Load Dump (ISO)	V_S = 86.5 V, R_S = 0.5 Ω, t_r = 5 ms, t_d = 400 ms
	(DIN)	V_S = 120 V, R_S = 0.5 Ω, t_r = 100 ns, t_d = 400 ms
6	Ignition Coil Disconnect EXTERNAL PROTECTION REQ'D	V_S = -300 V, R_S = 30 Ω, t_r = 60 µs, t_d = 300 µs
7	Field Decay (Negative)	V_S = -80 V, R_S = 10 Ω, t_r = 5 ms, t_d = 100 ms



Dwg. WH-008

Power supply voltage transients, or device output short circuits, may be caused by faulty connectors, crimped wiring harnesses, or service errors. To prevent catastrophic failure, internal protection against overvoltage, reverse voltage, output overloads have been incorporated to meet the automotive 12 volt system protection requirements of ISO DP7637/1 and DIN 40839-1. A series-blocking diode or current-limiting resistor is required in order to survive pulse number six.

Output Overloads. Current through the output source transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to between -26 mA and -70 mA. Under short-circuit conditions, the device will dissipate an increased amount of power ($P_D = V_{OUT} \times I_{LIMIT}$) and the output transistor will be thermally stressed. Current through the active pull-down is limited to between 8 mA and 25 mA.

Overvoltage. The device protects itself against high-voltage transients by shutting OFF the output source driver and all supply-referenced active components, reducing the supply current, and minimizing device power dissipation. Overvoltage shutdown can occur anywhere between 28 V and 55 V and device operation above 28 V cannot be recommended. The device will continue to operate, with increased power dissipation, for supply voltages above the internal clamp voltage but below the over-voltage shutdown. Under a sustained overvoltage, the device may be required to dissipate an increased amount of power ($P_D = V_{CC} \times I_{CC}$) and the device may be thermally stressed (see above).

Output Voltage. The output is clamped with an on-chip Zener diode to prevent supply overvoltage faults from appearing at the output when the field is less than B_{RP}.

When any fault condition is removed, the device returns to normal operating mode.

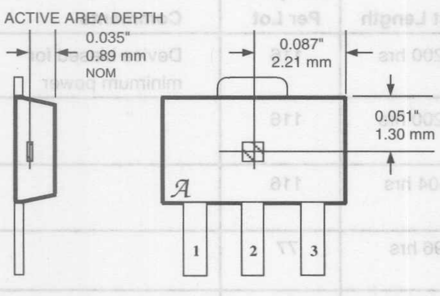
CRITERIA FOR DEVICE QUALIFICATION

All Allegro sensors are subjected to stringent qualification requirements prior to being released to production. To become qualified, except for the destructive ESD tests, no failures are permitted.

Qualification Test	Test Method and Test Conditions	No. of Lots	Test Length	Samples Per Lot	Comments
Biased Humidity	JESD22-A101 T_A = 85°C, RH = 85%	3	1200 hrs	116	Device biased for minimum power
High-Temperature Operating Life	JESD22-A108 T_A = 150°C, T_J = 165°C	3	1200 hrs	116	
Surge Operating Life	JESD22-A108 T_A = 175°C, T_J = 190°C	1	504 hrs	116	
Pressure Cooker, Unbiased	JESD22-A102, Method C	3	96 hrs	77	
Storage Life	MIL-STD-883, Method 1008 T_A = 170°C	1	1200 hrs	77	
Temperature Cycle	MIL-STD-883, Method 1010	3	1000 cycles	153	
ESD Human Body Model	MIL-STD-883, Method 3015	1	Pre/Post Reading	3 per test	Test to failure HBM ≥ 12 kV
ESD Machine Model		1	Pre/Post Reading	3 per test	Test to failure MM ≥ 600 V

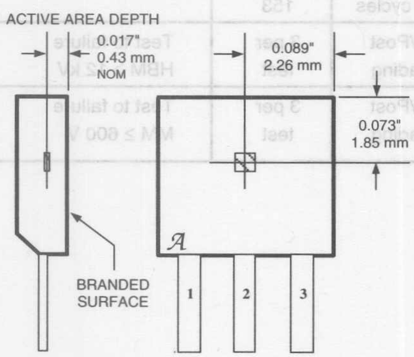
SENSOR LOCATIONS (±0.005" [0.13 mm] die placement)

SUFFIX "LT"



Dwg. MH-008-6

SUFFIX "U"



Dwg. MH-002-13

APPLICATIONS INFORMATION

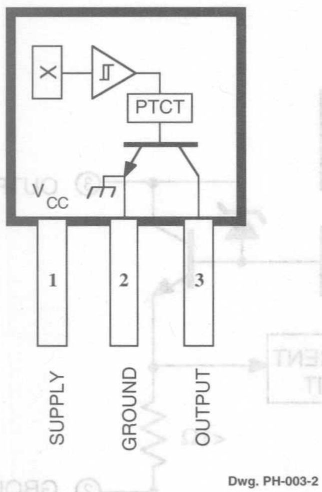
The A3195– latch has been optimized for use in automotive ring magnet sensing applications. Such applications include transmission speed sensors, motor position encoders, and wheel bearing speed sensors. Special care has been taken to optimize the operation of these devices in automotive subsystems that require ISO DP9637 protection but NOT operation. Short-circuit protection is included to prevent damage caused by pinched wiring harnesses. An on-chip pull-down resistor is provided to allow device testing without the connection of the control module.

A typical application consists of a ferrite ring magnet located on a rotating shaft. Typically, this shaft is attached to the transmission, the sensor is mounted on a board, with care being taken to keep a tight tolerance on the air gap between the package face and the magnet. The device will provide a change in digital state at the transition of every magnetic pole and, thus, give an indication of the transmission speed. The high magnetic hysteresis allows the device to be immune to vibration of the magnet shaft and relatively good duty cycles can be obtained.

Hall effect applications information is available in the "Hall-Effect IC Applications Guide".

27609.10

PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}
- (100 ms) .... **115 V***
- (continuous) **26V**

Reverse Battery Voltage, V_{RCC}
- (100 ms) .... **-100 V**
- (continuous) .... **-30 V**

Magnetic Flux Density, B .... **Unlimited**
Output OFF Voltage, V_{OUT} .... **26 V**
Reverse Output Voltage V_{OUT} .... **-0.5 V**
Continuous Output Current,
- I_{OUT} .... **Internally Limited**

Reverse Output Current,
- I_{OUT} ....**-100 mA**

Package Power Dissipation,
- P_D .... **See Graph**

Junction Temperature, T_J .... **170 °C**
Operating Temperature Range, T_A
- Suffix "E–" ....**-40°C to +85°C**
- Suffix "L–" ....**-40°C to +150°C**

Storage Temperature, T_S .... **170 °C**

*Fault condition, internal overvoltage shutdown above 28V.

These open-collector Hall-effect latches are capable of sensing magnetic fields while using an unprotected power supply. The A3197– can provide position and speed information by providing a digital output for magnetic fields that exceed their predefined switch points. These devices operate down to zero speed and have switch points that are designed to be extremely stable over a wide operating temperature and voltage range. The latching characteristics make them ideal for use in pulse counting applications when used with a multi-pole ring magnet. Thermal and output short-circuit protection allow an increased wiring harness fault tolerance. The temperature compensated switch points, the wide operating voltage range, and the integrated protection make these devices ideal for use in automotive applications such as transmission speed sensors and integrated wheel bearing speed sensors.

Each monolithic device contains an integrated Hall-effect transducer, a temperature-compensated comparator, a voltage regulator, and a buffered 35 mA output sink stage. Supply protection is made possible by the integration of overvoltage and undervoltage shutdown circuitry that monitor supply fault conditions and shut down the IC. Noise shutdown circuitry (patent applied for) prevents the propagation of supply transients to the logic load. Output protection circuitry includes a current limit loop that limits the maximum output sink current, and thermal protection circuitry that shuts down the device during an over-heating condition such as with a shorted load.

The A3197E– is rated for operation over a temperature range of -40°C to +85°C; the A3197L– is rated for operation over an extended temperature range of -40°C to +150°C. They are supplied in a three-lead SIP (suffix –U) or a surface-mount SOT-89 (suffix –LT).

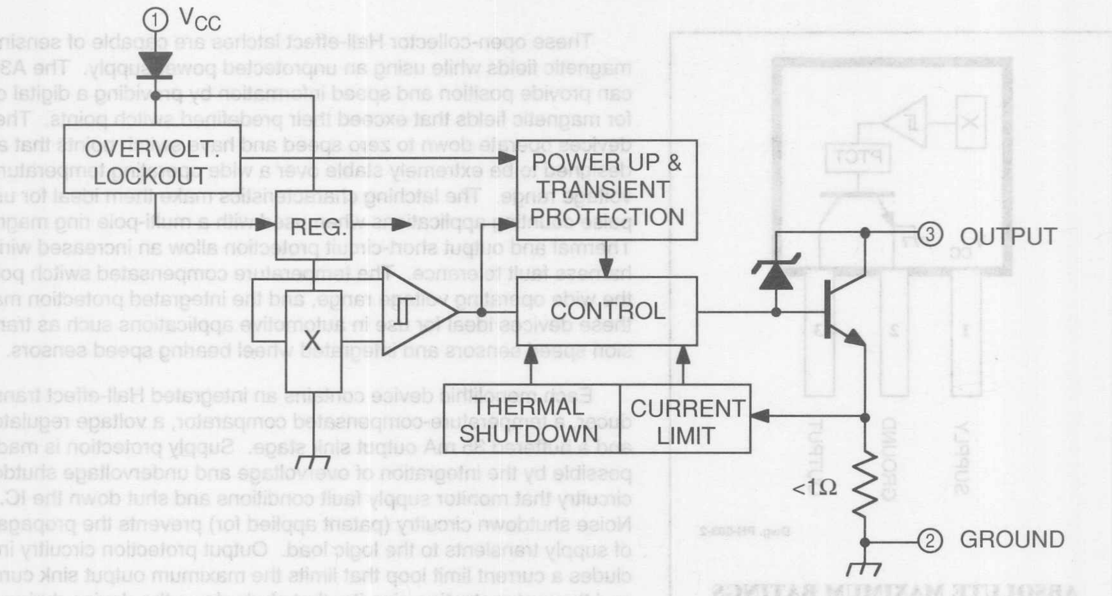
FEATURES

- Internal Protection For Automotive (ISO/DIN) Transients
- Operation From Unregulated Supply
- Reverse Battery Protection
- Undervoltage Lockout
- Supply Noise-Suppression Circuitry
- Output Short-Circuit Protection
- Output Zener Clamp
- Thermal Protection
- Symmetrical Latching Switch Points
- Operable with Multipole Ring Magnets

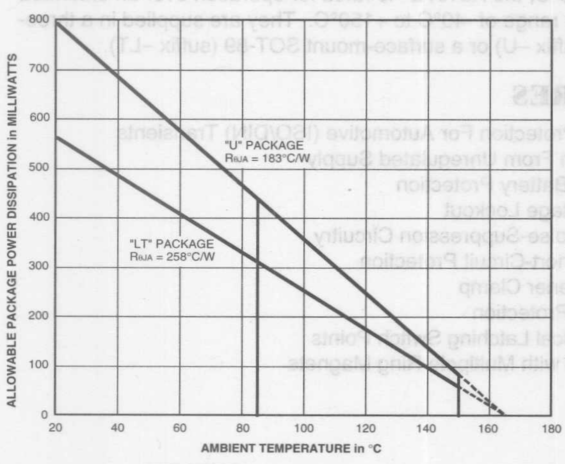
Always order by complete part number, e.g., **A3197LU**.

3197
PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH

FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-012A



Dwg. GH-054A

3197
PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH

ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage	V_{CC}	Operating (but V_{CC} x I_{CC} vs T_A limited)	$V_{CC(UV)}$	12	26	V
Overvoltage Shutdown*	$V_{CC(OV)}$	$B > B_{OP}$	28	—	55	V
Undervoltage Shutdown*	$V_{CC(UV)}$	$B > B_{OP}$	3.7	—	4.5	V
Output Voltage, On	$V_{OUT(SAT)}$	$B > B_{OP}$, I_{OUT} = 30 mA, V_{CC} = 16 V	—	0.2	0.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 26 V	—	—	5.0	µA
Output Clamp Voltage	$V_{OUT(CLMP)}$	$B < B_{RP}$, V_{CC} = 115 V*, I_{OUT} = 0	28	32	40	V
Output Current Limit	$I_{OUT}MAX$	$B > B_{OP}$, V_{OUT} = 12 V	35	50	70	mA
Supply Current	I_{CC}	$B < B_{RP}$, V_{CC} = 24 V	—	6.0	9.0	mA
		$B > B_{OP}$, I_{OUT} = 20 mA	—	8.0	12	mA
		V_{CC} = +115 V*	—	8.0	17	mA
Reverse Battery Current*	I_{RCC}	V_{RCC} = -35 V*	—	-0.5	-5.0	mA
		V_{RCC} = -100 V*	—	-2.0	-10	mA
Output Rise Time	t_r	C_L = 20 pF, R_L = 330 Ω, V_{BB} = 12 V	—	0.05	2.0	µs
Output Fall Time	t_f	C_L = 20 pF, R_L = 330 Ω, V_{BB} = 12 V	—	0.30	5.0	µs
Thermal Shutdown Temp.*	T_J		165	—	190	°C
Package Thermal Resist.	$R_{\theta JA}$	"LT" Package	—	258	—	°C/W
		"U" Package	—	183	—	°C/W

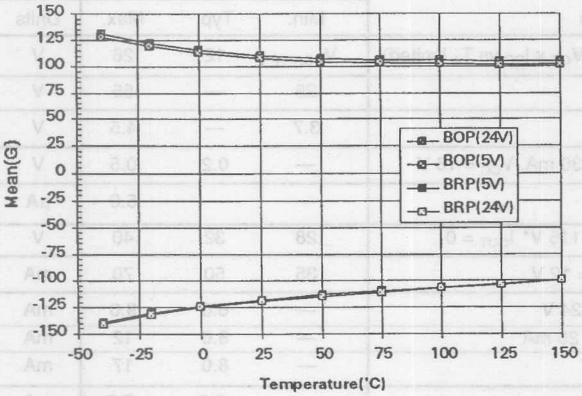
MAGNETIC CHARACTERISTICS over operating voltage (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Operate Point	B_{OP}	T_A = -40°C	60	125	200	G
		T_A = +25°C	50	110	160	G
		T_A = Maximum	40	100	150	G
Release Point	B_{RP}	T_A = -40°C	-200	-125	-60	G
		T_A = +25°C	-160	-110	-50	G
		T_A = Maximum	-150	-100	-40	G
Hysteresis (B_{OP} - B_{RP})	B_{hys}	T_A = -40°C	150	250	—	G
		T_A = +25°C	130	220	—	G
		T_A = Maximum	110	200	—	G

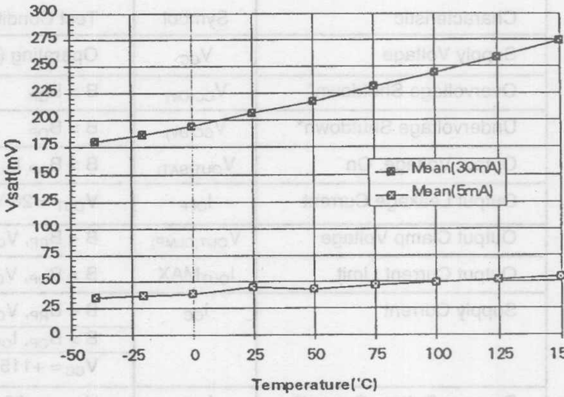
NOTES: B_{OP} = magnetic operate point (output turns ON); B_{RP} = magnetic release point (output turns OFF).
As used here, negative flux densities are defined as less than zero (algebraic convention).
Typical values are at T_A = +25°C and V_{CC} = 12 V.
* Fault condition. Device is shut down and operation is not possible.

TYPICAL OPERATING CHARACTERISTICS

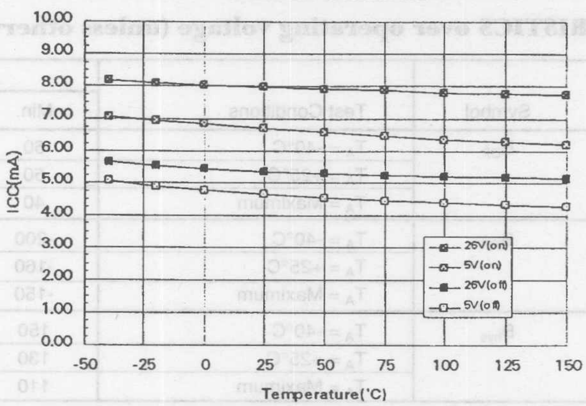
SWITCH POINTS



OUTPUT SATURATION VOLTAGE



SUPPLY CURRENT



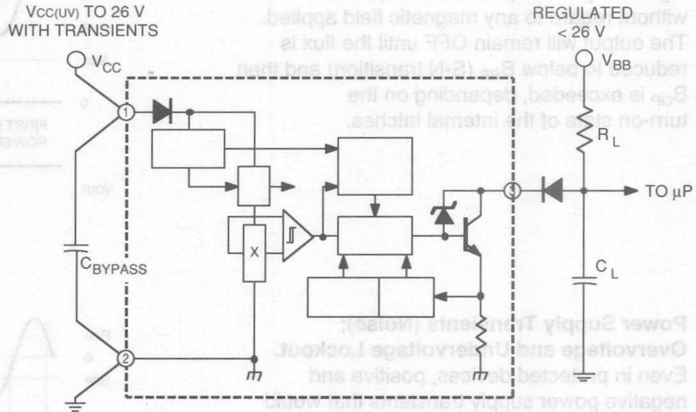
OPERATION

In operation, the output transistor is OFF until the strength of the magnetic field perpendicular to the surface of the chip exceeds the threshold or operate point (B_{OP}). When the field strength exceeds B_{OP}, the output transistor switches ON (a logic low) and is capable of sinking 35 mA of current.

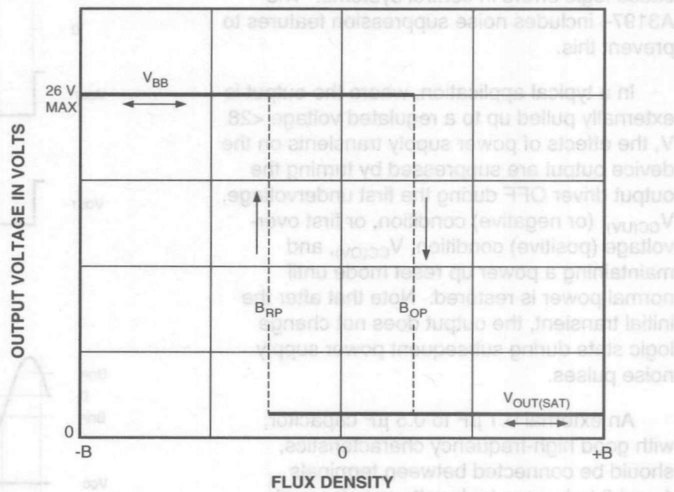
The output transistor switches OFF (a logic high) when magnetic field reversal results in a magnetic flux density below the OFF threshold (B_{RP}). This is illustrated in the transfer characteristics graph. Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

The switch points increase in sensitivity with increasing temperature to compensate for the typical ferrite magnet temperature characteristic. The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation are possible.

TEST CIRCUIT AND TYPICAL APPLICATION



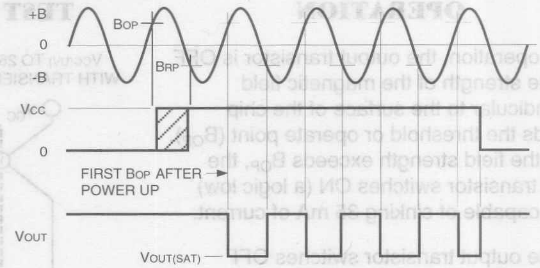
Dwg. EH-006A



Dwg. GH-034-2A

3197
PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH

Power Up Reset. These devices are designed to power up with the output OFF without regard to any magnetic field applied. The output will remain OFF until the flux is reduced to below B_{RP} (S-N transition) and then B_{OP} is exceeded, depending on the turn-on state of the internal latches.

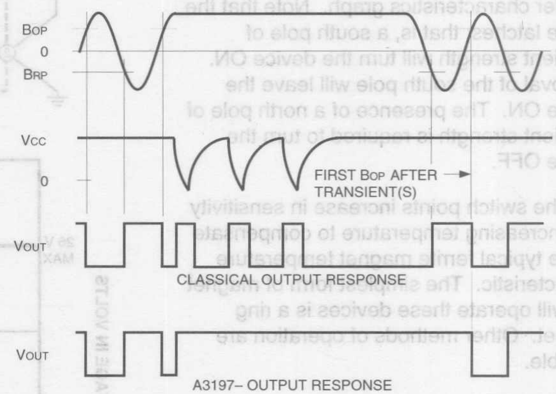


Dwg. WH-006

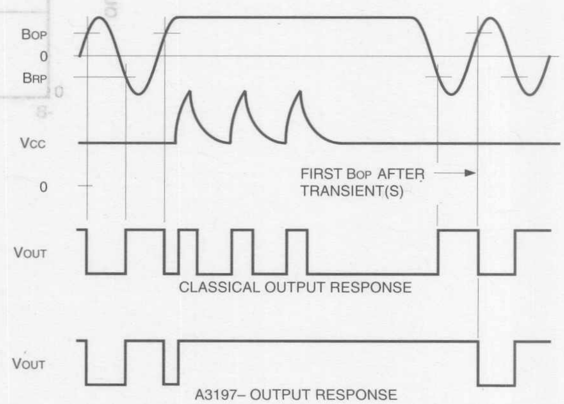
Power Supply Transients (Noise); Overvoltage and Undervoltage Lockout. Even in protected devices, positive and negative power supply transients that would not normally cause physical damage can cause logic errors in control systems. The A3197– includes noise suppression features to prevent this.

In a typical application, where the output is externally pulled up to a regulated voltage <28 V, the effects of power supply transients on the device output are suppressed by turning the output driver OFF during the first undervoltage, $V_{CC(UV)}$, (or negative) condition, or first overvoltage (positive) condition, $V_{CC(OV)}$, and maintaining a power up reset mode until normal power is restored. Note that after the initial transient, the output does not change logic state during subsequent power supply noise pulses.

An external 0.1 µF to 0.5 µF capacitor, with good high-frequency characteristics, should be connected between terminals 1 and 2 to bypass high-voltage noise and reduce EMI susceptibility.



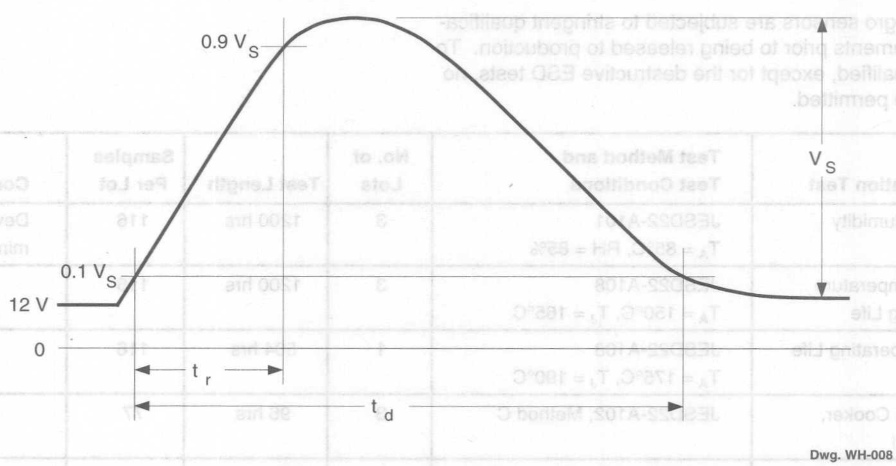
Dwg. WH-007-2A



Dwg. WH-007-1A

INTERNAL PROTECTIVE FEATURES

ISO Pulse No.	Test	Test Conditions (over operating temperature range)
1	Inductive Turn Off (Negative)	V_S = -100 V, R_S = 10 Ω, t_r = 1 µs, t_d = 2 ms
2	Inductive Turn Off (Positive)	V_S = 100 V, R_S = 10 Ω, t_r = 1 µs, t_d = 50 µs
3a	Capacitive/Inductive Coupling (Neg)	V_S = -150 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
3b	Capacitive/Inductive Coupling (Pos)	V_S = 100 V, R_S = 50 Ω, t_r = 50 ns, t_d = 100 ns
4	Reverse Battery	V_S = -14 V, t_d = 20 s
5	Load Dump	(ISO) V_S = 86.5 V, R_S = 0.5 Ω, t_r = 5 ms, t_d = 400 ms (DIN) V_S = 120 V, R_S = 0.5 Ω, t_r = 100 ns, t_d = 400 ms
6	Ignition Coil Disconnect EXTERNAL PROTECTION REQ'D	V_S = -300 V, R_S = 30 Ω, t_r = 60 µs, t_d = 300 µs
7	Field Decay (Negative)	V_S = -80 V, R_S = 10 Ω, t_r = 5 ms, t_d = 100 ms



Power supply voltage transients, or device output short circuits, may be caused by faulty connectors, crimped wiring harnesses, or service errors. To prevent catastrophic failure, internal protection against overvoltage, reverse voltage, output overloads, and thermal stress have been incorporated to meet the automotive 12 volt system protection requirements of ISO DP7637/1 and DIN 40839-1. A series-blocking diode or current-limiting resistor is required in order to survive pulse number six.

Output Overloads. Current through the output transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to between 35 mA and 70 mA. Under short-circuit conditions, the device will dissipate an increased amount of power ($P_D = V_{OUT} \times I_{LIMIT}$) and the output transistor will be thermally stressed.

Thermal Stress. When thermal stresses (either internal or external) cause the junction temperature to exceed +165°C, thermal shutdown of the output transistor is activated. The thermal shutdown circuitry only provides protection against thermal stresses caused by increased power dissipation of the output transistor.

Overvoltage. The device protects itself against high-voltage transients by shutting OFF all supply-referenced active components, reducing the supply current, and minimizing device power dissipation. Overvoltage shutdown can occur anywhere between 28 V and 55 V and device operation above 28 V cannot be recommended. Under a sustained overvoltage, the device may be required to dissipate an increased amount of power ($P_D = V_{CC} \times I_{CC}$) and the device may be thermally stressed (see above).

Output Voltage. The output is clamped with an on-chip Zener diode to limit the maximum output voltage that can occur during overvoltage faults or when switching an inductive load.

When any fault condition is removed, the device returns to normal operating mode.

CRITERIA FOR DEVICE QUALIFICATION

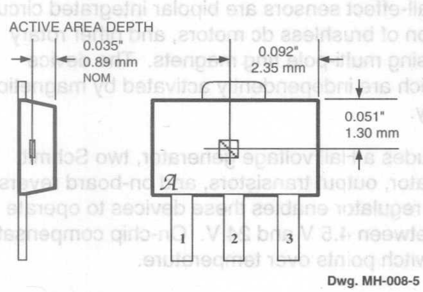
All Allegro sensors are subjected to stringent qualification requirements prior to being released to production. To become qualified, except for the destructive ESD tests, no failures are permitted.

Qualification Test	Test Method and Test Conditions	No. of Lots	Test Length	Samples Per Lot	Comments
Biased Humidity	JESD22-A101 T_A = 85°C, RH = 85%	3	1200 hrs	116	Device biased for minimum power
High-Temperature Operating Life	JESD22-A108 T_A = 150°C, T_J = 165°C	3	1200 hrs	116	
Surge Operating Life	JESD22-A108 T_A = 175°C, T_J = 190°C	1	504 hrs	116	
Pressure Cooker, Unbiased	JESD22-A102, Method C	3	96 hrs	77	
Storage Life	MIL-STD-883, Method 1008 T_A = 170°C	1	1200 hrs	77	
Temperature Cycle	MIL-STD-883, Method 1010	3	1000 cycles	153	
ESD Human Body Model	MIL-STD-883, Method 3015	1	Pre/Post Reading	3 per test	Test to failure HBM ≥ 8 kV
ESD Machine Model		1	Pre/Post Reading	3 per test	Test to failure MM ≥ 700 V

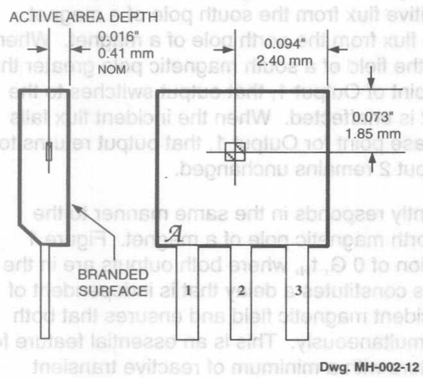
3197
PROTECTED, HIGH-TEMPERATURE, OPEN-COLLECTOR HALL-EFFECT LATCH

SENSOR LOCATIONS
(±0.005" [0.13 mm] die placement)

SUFFIX "LT"



SUFFIX "U"



APPLICATIONS INFORMATION

The A3197– latch has been optimized for use in automotive ring magnet sensing applications. Such applications include transmission speed sensors, motor position encoders, and wheel bearing speed sensors. Special care has been taken to optimize the operation of these devices in automotive subsystems that require ISO DP9637 protection but NOT operation. Undervoltage lockout is included to prevent propagation of false logic pulses during low battery, cold-start conditions. Noise suppression is included to prevent false switching of the device when subjected to ISO transients. Short-circuit protection is included to prevent damage caused by pinched wiring harnesses.

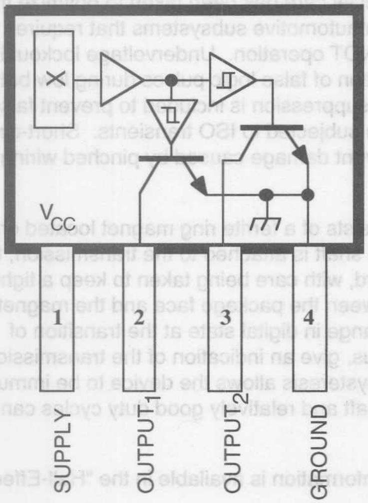
A typical application consists of a ferrite ring magnet located on a rotating shaft. Typically, this shaft is attached to the transmission, the sensor is mounted on a board, with care being taken to keep a tight tolerance on the air gap between the package face and the magnet. The device will provide a change in digital state at the transition of every magnetic pole and, thus, give an indication of the transmission speed. The high magnetic hysteresis allows the device to be immune to vibration of the magnet shaft and relatively good duty cycles can be obtained.

Hall effect applications information is available in the "Hall-Effect IC Applications Guide".

3235

27633A

DUAL-OUTPUT HALL-EFFECT SWITCH



Dwg. PH-007

Pinning is shown viewed from branded side.

Type UGN3235K Hall-effect sensors are bipolar integrated circuits designed for commutation of brushless dc motors, and other rotary encoding applications using multi-pole ring magnets. The device features two outputs which are independently activated by magnetic fields of opposite polarity.

Each sensor IC includes a Hall voltage generator, two Schmitt triggers, a voltage regulator, output transistors, and on-board reverse polarity protection. The regulator enables these devices to operate from voltages ranging between 4.5 V and 24 V. On-chip compensation circuitry stabilizes the switch points over temperature.

Each open-collector output is independently operated by the proper amount and polarity of incident magnetic flux. Output 1 responds only to the positive flux from the south pole of a magnet, Output 2 to the negative flux from the north pole of a magnet. When the sensor experiences the field of a south magnetic pole greater than the maximum operate point of Output 1, that output switches to the LOW state and Output 2 is unaffected. When the incident flux falls below the minimum release point for Output 1, that output returns to the HIGH state and Output 2 remains unchanged.

Output 2 independently responds in the same manner to the negative flux from the north magnetic pole of a magnet. Figure 1 shows a zone in the region of 0 G, t_H, where both outputs are in the HIGH or OFF state. This constitutes a delay that is independent of rate of change of the incident magnetic field and ensures that both outputs are never ON simultaneously. This is an essential feature for driving brushless dc motors with a minimum of reactive transient currents.

The UGN3235K is supplied in a four-pin plastic single in-line package (SIP) measuring just 0.205" wide x 0.135" high x 0.060" thick (5.2 x 3.4 x 1.55 mm).

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

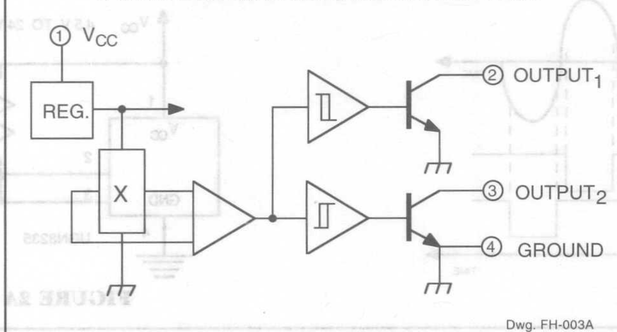
Power Supply, V_{CC}	**25 V**
Reverse Battery Voltage, V_{RCC}	**-30 V**
Magnetic Flux Density, B	**Unlimited**
Output OFF Voltage, V_{OUT}	**25 V**
Output ON Current, I_{OUT}	**50 mA**
Operating Temperature Range, T_A	**-20°C to + 85°C**
Storage Temperature Range T_S	**-65°C to +150°C**

FEATURES

- Reliable and Rugged Magnetic Sensing Switch
- Two Outputs Independently Switched by North and South Poles
- Independent Actuation of Outputs Minimizes Inductive-Load Reactive Transient
- Built-in Hysteresis Minimizes Interference from Stray Fields
- Operates from 4.5 V to 24 V
- Outputs Compatible with All Logic Levels
- On-Board Reverse Polarity Protection
- Open-Collector, Active-Low Outputs

Always order by complete part number: **UGN3235K**

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}		4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 24 V, I_{OUT} = 20 mA	—	160	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, V_{CC} = 24 V	—	—	1.0	µA
Supply Current	I_{CC}	V_{CC} = 24 V, Output Open	—	6.0	8.0	mA
Output Rise Time	t_r	V_{CC} = 14 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	0.4	µs
Output Fall Time	t_f	V_{CC} = 14 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	0.4	µs

MAGNETIC CHARACTERISTICS at V_{CC} = 4.5 V to 24 V

Characteristic	Test Conditions	Output	Min.	Max.	Units
Operate Point, B_{OP}	T_A = +25°C	Q1	50	175	G
		Q2	-175	-50	G
	T_A = -20°C to +85°C	Q1	35	200	G
		Q2	-200	-35	G
Release Point, B_{RP}	T_A = +25°C	Q1	25	160	G
		Q2	-160	-25	G
	T_A = -20°C to +85°C	Q1	15	190	G
		Q2	-190	-15	G
Hysteresis, B_{hys}	T_A = +25°C	Q1 & Q2	15	100	G
	T_A = -20°C to +85°C	Q1 & Q2	15	110	G

OUTPUT SWITCHING CHARACTERISTICS

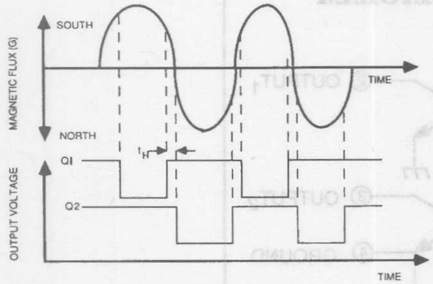


FIGURE 1

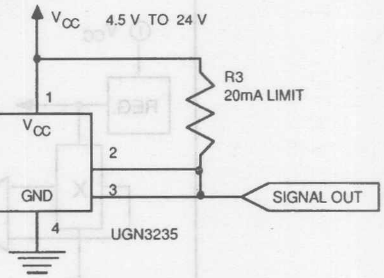


FIGURE 2A

MOTOR COIL DRIVER

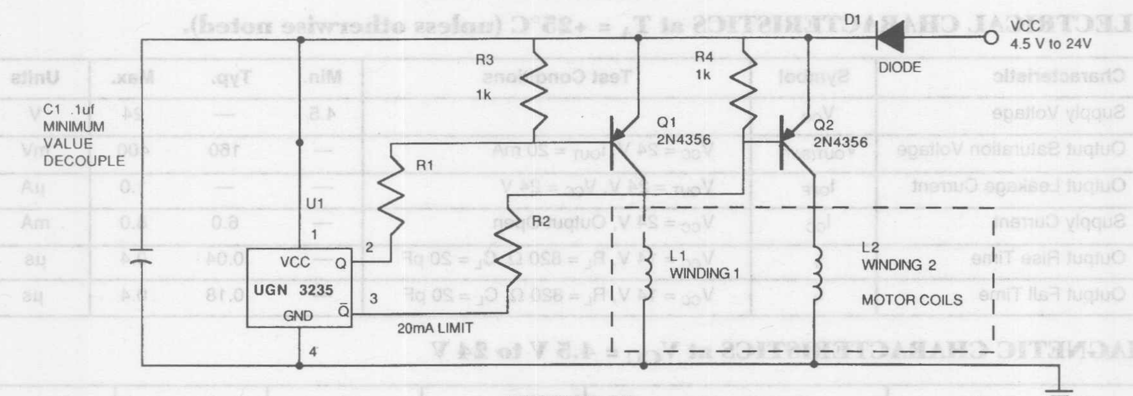
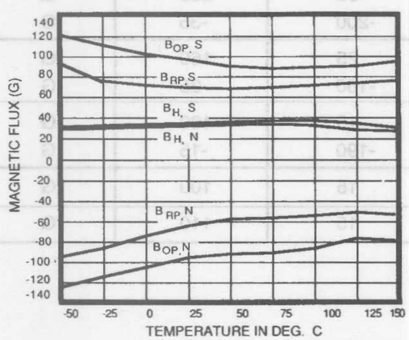


FIGURE 2B

SWITCH POINTS VERSUS TEMPERATURE

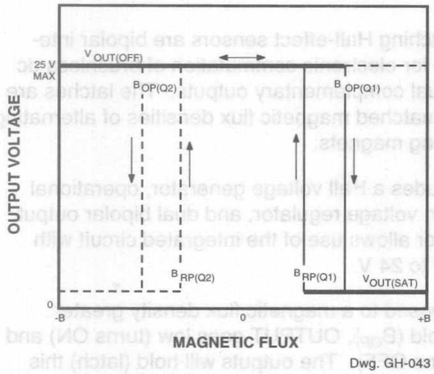


APPLICATIONS

Figure 2A gives a method of sensing the presence of either a north or south magnetic pole. Since the UGN3235K is an open collector device, it is possible to directly connect (OR-wire) the two outputs. This causes the output to go LOW when a north or south pole of sufficient magnitude is sensed.

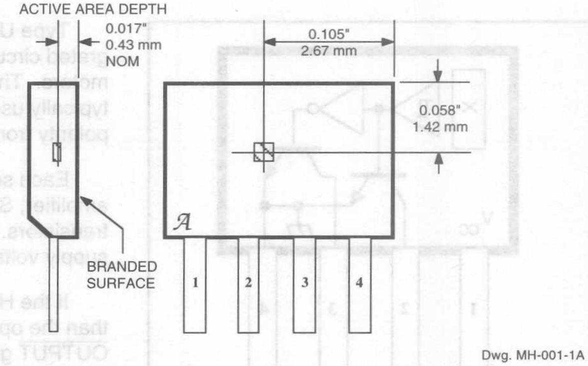
The device connected in this manner suits many applications, ranging from doubling the resolution of a ring-magnet encoder, to zero-crossing detection. Figure 1 shows that t_H is centered around the zero-G portion of the magnetic field plot. Thus, by decoding the HIGH portion of the UGN3235K OR-wired output, the zero-crossing can be encoded.

HYSTERESIS CHARACTERISTICS



Dwg. GH-043

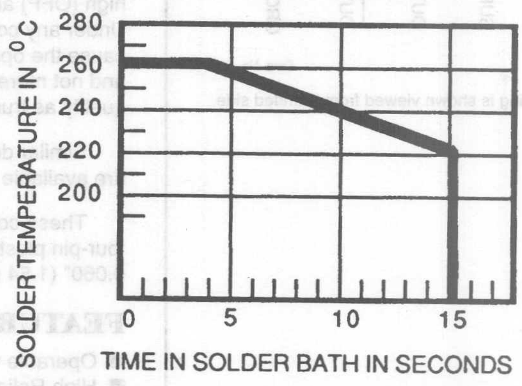
SENSOR LOCATION
(±0.005” [0.13mm] die placement)



Dwg. MH-001-1A

Figure 2B shows that the UGN3235K makes it possible to implement a very efficient brushless dc motor using a minimum number of components. Referring again to Fig. 1, the dead time (t_H) of the switching characteristics allow the motor coil fields to decay sufficiently. This avoids both excessive reactive voltages and the magnetic drag resulting from the motor coils working in opposition to each other.

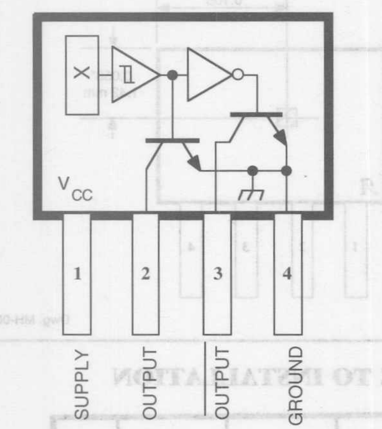
GUIDE TO INSTALLATION



Dwg. No. A-12.062

1. All Hall effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package. Use of epoxy glue is recommended. Other types may deform the epoxy package.
2. To prevent permanent damage to the Hall cell, heat-sink the leads during hand soldering. Recommended maximum conditions for wave soldering are shown in the graph above.

COMPLEMENTARY-OUTPUT HALL-EFFECT LATCH



Dwg. No. PH-002

Pinning is shown viewed from branded side.

Type UGN3275K latching Hall-effect sensors are bipolar integrated circuits designed for electronic commutation of brushless dc motors. They feature dual complementary outputs. The latches are typically used to sense matched magnetic flux densities of alternating polarity from multipole ring magnets.

Each sensor IC includes a Hall voltage generator, operational amplifier, Schmitt trigger, voltage regulator, and dual bipolar output transistors. The regulator allows use of the integrated circuit with supply voltages of 4.5 V to 24 V.

If the Hall cell is exposed to a magnetic flux density greater than the operate threshold (B_{OP}), OUTPUT goes low (turns ON) and $\overline{\text{OUTPUT}}$ goes high (turns OFF). The outputs will hold (latch) this state until magnetic field reversal exposes the Hall cell to a magnetic flux density below the release threshold (B_{RP}) when OUTPUT will go high (OFF) and $\overline{\text{OUTPUT}}$ will go low (ON). This state is also latched. Under any condition one output is ON while the other is OFF. Because the operating state switches only with magnetic field reversal, and not merely with a change in the strength, these integrated circuits qualify as true Hall-effect latches.

Similar devices, with a 500 mA continuous output current rating, are available as the UGN5275K.

These complementary-output Hall-effect latches are supplied in a four-pin plastic SIP, 0.200" (5.08 mm) wide, 0.130" (3.3 mm) high, and 0.060" (1.54 mm) thick.

FEATURES

- Operable with Multipole Ring Magnets
- High Reliability
- Small Size
- Output Compatible with All Digital Logic Families
- 4.5 V to 24 V Operation
- High Hysteresis Level Minimizes Stray-Field Problems
- Complementary Outputs

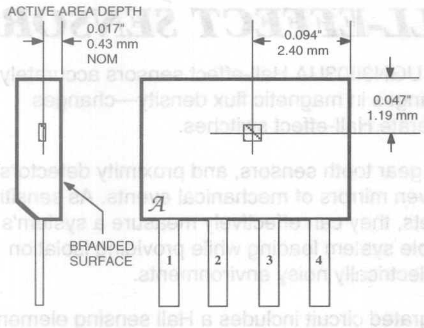
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . **25 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Output OFF Voltage, V_{OUT} . . . . **25 V**
Output ON Current, I_{OUT} . . . . **50 mA**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

Always order by complete part number: **UGN3275K**.

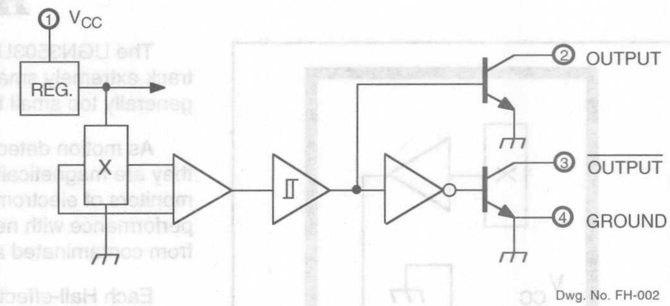
3275
COMPLEMENTARY OUTPUT HALL-EFFECT LATCH

SENSOR LOCATION



Dwg. No. MH-001-2

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FH-002

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating	4.5	—	24	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{CC} = 4.5 V, I_{OUT} = 20 mA, B > B_{OP}	—	—	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, V_{CC} = 24 V, B < B_{RP}	—	—	10	μA
Supply Current	I_{CC}	V_{CC} = 24 V, B < B_{RP}	—	—	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.04	0.4	μs
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	0.18	0.4	μs

MAGNETIC CHARACTERISTICS

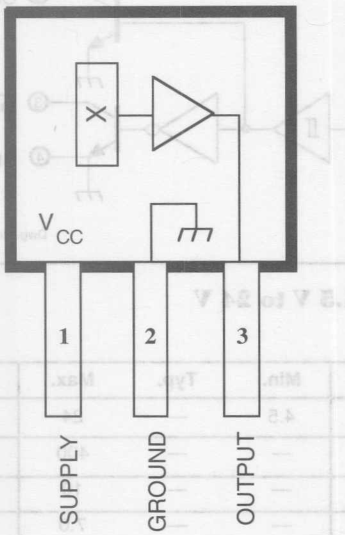
Characteristic	Symbol	T_A = +25°C		T_A = -20°C to +85°C		Units
		Min.	Max.	Min.	Max.	
Operate Point	B_{OP}	25	250	15	250	G
Release Point	B_{RP}	-250	-25	-250	-15	G
Hysteresis	B_{hys}	100	—	100	—	G

NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

3503

27501A*

RATIOMETRIC, LINEAR HALL-EFFECT SENSORS



Dwg. PH-006

Pinning is shown viewed from branded side.

The UGN3503U and UGN3503UA Hall-effect sensors accurately track extremely small changes in magnetic flux density—changes generally too small to operate Hall-effect switches.

As motion detectors, gear tooth sensors, and proximity detectors, they are magnetically driven mirrors of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while providing isolation from contaminated and electrically noisy environments.

Each Hall-effect integrated circuit includes a Hall sensing element, linear amplifier, and emitter-follower output stage. Problems associated with handling tiny analog signals are minimized by having the Hall cell and amplifier on a single chip.

The UGN3503U and UGN3503UA are rated for continuous operation over the temperature range of -20°C to +85°C.

FEATURES

- Extremely Sensitive
- Flat Response to 23 kHz
- Low-Noise Output
- 4.5 V to 6 V Operation
- Magnetically Optimized Package

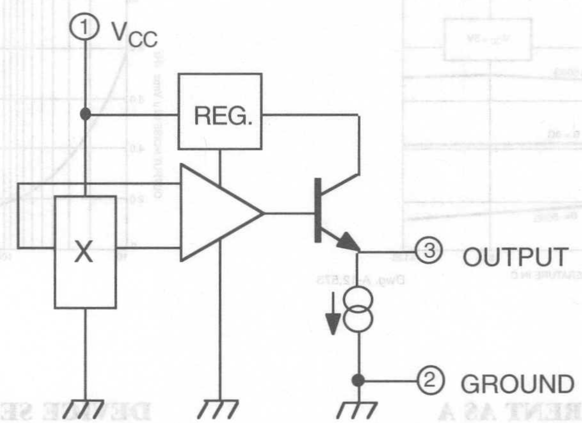
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... **8 V**
Magnetic Flux Density, B .... **Unlimited**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

Always order by complete part number:

Part Number	Package
UGN3503U	**3-Pin Mini-SIP**
UGN3503UA	**3-Pin Ultra-Mini-SIP**

FUNCTIONAL BLOCK DIAGRAM



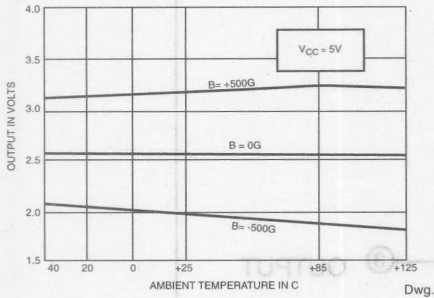
Dwg. FH-007

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 5 V

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage	V_{CC}		4.5	—	6.0	V
Supply Current	I_{CC}		—	9.0	14	mA
Quiescent Output Voltage	V_{OUT}	B = 0 G	2.25	2.50	2.75	V
Sensitivity	ΔV_{OUT}	B = 0 G to ±900 G	0.75	1.30	1.72	mV/G
Bandwidth (-3 dB)	BW		—	23	—	kHz
Broadband Output Noise	V_{out}	BW = 10 Hz to 10 kHz	—	90	—	µV
Output Resistance	R_{OUT}		—	50	—	Ω

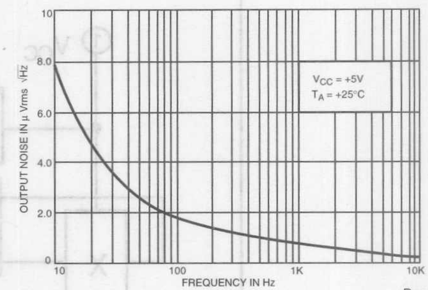
All output-voltage measurements are made with a voltmeter having an input impedance of at least 10 kΩ.
Magnetic flux density is measured at most sensitive area of device located 0.016" (0.41 mm) below the branded face of the 'U' package; 0.020" (0.51 mm) below the branded face of the 'UA' package.

OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE



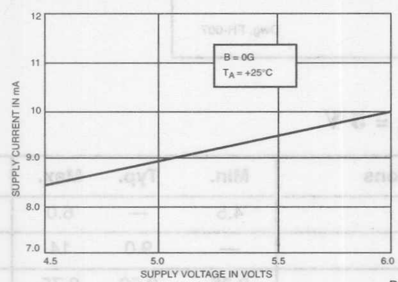
Dwg. A-12,573

OUTPUT NOISE AS A FUNCTION OF FREQUENCY



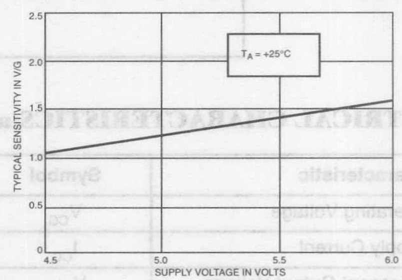
Dwg. A-12,505

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



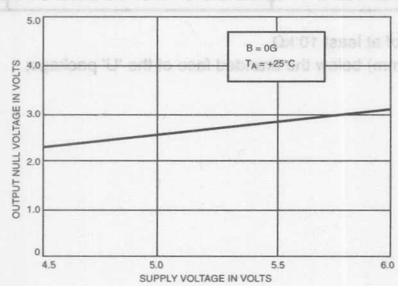
Dwg. A-12,506

DEVICE SENSITIVITY AS A FUNCTION OF SUPPLY VOLTAGE



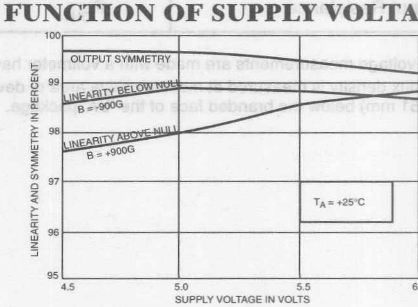
Dwg. A-12,507

OUTPUT NULL VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



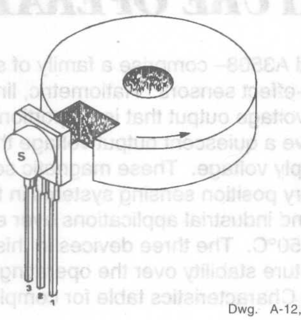
Dwg. A-12,508

LINEARITY AND SYMMETRY AS A FUNCTION OF SUPPLY VOLTAGE



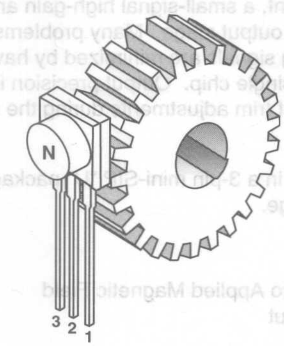
Dwg.A-12,509

NOTCH SENSOR



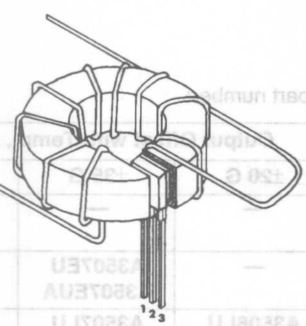
Dwg. A-12,574

GEAR TOOTH SENSOR



Dwg. A-12,512

CURRENT MONITOR



Dwg. A-12,513

OPERATION

The output null voltage (B = 0 G) is nominally one-half the supply voltage. A south magnetic pole, presented to the branded face of the Hall-effect sensor will drive the output higher than the null voltage level. A north magnetic pole will drive the output below the null level.

In operation, instantaneous and proportional output-voltage levels are dependent on magnetic flux density at the most sensitive area of the device. Greatest sensitivity is obtained with a supply voltage of 6 V, but at the cost of increased supply current and a slight loss of output symmetry. The sensor's output is usually capacitively coupled to an amplifier that boosts the output above the millivolt level.

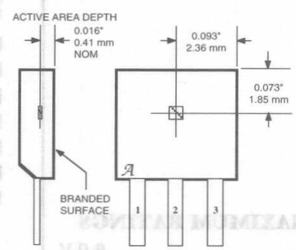
In two applications shown, a permanent bias magnet is attached with epoxy glue to the back of the epoxy package. The presence of ferrous material at the face of the package acts as a flux concentrator.

The south pole of a magnet is attached to the back of the package if the Hall-effect IC is to sense the presence of ferrous material. The north pole of a magnet is attached to the back surface if the integrated circuit is to sense the absence of ferrous matrial.

Calibrated linear Hall devices, which can be used to determine the actual flux density presented to the sensor in a particular application, are available.

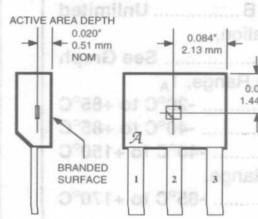
SENSOR LOCATIONS

SUFFIX "U"



Dwg. MH-002-5A

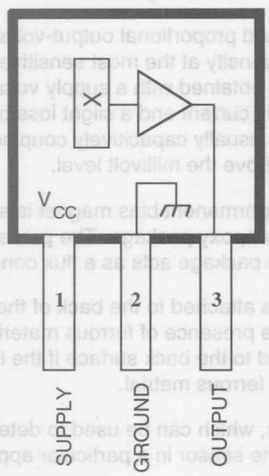
SUFFIX "UA"



Dwg. MH-011-3A

3506, 3507, AND 3508

RATIOMETRIC, LINEAR HALL-EFFECT SENSORS FOR HIGH-TEMPERATURE OPERATION



Dwg. PH-006

Pinning is shown viewed from branded side.

The A3506–, A3507–, and A3508– comprise a family of sensitive, temperature-stable linear Hall-effect sensors. Ratiometric, linear Hall-effect sensors provide a voltage output that is proportional to the applied magnetic field and have a quiescent output voltage that is approximately 50% of the supply voltage. These magnetic sensors are ideal for use in linear and rotary position sensing systems in the harsh environments of automotive and industrial applications over extended temperatures to -40°C and +150°C. The three devices in this series are similar except for temperature stability over the operating temperature range. See the Magnetic Characteristics table for complete, individual device parametrics.

Each monolithic circuit integrates a quadratic Hall element, improved temperature compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, and a rail-to-rail low-impedance output stage. Many problems normally associated with low-level analog signals are minimized by having the Hall element and amplifier in a single chip. Output precision is obtained by internal gain and offset trim adjustments during the manufacturing process.

These devices are supplied in a 3-pin mini-SIP “U” package or a 3-pin ultra-mini-SIP “UA” package.

FEATURES

- Output Voltage Proportional to Applied Magnetic Field
- Ratiometric Rail-to-Rail Output
- Improved Sensitivity
- Superior Temperature Stability
- 4.5 V to 5.5 V Operation
- Small Package Size
- Solid-State Reliability

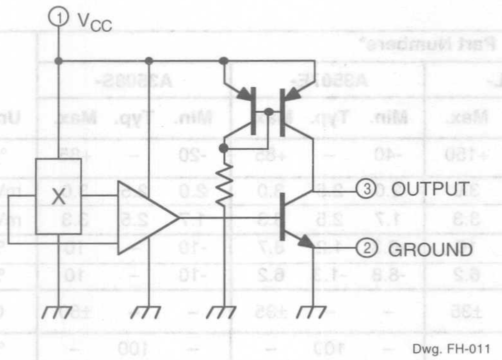
ABSOLUTE MAXIMUM RATINGS

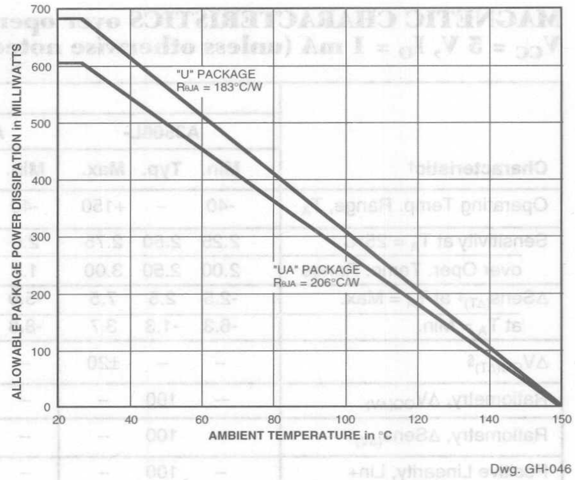
Supply Voltage, V_{CC} .... **6.0 V**
Output Voltage, V_O .... **6.0 V**
Output Sink Current, I_O .... **5.0 mA**
Magnetic Flux Density, B .... **Unlimited**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range, T_A
Suffix S– .... **-20°C to +85°C**
Suffix E– .... **-40°C to +85°C**
Suffix L– .... **-40°C to +150°C**
Storage Temperature Range,
T_S .... **-65°C to +170°C**

Always order by complete part number:

Operating Temperature Range	Output Offset with Temp., $\Delta V_{OQ(\Delta T)}$		
	±20 G	±35 G	±50 G
-20°C to +85°C	—	—	A3508SU A3508SUA
-40°C to +85°C	—	A3507EU A3507EUA	—
-40°C to +150°C	A3506LU A3506LUA	A3507LU A3507LUA	—

FUNCTIONAL BLOCK DIAGRAM





ELECTRICAL CHARACTERISTICS over operating temperature range, at V_{CC} = 5 V (unless otherwise noted).

Characteristic	Symbol	Device Type*	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage	V_{CC}	All	Operating	4.5	5.0	5.5	V
Supply Current	I_{CC}	All	B = 0, V_{CC} = 5.5 V, I_O = 0	–	–	10	mA
Quiescent Voltage Output	V_{OQ}	3506	B = 0, I_O = 1 mA, T_A = 25°C	2.25	2.50	2.75	V
		3507/08		2.0	2.5	3.0	V
		3506	B = 0, I_O = 1 mA	2.10	2.50	2.90	V
		3507/08		1.8	2.5	3.2	V
Output Voltage	V_{OH}	All	B = +X†, I_O = 1 mA	4.5	4.8	–	V
	V_{OL}	All	B = -X†, I_O = -1 mA	–	0.2	0.5	V
Bandwidth (-3 dB)	BW	All		20	–	–	kHz
Output Resistance	r_O	All		–	2.5	10	Ω
Wide-Band Output Noise	e_o	All	B = 0, BW = 10 Hz to 10 kHz, T_A = 25°C	–	125	–	µV

Negative current is defined as coming out of (sourcing) the output.

* Complete part number includes the Allegro prefix "A", and a suffix to identify operating temperature range (S–, E–, or L–) and package type (–U or –UA). See first page for available combinations.

† This test requires positive and negative fields sufficient to swing the output driver between fully OFF and saturated (ON), respectively. It is NOT intended to indicate a range of linear operation.

3506, 3507, AND 3508 RATIOMETRIC, LINEAR HALL-EFFECT SENSORS FOR HIGH-TEMPERATURE OPERATION

MAGNETIC CHARACTERISTICS over operating temperature range, at V_{CC} = 5 V, I_O = 1 mA (unless otherwise noted).

	Part Numbers*												
	A3506L-			A3507L-			A3507E-			A3508S-			
Characteristic†	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Operating Temp. Range, T_A	-40	–	+150	-40	–	+150	-40	–	+85	-20	–	+85	°C
Sensitivity at T_A = 25°C	2.25	2.50	2.75	2.0	2.5	3.0	2.0	2.5	3.0	2.0	2.5	3.0	mV/G
over Oper. Temp. Range	2.00	2.50	3.00	1.7	2.5	3.3	1.7	2.5	3.3	1.7	2.5	3.3	mV/G
$\Delta Sens_{(\Delta T)}$‡ at T_A = Max.	-2.5	2.5	7.5	-5.0	2.5	10	-6.3	1.2	8.7	-10	–	10	%
at T_A = Min.	-6.3	-1.3	3.7	-8.8	-1.3	6.2	-8.8	-1.3	6.2	-10	–	10	%
$\Delta V_{OQ(\Delta T)}$§	–	–	±20	–	–	±35	–	–	±35	–	–	±50	G
Ratiometry, $\Delta V_{OQ(\Delta V)}$	–	100	–	–	100	–	–	100	–	–	100	–	%
Ratiometry, $\Delta Sens_{(\Delta V)}$	–	100	–	–	100	–	–	100	–	–	100	–	%
Positive Linearity, Lin+	–	100	–	–	100	–	–	100	–	–	100	–	%
Negative Linearity, Lin–	–	100	–	–	100	–	–	100	–	–	100	–	%
Symmetry	–	100	–	–	100	–	–	100	–	–	100	–	%

Magnetic flux density is measured at most sensitive area of device located 0.017" (0.43 mm) below the branded face of the "U" package; 0.020" (0.51 mm) below the branded face of the "UA" package.

* Complete part number includes a suffix to indicate package type (–U or –UA).

† See Characteristics Definitions for test conditions.

‡ The nominal sensitivity temperature stability is designed to compensate for the temperature coefficient of samarium-cobalt magnets (-0.02%/°C).

§ This calculation (formula 1 below) yields the device's equivalent accuracy, over the operating temperature range, in gauss.

CHARACTERISTICS DEFINITIONS

Quiescent Voltage Output. In the quiescent state (no magnetic field), the output is ideally equal to one-half of the supply voltage over the operating voltage and temperature range ($V_{OQ} \approx V_{CC}/2$). Due to internal component tolerances and thermal considerations, there is a tolerance on the quiescent voltage output and on the quiescent voltage output as a function of supply voltage and ambient temperature. For purposes of specification, the quiescent voltage output as a function of temperature is defined as

$$\Delta V_{OQ(\Delta T)} = \frac{V_{OQ(TA)} - V_{OQ(25°C)}}{Sens_{(25°C)}} \qquad (1)$$

This calculation yields the device's equivalent accuracy, over the operating temperature range, in gauss.

Sensitivity. The presence of a south-pole magnetic field perpendicular to the package face (the branded surface) will increase the output voltage from its quiescent value toward the supply voltage rail by an amount proportional to the magnetic field applied. Conversely, the application of a north pole will decrease the output voltage from its quiescent value. This proportionality is specified as the sensitivity of the device and is defined as

$$Sens = \frac{V_{O(500G)} - V_{O(-500G)}}{1000\ G} \qquad (2)$$

CHARACTERISTICS DEFINITIONS (concluded)

The stability of sensitivity as a function of temperature is defined as

$$\Delta Sens_{(\Delta T)} = \frac{Sens_{(TA)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad (3)$$

Ratiometry. The A3506–, A3507–, and A3508– feature a ratiometric output. The quiescent voltage output and sensitivity are proportional to the supply voltage (ratiometric).

The percentage ratiometric change in the quiescent voltage output is defined as

$$\Delta V_{OQ(\Delta V)} = \frac{V_{OQ(VCC)} / V_{OQ(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (4)$$

and the percentage ratiometric change in sensitivity is defined as

$$\Delta Sens_{(\Delta V)} = \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V} \times 100\% \quad (5)$$

Linearity and Symmetry. The on-chip output stage is designed to provide a linear output to within 500 mV of either rail with a supply voltage of 5 V. This is equivalent to approximately ±800 gauss of ambient field. Although application of stronger magnetic fields will not damage these devices, it will force the output into a non-linear region.

Linearity in per cent is measured and defined as

$$Lin+ = \frac{V_{O(500G)} - V_{OQ}}{2\ (V_{O(250G)} - V_{OQ})} \times 100\% \quad (6)$$

$$Lin- = \frac{V_{O(-500G)} - V_{OQ}}{2\ (V_{O(-250G)} - V_{OQ})} \times 100\% \quad (7)$$

and output symmetry as

$$Sym = \frac{V_{O(500G)} - V_{OQ}}{V_{OQ} - V_{O(-500G)}} \times 100\% \quad (8)$$

APPLICATIONS INFORMATION

Calibrated linear Hall devices, which can be used to determine the actual flux density presented to the sensor in a particular application, are available.

For safe, reliable operation, the output should not be pulled above the supply voltage or pulled below the device ground.

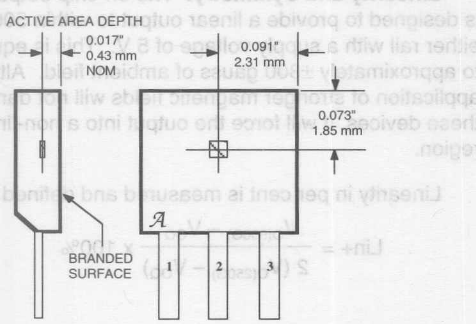
For optimum performance, a 100 pF capacitor between the output and ground should be added.

The nominal sensitivity is factory set to compensate for the temperature coefficient of samarium-cobalt magnets (-0.02%/°C).

The ratiometric feature is especially valuable when these devices are used with an analog-to-digital converter. A/D converters typically derive their LSB step size by ratioing off a reference voltage line. If the reference voltage varies, the LSB will vary proportionally. This is a major error source in many sensing systems. The A3506/07/08– can eliminate this source of error by their ratiometric operation. Because their gain and offsets are proportional to the supply voltage, if they are powered from the A/D reference voltage, the sensor output voltage will track changes in the LSB value.

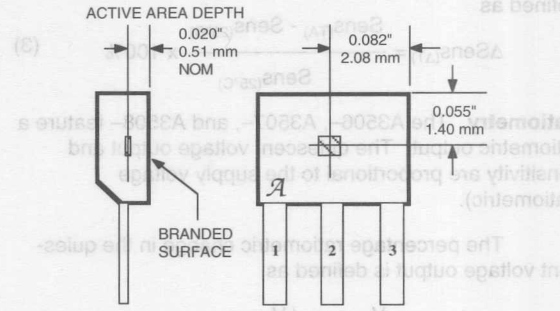
SENSOR LOCATIONS

SUFFIX "U"



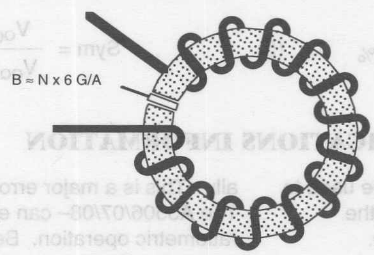
Dwg. MH-002-11

SUFFIX "UA"



Dwg. MH-011-6

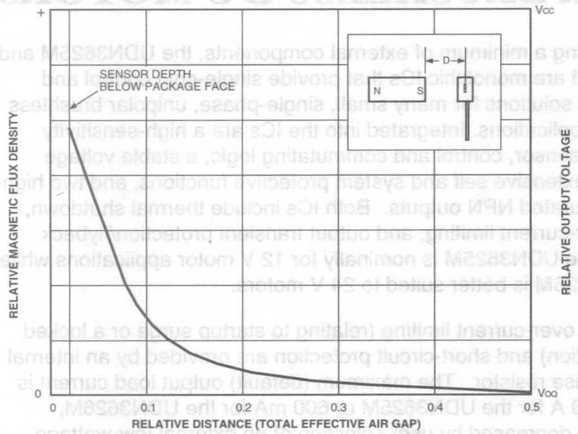
TYPICAL CURRENT-SENSING APPLICATION



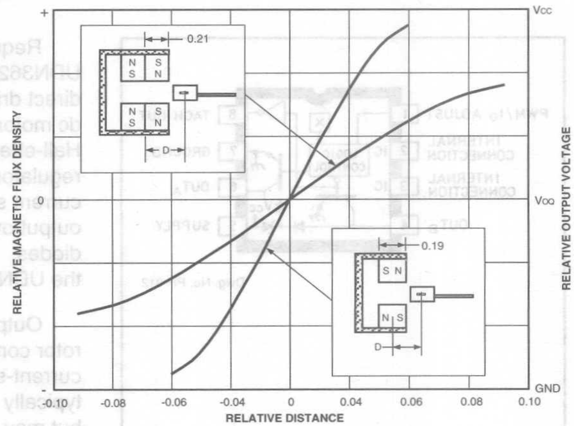
Dwg. AH-005

3506, 3507, AND 3508
RATIOMETRIC, LINEAR HALL-EFFECT SENSORS FOR HIGH-TEMPERATURE OPERATION

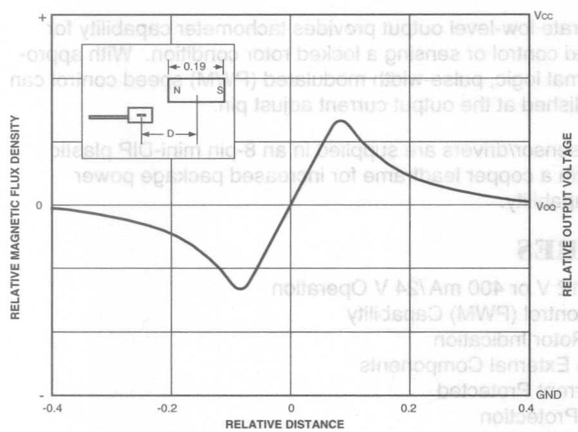
TYPICAL POSITION-SENSING APPLICATIONS
(Alnico 8, dimensions in inches)



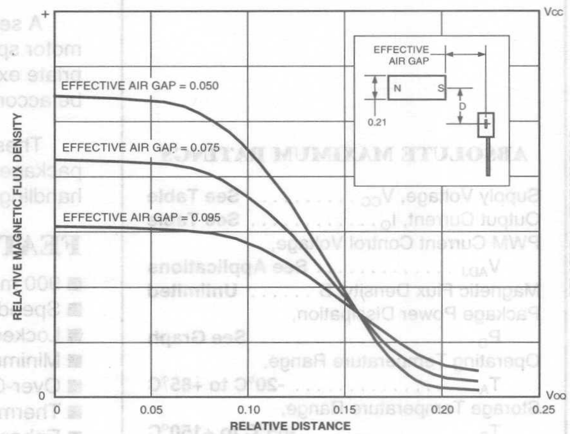
Dwg. GH-047



Dwg. GH-049



Dwg. GH-048

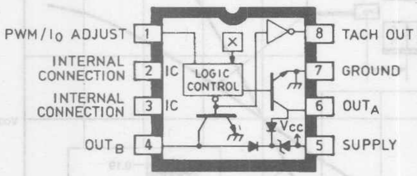


Dwg. GH-050

3625 AND 3626

27690A

POWER HALL™ SENSOR/DRIVER FOR BRUSHLESS DC MOTORS



Dwg. No. PP-012

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... **See Table**
Output Current, I_O .... **See Table**
PWM Current Control Voltage,
V_{ADJ} .... **See Applications**
Magnetic Flux Density, B ...... **Unlimited**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

	UDN3625M	UDN3626M
$V_{CC(MAX)}$	14 V	26 V
$I_{O(CONT)}$	1.0 A	0.45 A
$I_{O(PEAK)}$	1.6 A	0.75 A

Output current rating will be limited by ambient temperature, supply voltage, and duty cycle. Under any set of conditions, do not exceed a junction temperature of +150°C.

Requiring a minimum of external components, the UDN3625M and UDN3626M are monolithic ICs that provide single-chip control and direct drive solutions for many small, single-phase, unipolar brushless dc motor applications. Integrated into the ICs are a high-sensitivity Hall-effect sensor, control and commutating logic, a stable voltage regulator, extensive self and system protective functions, and two high-current saturated NPN outputs. Both ICs include thermal shutdown, output over-current limiting, and output transient protection/flyback diodes. The UDN3625M is nominally for 12 V motor applications while the UDN3626M is better suited to 24 V motors.

Output over-current limiting (relating to startup surge or a locked rotor condition) and short-circuit protection are provided by an internal current-sense resistor. The maximum (default) output load current is typically 1.3 A for the UDN3625M or 600 mA for the UDN3626M, but may be decreased by user selection of an external low-wattage resistor.

A separate low-level output provides tachometer capability for motor speed control or sensing a locked rotor condition. With appropriate external logic, pulse-width modulated (PWM) speed control can be accomplished at the output current adjust pin.

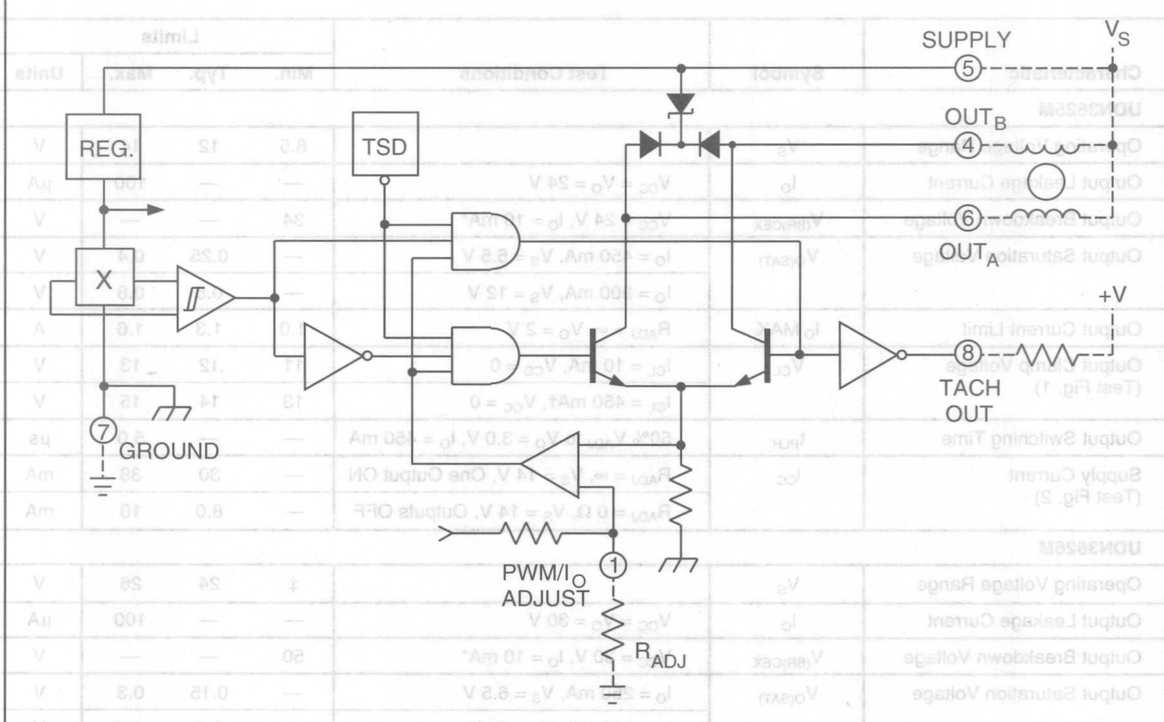
These sensor/drivers are supplied in an 8-pin mini-DIP plastic package with a copper leadframe for increased package power handling capability.

FEATURES

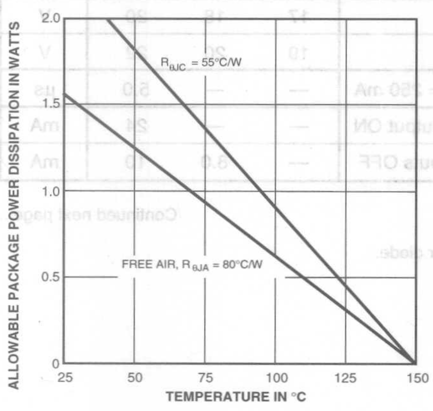
- 900 mA/12 V or 400 mA/24 V Operation
- Speed-Control (PWM) Capability
- Locked-Rotor Indication
- Minimum External Components
- Over-Current Protected
- Thermal Protection
- Enhanced Reliability
- Reduced Cost

Always order by complete part number, e.g., **UDN3625M** .
See Maximum Ratings at left.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FP-005-1



Dwg. No. GP-009-1B

TRUTH TABLE

Mag. Field	PWM/I$_O$ADJ	OUT$_A$	OUT$_B$
> +B$_{OP}$	Open	Low	High
> -B$_{OP}$	Open	High	Low
Any	<0.3 V	High	High

ELECTRICAL CHARACTERISTICS at T_A = +25°C, R_{ADJ} = ∞, Over Operating Voltage Range (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
UDN3625M						
Operating Voltage Range	V_S		6.5	12	14	V
Output Leakage Current	I_O	$V_{CC} = V_O = 24$ V	—	—	100	µA
Output Breakdown Voltage	$V_{(BR)CEX}$	$V_{CC} = 24$ V, $I_O = 10$ mA*	34	—	—	V
Output Saturation Voltage	$V_{O(SAT)}$	$I_O = 450$ mA, $V_S = 6.5$ V	—	0.25	0.4	V
		$I_O = 900$ mA, $V_S = 12$ V	—	0.5	0.8	V
Output Current Limit	I_O MAX	$R_{ADJ} = \infty$, $V_O = 2$ V	1.0	1.3	1.6	A
Output Clamp Voltage (Test Fig. 1)	V_{CL}	$I_{CL} = 10$ mA, $V_{CC} = 0$	11	12	13	V
		$I_{CL} = 450$ mA†, $V_{CC} = 0$	13	14	15	V
Output Switching Time	t_{PLH}	50% V_{ADJ} to $V_O = 3.0$ V, $I_O = 450$ mA	—	—	5.0	µs
Supply Current (Test Fig. 2)	I_{CC}	$R_{ADJ} = \infty$, $V_S = 14$ V, One Output ON	—	30	38	mA
		$R_{ADJ} = 0\ \Omega$, $V_S = 14$ V, Outputs OFF	—	8.0	10	mA
UDN3626M						
Operating Voltage Range	V_S		‡	24	26	V
Output Leakage Current	I_O	$V_{CC} = V_O = 30$ V	—	—	100	µA
Output Breakdown Voltage	$V_{(BR)CEX}$	$V_{CC} = 30$ V, $I_O = 10$ mA*	50	—	—	V
Output Saturation Voltage	$V_{O(SAT)}$	$I_O = 250$ mA, $V_S = 6.5$ V	—	0.15	0.3	V
		$I_O = 400$ mA, $V_S = 24$ V	—	0.3	0.5	V
Output Current Limit	I_OMAX	$R_{ADJ} = \infty$, $V_O = 2$ V	450	600	750	mA
Output Clamp Voltage (Test Fig. 1)	V_{CL}	$I_{CL} = 10$ mA, $V_{CC} = 0$	17	18	20	V
		$I_{CL} = 250$ mA†, $V_{CC} = 0$	19	20	22	V
Output Switching Time	t_{PLH}	50% V_{ADJ} to $V_O = 3.0$ V, $I_O = 250$ mA	—	—	5.0	µs
Supply Current (Test Fig. 2)	I_{CC}	$R_{ADJ} = \infty$, $V_S = 26$ V, One Output ON	—	—	24	mA
		$R_{ADJ} = 0\ \Omega$, $V_S = 26$ V, Outputs OFF	—	8.0	10	mA

* I_O is almost entirely Zener clamp current.
† Pulse test.
‡ Dependent on value of external series Zener diode (see Applications), 6.5 V without a Zener diode.

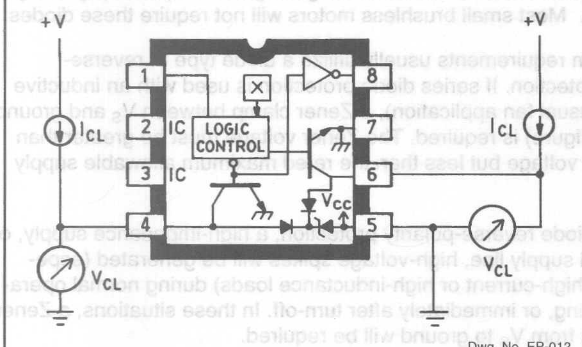
Continued next page...

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Both						
Operate Point§	B_{OP}		—	±100	±150	G
Hysteresis	B_H		—	200	—	G
Output Current Limit Ratio	I_O/I_O MAX	R_{ADJ} = 39 kΩ	—	0.75	—	—
		R_{ADJ} = 17 kΩ	—	0.50	—	—
		R_{ADJ} = 10 kΩ	—	0.25	—	—
PWM Control Current	I_{ADJ}	V_{ADJ} = 0	—	-350	-500	μA
Tach Output Leak. Current	I_T	V_T = 14 V	—	—	10	μA
Tach Output Sat. Voltage	$V_{T(SAT)}$	I_T = 750 μA	—	0.2	0.4	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	ΔT_J		—	10	—	°C

§ Magnetic flux density is measured at most sensitive area of device, nominally located 0.055" (1.40 mm) below the top of the package.

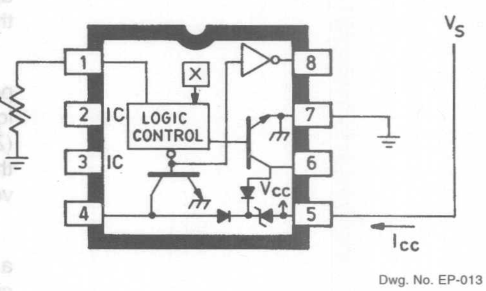
OUTPUT CLAMP VOLTAGE TEST
(ONE OUTPUT TESTED AT A TIME)



Dwg. No. EP-012

TEST FIG. 1

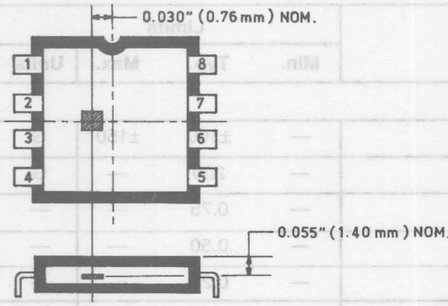
SUPPLY CURRENT TEST



Dwg. No. EP-013

TEST FIG. 2

SENSOR LOCATION



Dwg. No. MP-002

APPLICATIONS INFORMATION

Power Dissipation. Care should be taken in evaluating the package power dissipation of these devices. Total power dissipated by the device will consist of power due to the internal regulator, logic and drive circuitry (I_{CC} x V_{CC}), power due to the output drivers (I_O x $V_{O(SAT)}$), and power due to the clamp circuitry (I_{CL} x V_{CL} x duty cycle).

For example:

I_{CC} x V_{CC} = 38 mA (max) x 14 V = 532 mW (max)

I_O x $V_{O(SAT)}$ = 450 mA x 0.4 V (max) = 180 mW (max)

I_{CL} x V_{CL} x duty cycle = 450 mA x 15 V (max) x 1% = 67.5 mW (max)

Total package power dissipation = 779.5 mW (max)

Some of the power dissipated by the device (I_{CC} x V_{CC}) can be reduced by inserting a Zener diode in the supply line (Z_A in the figure). Note that the voltage at the V_{CC} pin under worst-case conditions must be greater than the minimum operating voltage (6.5 V).

Transient Protection. A note of caution concerns negative (below ground) excursions of the outputs. In application, the coupling of the two motor windings can provide for just such a case. Reducing the coupling between windings will help, but ground clamp diodes **or** diodes in series with the motor windings might be required (D_C **or** D_S in the figure). Most small brushless motors will not require these diodes.

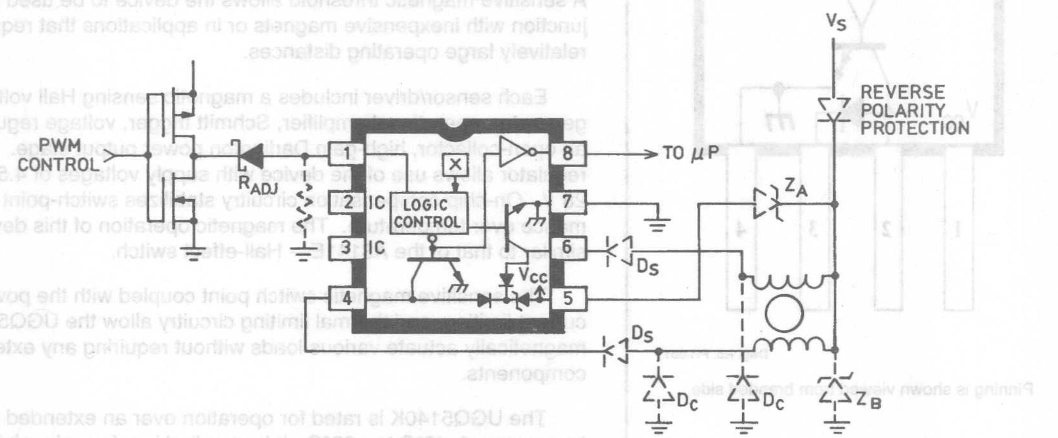
System requirements usually utilize a diode type of reverse-polarity protection. If series diode protection is used with an inductive load (the usual fan application), a Zener clamp between V_S and ground (Z_B in the figure) is required. The Zener voltage must be greater than the supply voltage but less than the rated maximum allowable supply voltage.

With diode reverse-polarity protection, a high-impedance supply, or a switched supply line, high-voltage spikes will be generated (especially with high-current or high-inductance loads) during normal operation, coasting, or immediately after turn-off. In these situations, a Zener clamp (Z_B) from V_S to ground will be required.

Over-Current Adjust Pin. The over-current limit may be reduced from the default value (I_O MAX) by selection of an external resistor (R_{ADJ}) at the PWM/I_O ADJ pin.

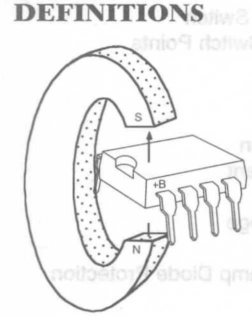
The external overcurrent adjust and the thermal shutdown are commoned at the PWM/I_O ADJ pin and tieing it to V_{CC} will disable the thermal shutdown. PWM current/speed control can be performed at the PWM/I_O ADJ pin from a standard totem-pole logic output with a series Schottky diode (1N5818,1N5819, or equivalent) or by pulling it low through an open-collector transistor (no pull-up resistor). PWM/I_O ADJ input voltages greater than 0.3 V are not recommended and may create an unstable operating condition.

TYPICAL FAN APPLICATION

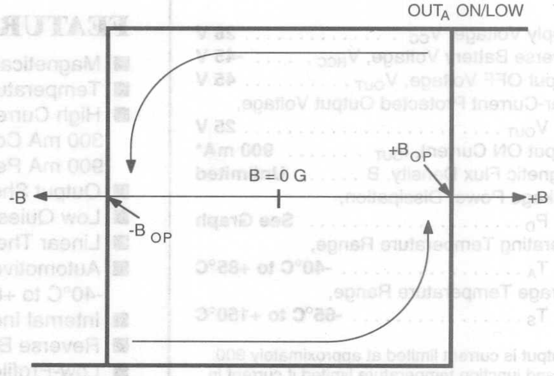


Dwg. No. EP-014

MAGNETIC FIELD DEFINITIONS



Dwg. No. AP-001-1



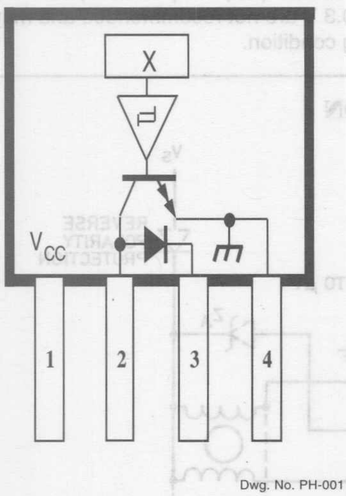
Dwg. No. GP-008

The north pole of a magnet is the north-seeking pole and is attracted to the earth's magnetic north pole.
By accepted magnetic convention, lines of flux emanate from the north-seeking pole of a magnet and enter the south-seeking pole.

5140

27695

PROTECTED POWERHALL® SENSOR — LAMP/SOLENOID DRIVER



Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . **28 V**
Reverse Battery Voltage, V_{RCC} . . . . . **-45 V**
Output OFF Voltage, V_{OUT} . . . . **45 V**
Over-Current Protected Output Voltage,
V_{OUT} . . . . **25 V**
Output ON Current, I_{OUT} . . . . **900 mA***
Magnetic Flux Density, B . . . . . . **Unlimited**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

* Output is current limited at approximately 900 mA and junction temperature limited if current in excess of 900 mA is attempted. See Circuit Description and Applications for further information.

The UGQ5140K unipolar Hall effect switch is a monolithic integrated circuit designed for magnetic actuation of low-power incandescent lamps or inductive loads such as relays or solenoids. Included on chip is a Darlington power output that is capable of continuously sinking in excess of 300 mA. Internal protection circuitry limits surge (lamp turn-ON) or fault currents to approximately 900 mA. A sensitive magnetic threshold allows the device to be used in conjunction with inexpensive magnets or in applications that require relatively large operating distances.

Each sensor/driver includes a magnetic sensing Hall voltage generator, operational amplifier, Schmitt trigger, voltage regulator, and an open-collector, high-gain Darlington power output stage. The regulator allows use of the device with supply voltages of 4.5 V to 28 V. On-chip compensation circuitry stabilizes switch-point performance over temperature. The magnetic operation of this device is similar to that of the A3141E— Hall-effect switch.

The sensitive magnetic switch point coupled with the power output, current limiting, and thermal limiting circuitry allow the UGQ5140K to magnetically actuate various loads without requiring any external components.

The UGQ5140K is rated for operation over an extended temperature range of -40°C to +85°C. It is supplied in a four-pin mini-SIP plastic package, 0.200" (5.08 mm) wide, 0.130" (3.30 mm) high, and 0.060" (1.54 mm) thick.

FEATURES

- Magnetically Actuated Power Switch
- Temperature-Compensated Switch Points
- High Current-Sink Capability
  300 mA Continuous
  900 mA Peak Current Limit
- Output Short-Circuit Protection
- Low Quiescent Standby Current
- Linear Thermal Limiting
- Automotive Temperature Range
  -40°C to +85°C, Operating
- Internal Inductive Flyback/Clamp Diode Protection
- Reverse Battery Protection
- Low-Profile 4-Pin Mini-SIP

Always order by complete part number: **UGQ5140K** .

ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted).

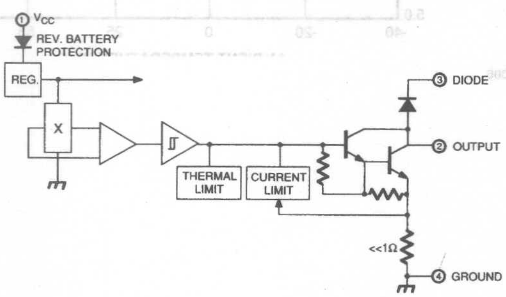
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	V_{CC}	Operating	4.5	12	24	V
Output Leakage Current	I_{OUT}	V_{OUT} = 24 V	—	<1.0	10	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 300 mA, V_{CC} = 24 V	—	0.84	1.2	V
Over-Current Limit	I_{LIMIT}	$V_{CC} = V_{OUT}$ = 12 V, B ≥ 500 G	—	900	—	mA
Output Rise Time	t_r	V_{CC} = 12 V, V_{BB} = 18 V,	—	0.04	2.0	µs
Output Fall Time	t_f	R_L = 1.1 kΩ, C_L = 20 pF	—	0.04	2.0	µs
Supply Current	I_{CC}	Output OFF	—	5.5	10	mA
Diode Forward Voltage	V_F	I_F = 300 mA	—	1.1	1.5	V
Diode Leakage Current	I_R	V_R = 35 V	—	<1.0	50	µA
Thermal Limit	T_{LIMIT}	$V_{CC} = V_{OUT}$ = 12 V, B ≥ 500 G, I_{OUT} = 10 mA	—	165	—	°C

Typical Data is at T_A = +25°C and is for design information only.

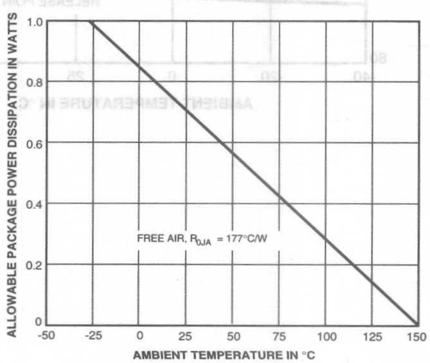
MAGNETIC CHARACTERISTICS at V_{CC} = 4.5 V to 24 V.

Characteristic	Symbol	T_A = +25°C Min.	T_A = +25°C Typ.	T_A = +25°C Max.	T_A = -40°C to +85°C Min.	T_A = -40°C to +85°C Typ.	T_A = -40°C to +85°C Max.	Units
Magnetic Operate Point	B_{OP}	70	155	200	45	—	240	G
Magnetic Release point	B_{RP}	50	100	180	25	—	220	G
Hysteresis	B_{hys}	20	55	—	20	—	—	G

FUNCTIONAL BLOCK DIAGRAM

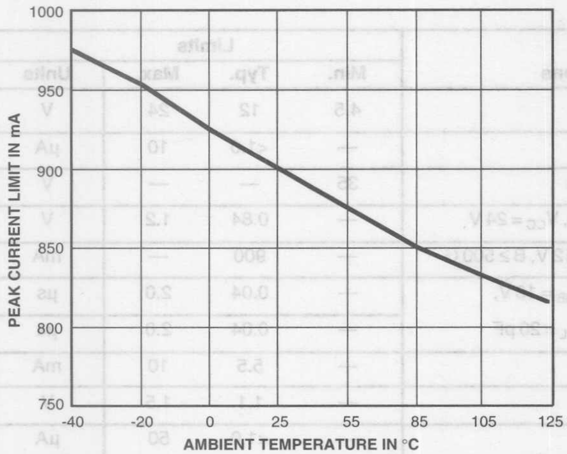


Dwg. No. FH-001

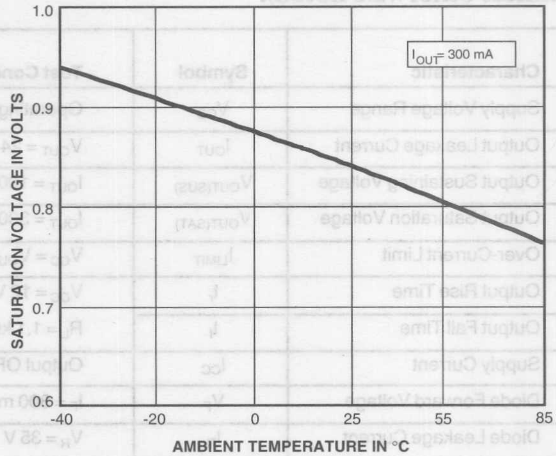


Dwg. No. GH-001

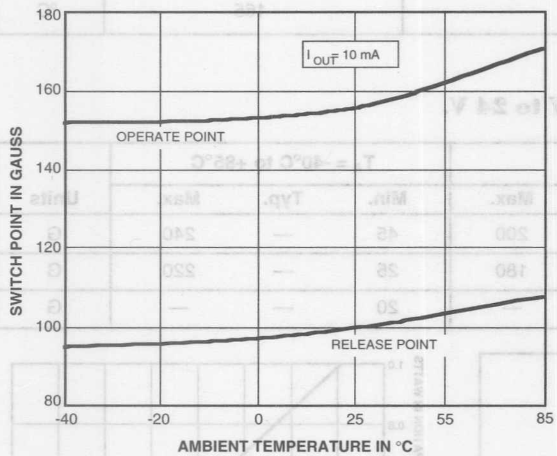
TYPICAL OPERATING CHARACTERISTICS



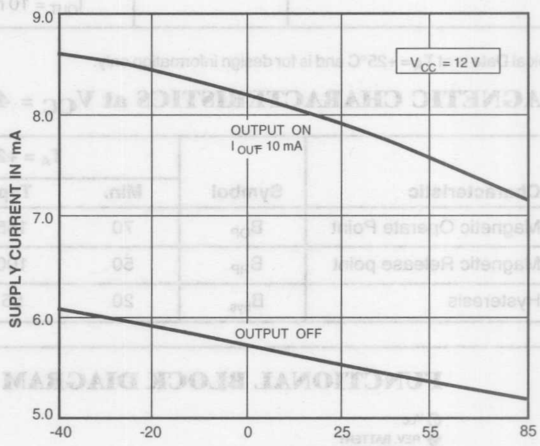
Dwg. No. GH-004



Dwg. No. GH-002

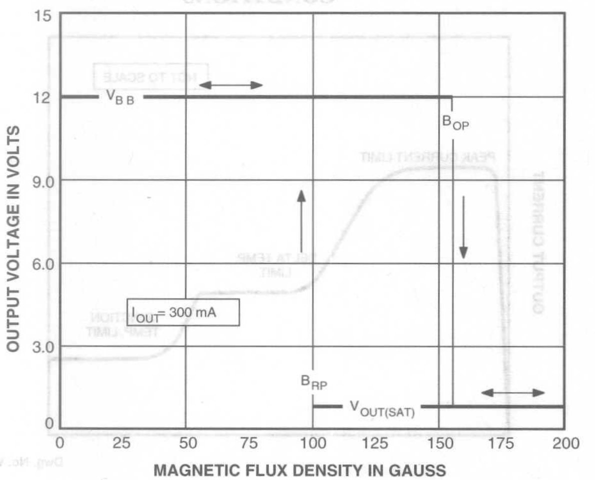


Dwg. No. GH-006



Dwg. No. GH-003

TYPICAL TRANSFER CHARACTERISTICS at T_A = +25°C



Dwg. No. GH-007

CIRCUIT DESCRIPTION AND OPERATION

The UGQ5140K merges state-of-the-art Hall effect sensing and power driving technologies to allow precision non-contact actuation of incandescent lamps or inductive loads. It is rated for operation over an extended temperature range as typically required in automotive applications.

MAGNETIC OPERATION

As shown in the Transfer Characteristics graph, the output of the device (pin 2) switches low when the magnetic field at the Hall sensor exceeds the operate point threshold (B_{OP}). At this point, the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced to below the release point threshold (B_{RP}), the device output goes high. The difference in the magnetic operate and release points is called the hysteresis (B_H) of the part. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

CURRENT AND THERMAL LIMITING

Output short circuits may be caused by faulty connectors, crimped wiring harnesses, or blown loads. In such cases, current and thermal limit circuitry will protect the output transistor against destruction.

Current through the output transistor is sensed with a low-value on-chip aluminum resistor. The voltage drop across this resistor is fed back to control the base drive of the output stage. This feedback prevents the output transistor from exceeding its maximum current density rating by limiting the output current to approximately 900 mA. It may also cause the output voltage to increase ($V_{OUT} = V_{BB}$ - [$I_{LIMIT} \times R_L$]). In this mode, the device will dissipate an increased amount of power ($P_D = V_{OUT} \times I_{LIMIT}$) and the output transistor will be thermally stressed.

This stress, unless protected against (as in the UGQ5140K), will cause the device junction temperature to rise until it fails catastrophically.

Thermal stress protection is provided in two manners; delta temperature protection, and junction temperature protection. Under worst-case conditions (see Figures 1 and 2), if the output is shorted to supply, the output transistor will heat up much faster than the rest of the integrated circuit. This condition could cause localized failure in the output transistor. To prevent damage, a delta temperature limiting scheme is used. If a large thermal gradient is sensed across the device, the output transistor base drive is reduced to lower the output current. This reduces the power (heat) generated by the output transistor.

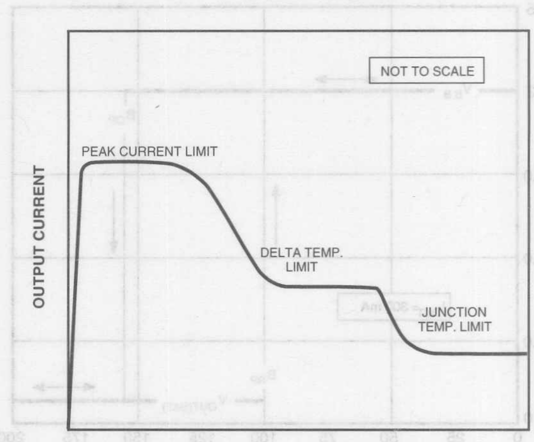
When thermal stresses cause the junction temperature to reach approximately +165°C, a linear thermal limiting circuit is activated. This circuit linearly reduces the base drive of the output transistor to maintain a constant junction temperature of 165°C. In this mode, the output current will be a function of the heat dissipating characteristics of the package and its environment. Linear thermal limiting eliminates the low-frequency thermal oscillation problems experienced by thermal shutdown (ON-OFF) schemes.

The output characteristics are shown in Figures 1 and 2. Note the three distinct operating regions: peak limit, delta limit, and thermal limit. In practice the output voltage and current may exhibit some oscillations during peak current limiting due to output load characteristics. These oscillations are of very-short duration (typically 50 ms) and may be damped with an external capacitor between pins 2 and 4.

When the fault condition that caused the output overload is corrected, the device returns to normal operating mode.

FIGURE 1

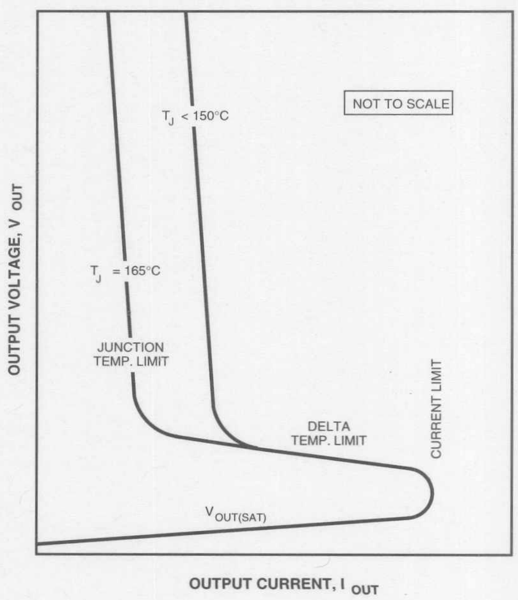
OUTPUT CURRENT UNDER SHORT-CIRCUIT CONDITIONS



Dwg. No. WH-002

FIGURE 2

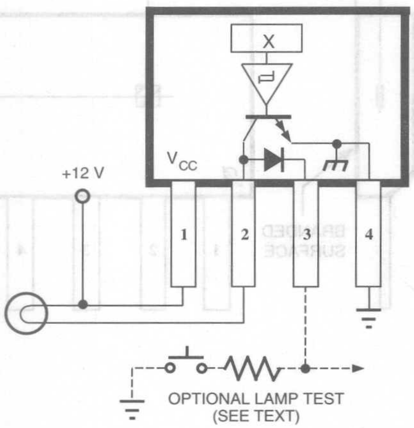
OUTPUT VOLTAGE vs OUTPUT CURRENT



Dwg. No. GP-013-1

FIGURE 3

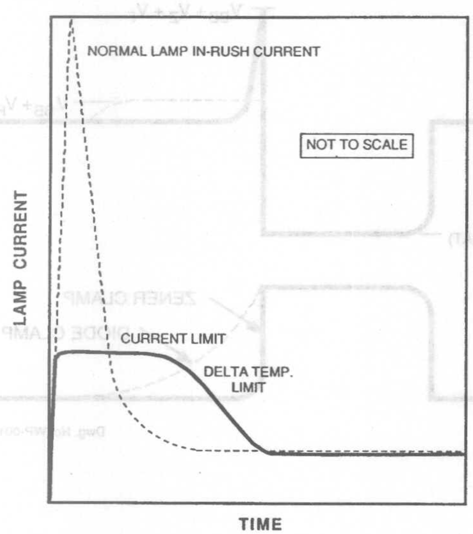
TYPICAL LAMP DRIVER APPLICATION



Dwg. No. EH-001

FIGURE 4

LAMP CURRENT vs TIME



Dwg. No. WH-001

TYPICAL APPLICATIONS

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON currents (commonly called in-rush currents) can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming resistors protect both driver and lamp but use significant power when the lamp is OFF while current-limiting resistors waste power when the lamp is ON. Lamps with steady-state current ratings to 300 mA can be driven by the UGQ5140K (Figure 3) without the need for warming or current limiting resistors. In applications using several sensor/drivers to control multiple lamps, the internal clamp diodes may be connected together to an appropriate current-limiting resistor and simple “lamp test” switch.

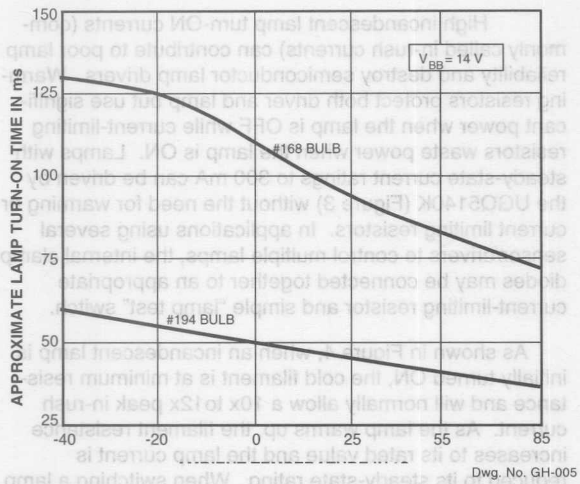
As shown in Figure 4, when an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and will normally allow a 10x to12x peak in-rush current. As the lamp warms up, the filament resistance increases to its rated value and the lamp current is reduced to its steady-state rating. When switching a lamp with the UGQ5140K, the internal current-limiting circuitry limits the peak current to approximately 900 mA. The device will stay in the current limit and delta temperature limit modes until the lamp resistance increases to its rated steady-state value (Figure 4). A side-effect of this current-limiting feature is that lamp turn-on times will increase. Typical lamp turn-on times are shown in Figure 5.

INDUCTIVE LOAD DRIVER

Connecting the internal clamp diode (pin 3) to the positive supply allows relays or other inductive loads to be driven directly, as shown in Figure 6. The internal diode prevents damage to the output transistor by clamping the high-voltage spikes which occur when turning OFF an inductive load. An optional external Zener diode can be used to increase the flyback voltage, providing a much faster inductive load turn-OFF current decay, resulting in faster dropout (reduced relay contact arcing), and improved performance. The maximum Zener voltage, plus the load supply voltage, plus the clamp diode forward voltage should not exceed 35 volts.

FIGURE 5

LAMP TURN-ON TIME



SENSOR LOCATION AREA

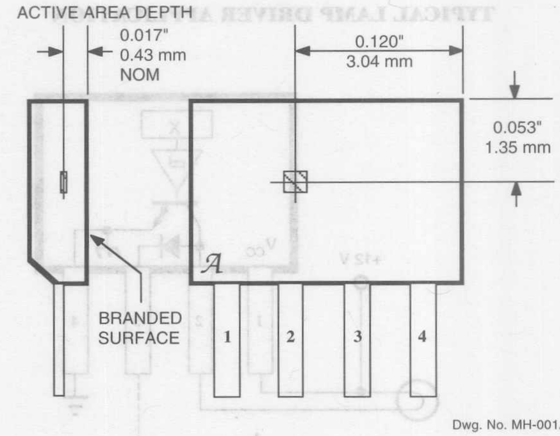
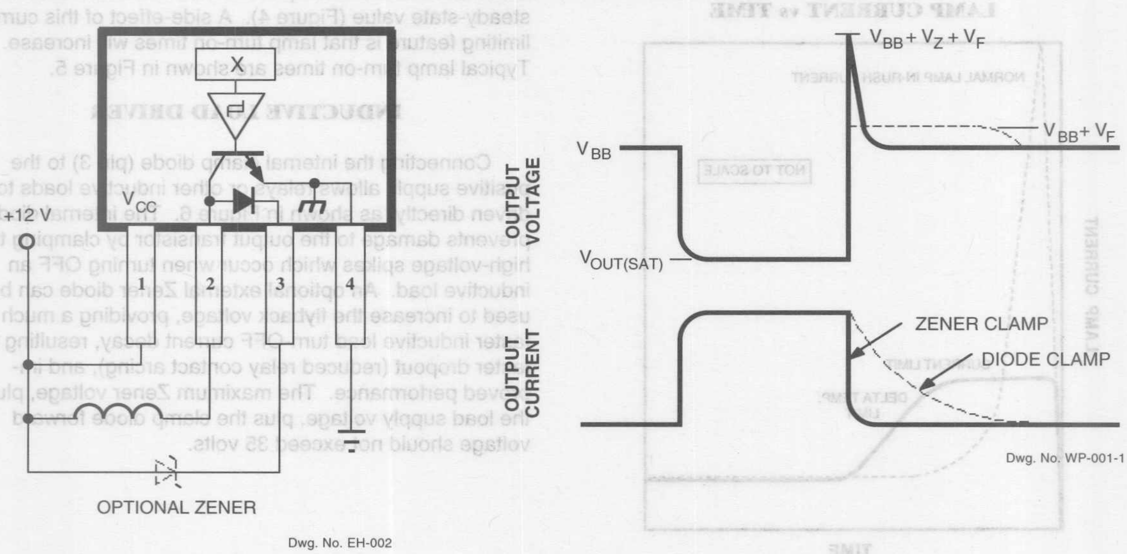


FIGURE 6

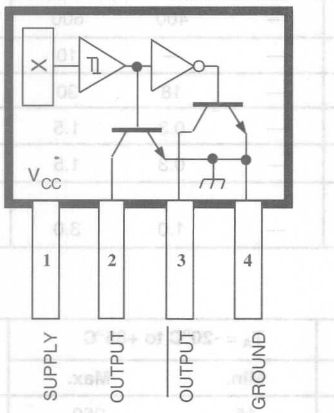
TYPICAL RELAY/SOLENOID DRIVER APPLICATION



5275

27632A

COMPLEMENTARY OUTPUT POWER HALL™ LATCH



Pinning is shown viewed from branded side.

Type UGN5275K latching Hall effect sensors are bipolar integrated circuits designed for electronic commutation of brushless dc motors. They feature open-collector complementary power outputs that are capable of sinking up to 300 mA continuously. Increased current ratings, complementary outputs, and sensitive switching points that are stable over temperature and time ideally suit these devices for minimum-component brushless dc motor designs.

Each sensor IC includes a Hall voltage generator, an operational amplifier, a Schmitt trigger, a voltage regulator, and large-area dual NPN output transistors. The regulator enables the IC to operate with supply voltages ranging from 4.5 V to 14 V. On-chip compensation circuitry stabilizes switch point performance over temperature. The large bipolar junction output transistors are fed by a unique driver stage which minimizes power dissipation within the IC. The magnetic operation of this device is similar to that of the UGN3275K complementary-output Hall effect latch.

Output Q of the IC switches to the LOW state when the internal Hall generator experiences a magnetic field that exceeds the rated operate point. Output $\overline{Q}$ switches HIGH within one µs of the Output Q change of state. When the device is exposed to a sufficient magnetic field of opposite polarity, Output Q returns to the HIGH state, and Output $\overline{Q}$ returns to the LOW state.

The UGN5275K is rated for operation over a temperature range of -20°C to +85°C, and is supplied in an environmentally rugged, four-pin miniature plastic SIP. Please consult the factory for alternate packaging and custom magnetic requirements.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} . . . . **14 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Output OFF Voltage, V_{CE} . . . . **60 V**
Output ON Current, I_C
  Continuous . . . . **0.5 A**
  Peak (Start Up) . . . . **0.9 A**
Operating Temperature Range,
  T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
  T_S . . . . **-65°C to +150°C**
Package Power Dissipation,
  P_D . . . . **750 mW**

FEATURES

- High Sink-Current Capability
- Magnetic Sensing, Complementary-Output Latch
- On-Chip Schmitt Trigger Provides Hysteresis
- Temperature-Compensated Switch Points
- Rugged, Low-Profile SIP

Always order by complete part number: **UGN5275K** .

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 14 V (unless otherwise noted).

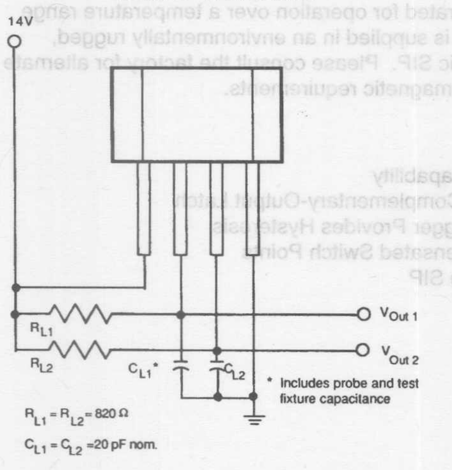
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}		4.5	—	14	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{CC} = 14 V, I_C = 300 mA	—	400	600	mV
Output Leakage Current	I_{CEX}	V_{CE} = 14 V, V_{CC} = 14 V	—	—	10	µA
Supply Current	I_{CC}	V_{CC} = 14 V, Output Open	—	18	30	mA
Output Rise Time	t_r	V_{CC} = 14 V, R_L = 45 Ω, C_L = 20 pF	—	0.3	1.5	µs
Output Fall Time	t_f	V_{CC} = 14 V, R_L = 45 Ω, C_L = 20 pF	—	0.3	1.5	µs
Switch Time Differential	Δt	V_{CC} = 14 V, R_L = 45 Ω, C_L = 20 pF	—	1.0	3.0	µs

MAGNETIC CHARACTERISTICS

Characteristic	Symbol	T_A = +25°C Min.	T_A = +25°C Max.	T_A = -20°C to +85°C Min.	T_A = -20°C to +85°C Max.	Units
Operate Point	B_{OP}	25	250	15	250	G
Release Point	B_{RP}	-250	-25	-250	-15	G
Hysteresis	B_{hys}	100	—	100	—	G

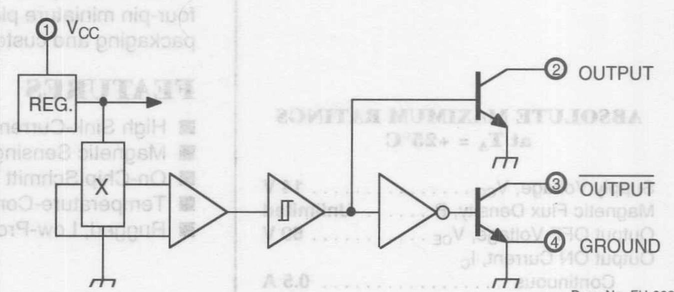
NOTE: As used here, negative flux densities are defined as less than zero (algebraic convention).

TEST CIRCUIT



Dwg. No. 1-14,408A

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. FH-002

MOTOR COIL DRIVER

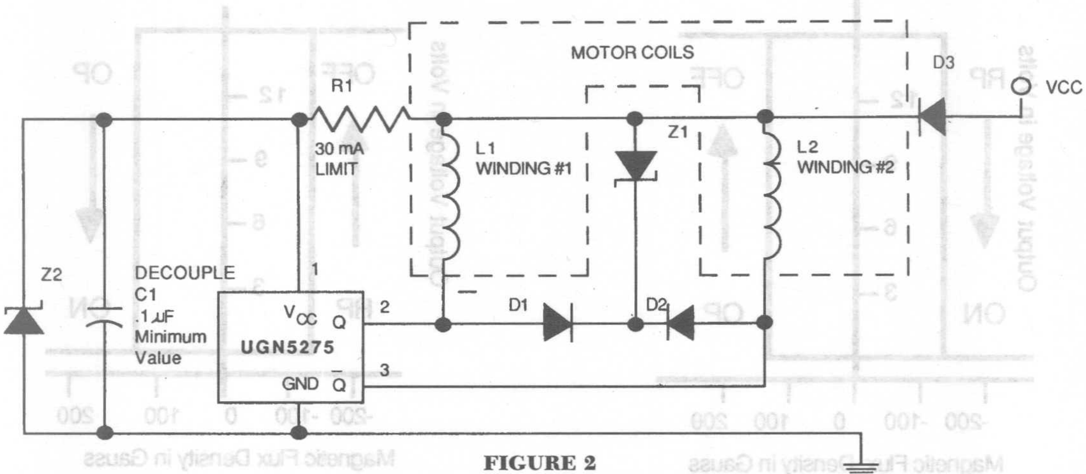
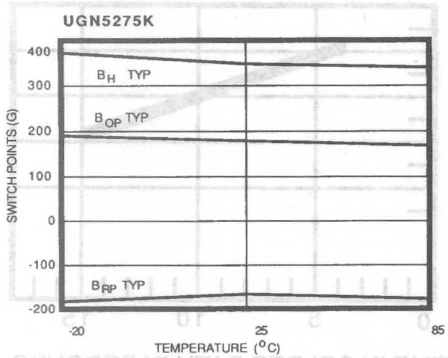


FIGURE 2

SWITCH POINTS VERSUS TEMPERATURE



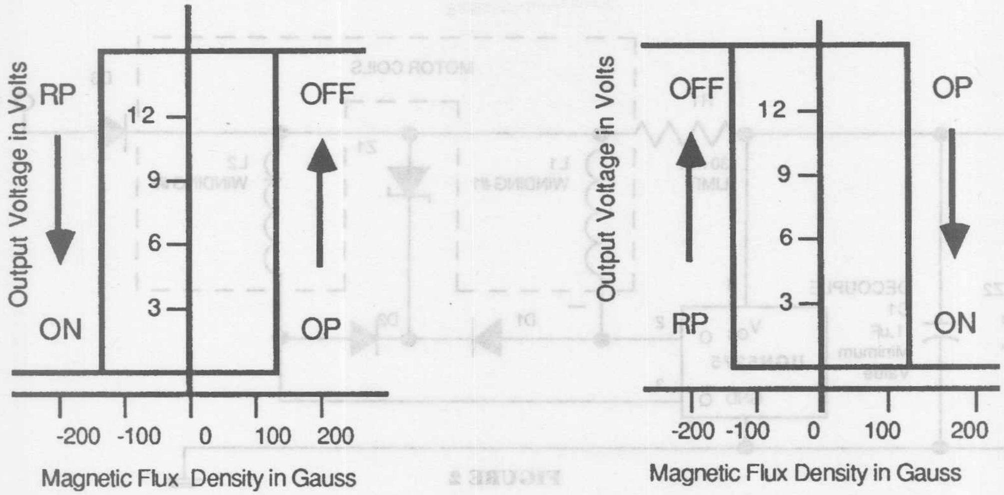
APPLICATIONS

The increased current sinking capability of the UGN5275K ideally suits it for building small, inexpensive brushless dc motors using a minimum number of external components. Figure 2 shows that the only components required to commutate motor windings L1 and L2 are the Hall effect IC, flyback diodes D1 and D2, and one decoupling capacitor. The remaining components are optional for improving motor performance. Care should be taken to ensure that the motor winding impedances are high enough to guarantee that start-up surge currents do not exceed the maximum rating of the Hall effect IC.

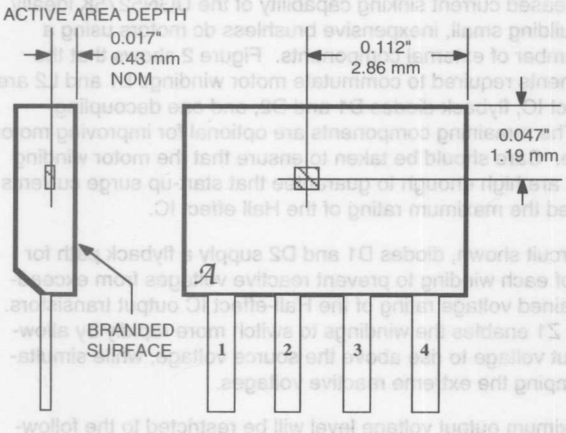
In the circuit shown, diodes D1 and D2 supply a flyback path for the current of each winding to prevent reactive voltages from exceeding the sustained voltage rating of the Hall-effect IC output transistors. Zener diode Z1 enables the windings to switch more rapidly by allowing the output voltage to rise above the source voltage, while simultaneously clamping the extreme reactive voltages.

The maximum output voltage level will be restricted to the following: $V_{CC} - V_{D3} + V_Z + V_{D1}$ (blocking diode D3 voltage drop). Blocking diode D3 provides reverse input-polarity protection, and should be used only if reverse battery voltage is a possibility. Capacitor C1 decouples the Hall-effect IC from any high dv/dt transients injected onto the V_{CC} rail to prevent regulator latch-up within the device. Zener diode Z2 and resistor R1 are required for operation from a V_{CC} exceeding 14 V.

HYSTERESIS CHARACTERISTICS



SENSOR LOCATION



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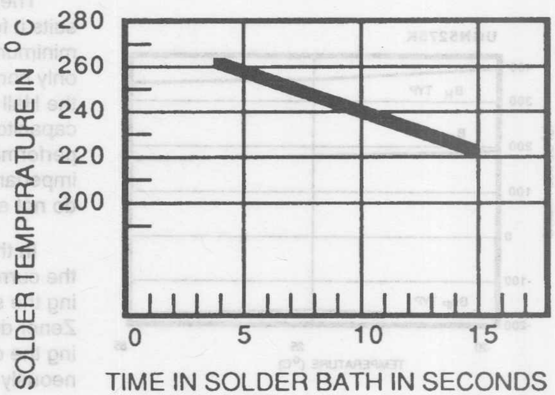
GUIDE TO INSTALLATION



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1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package. Use of epoxy glue is recommended. Other types may deform the epoxy package.

2. To prevent permanent damage to the Hall cell, heat-sink the leads during hand-soldering. Recommended maximum conditions for wave soldering are shown in the graph above.

THE HALL-EFFECT SENSOR

The basic Hall sensor is simply a small sheet of semiconductor material. A constant voltage source forces a constant bias current to flow in the semiconductor sheet. The output, a voltage measured across the width of the sheet, reads near zero if a magnetic field is not present (Figure 1).

If the biased Hall sensor is placed in a magnetic field oriented at right angles to the Hall current, the voltage output is in direct proportion to the strength of the magnetic field. This is the Hall effect, discovered by E. H. Hall in 1879 (Figure 2).

The basic Hall sensor is essentially a transducer that will respond with an output voltage if the applied magnetic field changes in any manner. Differences in the response of devices are generally related to tolerances and specifications, such as operate (turn on) and release (turn off) thresholds, as well as temperature range and temperature coefficients of these parameters. Also available are linear output sensors that differ in sensitivity or respond per gauss change.

A Hall sensor is activated by a magnetic field created by either electromagnets or permanent magnets. Magnetic fields have two important characteristics: magnitude and direction (or orientation). In the absence of any magnetic field, the most common Hall-effect digital switches are designed to be off (open circuit at output). They will turn on only if subjected to a magnetic field that has both sufficient strength and the correct polarity.

If the approach of the South pole of a magnet would cause switching action of a digital sensor, the approach of the North pole of a magnet would have no effect. In practice, a close approach by the South pole of a magnet will cause the output transistor to turn on.

The transfer characteristics graph (Figure 3) shows input vs output. The input variable, which is the strength of the activating magnetic field (magnetic flux density, measured in gauss), is plotted along the horizontal axis. The output variable, which is the digital (on, off) output from a Hall switch, is plotted along the vertical axis.

In the absence of any magnetic field (zero gauss), the Hall-effect switch is off and the output voltage equals the power supply (12 V). As the strength of the magnetic field increases, at some point (240 gauss in this case) the output transistor will turn on and the output voltage goes to zero. The output does not change even if the magnetic field's strength continues to increase.

The switch stays on until the magnetic field falls well below the 240 G operating point. This is a circuit design characteristic (hyster-

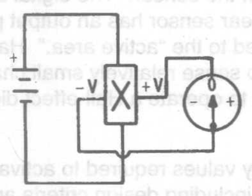


FIGURE 1

If no magnetic field is present, the voltage measured across the width of the semiconductor material of the Hall-effect sensor is zero.

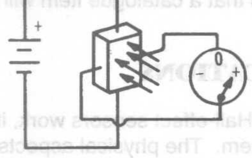


FIGURE 2

The output voltage of a Hall-effect sensor is directly proportional to the magnetic field present at right angles to the direction of current flow through the sensor.

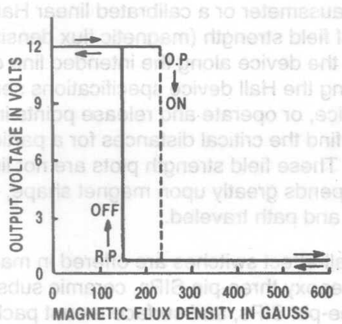


FIGURE 3

The transfer characteristic graph plots input on the horizontal axis vs output on the vertical axis. With no magnetic field present, the Hall-effect switch is off; as the field increases, the switch will turn on at a predesigned operating point. This particular device exhibits hysteresis of 90 gauss.

esis) that prevents oscillations. Our example uses a 90 gauss hysteresis (240-150), which will turn the device off at 150 gauss.

All switches turn on at or below their maximum operating point flux density, and when the magnetic field is reduced, all devices turn off before the flux density drops below their minimum release point value. Additionally, each device has a minimum amount (typically, 20 gauss) hysteresis to ensure clean switching action. This hysteresis ensures that even if mechanical vibration or electrical noise is present, the switch output is fast, clean, and occurs only once per threshold crossing.

FIGURES OF MERIT COMMONLY APPLIED TO MAGNETIC MATERIALS

- **Residual Induction (B_r) in Gauss.** How strong is the magnetic field? A magnet must have sufficient flux density to satisfy the Hall switch maximum operating point specification at the required air gap.
- **Coercive Force (H_c) in Oersteds.** How well will the magnet resist external demagnetizing forces? This property becomes important if the operating environment will subject the magnet to a strong demagnetizing field, such as might be encountered near the rotor of an A.C. motor. For such applications, a permanent magnet with this coercive force (ceramic, alnico-8, or, best of all, RE cobalt) is clearly indicated.
- **Maximum Energy Product [(B_d x H_d) Max x 10^6] in Gauss-Oersteds.** A strong magnet that is also very resistant to demagnetizing forces would have a high maximum energy product. Generally, the larger the energy product, the better, stronger, and more expensive the magnet.
- **Temperature Coefficient in Percent per Degree Celsius.** How much will the strength of the magnet change as the temperature changes?

Linear Hall-effect sensors differ from digital Hall-effect sensors with respect to the output response from the sensor. The digital sensor has an off/on or high/low output; the linear sensor has an output proportional to the magnetic field subjected to the "active area." Hall-effect linear sensors are used primarily to sense relatively small changes in magnetic fields, changes too small to operate a Hall-effect digital switch.

The exact magnetic flux density values required to activate Hall sensors differ for several reasons, including design criteria and manufacturing tolerances. Extremes in temperature also affect the response characteristics of the sensors.

For each device type, worst-case magnetic specifications can be set out for the user by a Hall-effect sensor marketing or applications engineer, if it has been determined that a catalogue item will not meet required tolerances.

APPLICATIONS

With an understanding of how Hall-effect sensors work, it is possible to build devices around them. The physical aspects of their characteristics form the basis of Hall device applications.

Analysis. The field created by a magnet must be compatible with the characteristics of the Hall-effect device it is expected to operate. Measure the strength of the magnetic field, which is greatest at the magnet's pole face, with a gaussmeter or a calibrated linear Hall sensor. Then plot a graph of field strength (magnetic flux density) vs distance of the magnet from the device along the intended line of travel of the magnet. Then, by using the Hall device specifications sensitivity of mV/gauss for a linear device, or operate and release points in gauss for a digital device) one can find the critical distances for a particular magnet and type of motion. These field strength plots are not linear, and the shape of the plot depends greatly upon magnet shape, magnetic circuit (concentrators), and path traveled.

Total Effective Air Gap. Hall-effect switches are offered in many different packages, such as epoxy three-pin SIPs, ceramic substrate mounted chips, ceramic three-pin SIPs, and surface mount packages. The most critical difference between packages is the distance from the face of the package to the surface of the Hall cell: the active area depth, which effectively adds to the total effective air gap.

The total effective air gap (TEAG) is the sum of the active area depth and the distance between the package surface and the magnet's surface. For Hall device applications, the TEAG should be as small as possible, consistent with the limitations of the activating mechanical

THE HALL-EFFECT SENSOR

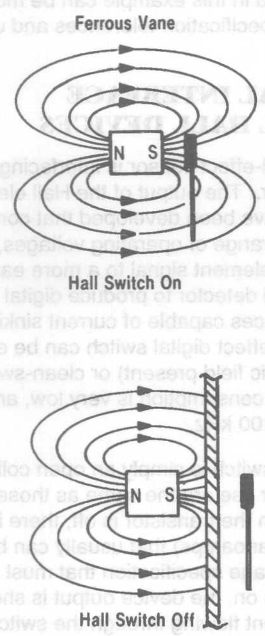


FIGURE 4

The ferromagnetic vane moves between the activating magnet and the Hall-effect switch shunting the flux field from the switch. These assemblies can be used for precision switching over large temperature ranges.

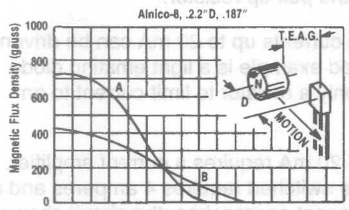


FIGURE 5

Hall devices must always switch on/off at the same point relative to the magnet. The effect of a change in flux density on switching distance is shown.

system. This will ensure that the magnetic flux will always be great enough to switch the device. Remember, magnetic flux decreases very sharply as the total effective air gap increases.

Modes of Operation. There are many ways to operate a Hall sensor. For example, with a simple bar or rod magnet there are two possible paths for the magnet to travel—head-on and slide-by. In the head-on mode, the magnetic pole moves along a perpendicular path straight at the active face of the Hall device. The head-on mode is simple, works well, and is relatively insensitive to lateral motion; however, if the mechanism moving the magnet overshoots the mark, the sensor package could be damaged.

A second possible path is to move the magnet in from the side of the hall device in the slide-by mode of operation. The slide-by mode is commonly used to avoid contact with the sensor package. The use of strong magnets or ferrous flux concentrators in well-designed slide-by magnetic circuits allows better sensing precision with a shorter travel path than the head-on mode.

Magnet manufacturers generally can provide head-on flux density curves for their magnets, but they often do not characterize magnets for slide-by operation, possibly because different air gap choices lead to an infinite number of these curves. Once a TEAG is chosen, however, the head-on magnet curves can be used to find the peak flux density (a single point) for slide-by applications by noting the value of magnetic flux at the chosen TEAG.

A third mode of operation keeps the Hall-effect sensor and magnet a fixed distance from one another and switches the sensor with a movable ferromagnetic vane. The Hall device and magnet can be molded together as a unit in a single rigid assembly, separated by an air gap. This eliminates alignment problems and produces an extremely rugged switching assembly.

The Hall device is held in the on state by the activating magnet. Placing the vane between the magnet and the Hall device (Figure 4) forms a magnetic shunt that distorts the flux field away from the Hall device. The vane can be made in many configurations to repeatedly sense position within ±0.002 in. over a 125°C temperature range.

The ferrous vane or vanes that interrupt the flux could have linear motion or rotational motion (as for a shaft encoder). Ferrous vane assemblies, due to the steep flux density/distance curves that can be achieved, are often used where precision switching over a large temperature range is required.

Steep Slopes and High Flux Densities. For linear Hall devices, greater flux changes for a given displacement give greater outputs, clearly an advantage because the voltage output of the sensor will be much greater, reducing the possibility of instruments picking up electrical noise. The same property is desirable for digital Hall

devices, but the reasons are more subtle. To achieve consistent switching action in a given application, the Hall device must always switch on and off at the same positions relative to the magnet.

Consider, for example, the flux density curves of the two different magnet configurations in Figure 5. With an operating point flux density of 200 gauss, a digital Hall-effect device would turn on at a distance of approximately 0.14 in. from either magnet. If manufacturing tolerance or temperature effects shifted the operating point of the sensor to 300 gauss, notice that in the curve for magnet "A" (steep slope) there is very little change in the distance at which switching occurs, while in the case of the curve of magnet "B", the change is considerable. The release point would be affected in much the same way.

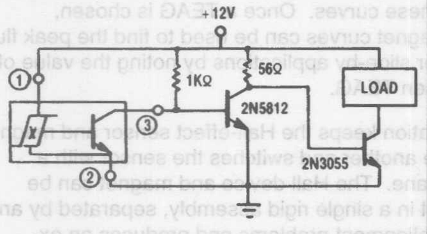


FIGURE 6

This circuit could be used if a load required a current of 4 A to switch.

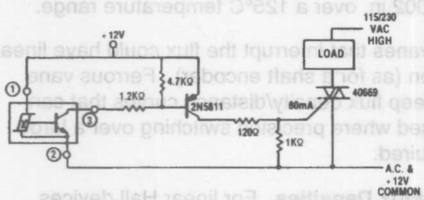


FIGURE 7

This circuit could be used to switch a 115 or 230 VAC load.

The basic principles illustrated in this example can be modified to include mechanism and device specification tolerances and used for worst-case design analysis.

ELECTRICAL INTERFACE FOR DIGITAL HALL DEVICES

A typical application for a Hall-effect sensor is interfacing the sensor signal to a microprocessor. The output of the Hall element is quite small; therefore, Hall ICs have been developed that contain a voltage regulator to allow a wide range of operating voltages, a high-quality DC amplifier to boost the element signal to a more easily used signal, a Schmitt trigger threshold detector to produce digital logic, and output stages for universal interfaces capable of current sinking or sourcing. The output of the Hall-effect digital switch can be either linear (proportional to the magnetic field present) or clean-switching (no bounce) digital logic. Energy consumption is very low, and frequency responses are well over 100 kHz.

The output stage of a digital switch is simply an open collector npn transistor switch, and the rules for use are the same as those for any similar switching transistor. When the transistor is off, there is a small leakage current (typically a few nanoamps) that usually can be ignored and a maximum (breakdown) voltage specification that must not be exceeded. When the transistor is on, the device output is shorted to the circuit common, and the current flowing through the switch must be externally limited to less than the maximum specified value to prevent damage (usually 20 mA).

Hall devices switch very rapidly; typical rise and fall times are in the 400 nano-second range. This is rarely significant, since switching times are almost universally controlled by the much slower mechanical parts of the device.

Interfacing with digital logic integrated circuits usually requires only an appropriate power supply and pull-up resistor.

Loads that require sinking currents up to 20 mA can be driven directly by a Hall switch. A good example is a light emitting diode (LED) indicator that requires only a resistor to limit current to an appropriate value.

Sinking more current than 20 mA requires a current amplifier. For example, if a certain load to be switched requires 4 amperes and must turn on when the activating magnet approaches, the circuit shown in Figure 6 could be used. To turn on a 115 or 230 VAC load, consider Figure 7. Note, however, that the +12 V supply common is connected to the low side of the AC line, and in the event of a mixup, the Hall switch and associated low voltage circuitry would be 115 volts above ground.

Due to the magnetic field around any current-carrying conductor, Hall-effect devices can be used to measure and limit current by converting this magnetic field to an electrical signal. The sensor response ranges from DC to the kHz range, and the conductor need not be interrupted. In low current applications, the magnetic field about a conductor is not normally intense enough to operate a Hall-effect digital switch; therefore, it would be best to use a toroid or closed magnetic circuit to increase the flux density.

Hall-effect linear sensors are used primarily to sense relatively small changes in magnetic fields—changes that are too small to operate a Hall-effect switching device. They are customarily capacitively coupled to an amplifier that boosts the output to a higher level (Figure 7).

As motion detectors, gear tooth sensors, and proximity detectors, linear Hall-effect sensors produce an electrical output that is a magnetically driven mirror of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while producing isolation from contaminated and electrically noisy environments.

Hall-effect sensors, both digital and linear, are used in the commutation of brushless DC motors, speed sensors, shaft encoders, current limiters and monitors, position sensors, and gear tooth sensors. Recent technology breakthroughs in Hall-effect devices have made available sensors for temperature ranges as high as 170°C. These sensors have been integrated into a vast array of innovative high-technology applications where reliability, efficiency, and cost competitiveness are a must.

MAGNETIC MATERIALS MOST COMMONLY USED

- **Rare Earth—Cobalt.** An alloy of rare earth metal, such as samarium, with cobalt (abbreviated RE cobalt). These magnets are the best in all categories but are also the most expensive. Too hard for machining, these magnets must be ground, if shaping is necessary. Maximum energy product, perhaps the best single measure of magnet quality, is approximately 16 x 10^6.
- **Alnico.** A class of alloys containing aluminum, nickel, cobalt, iron, and additives, which can be varied to give a wide range of properties. The magnets are strong and fairly expensive, but less so than RE cobalt. Alnico magnets can be cast or sintered by pressing metal powders into a die and heating. Sintered alnico is well suited to mass production of small, intricately shaped magnets, has a more uniform flux density, and is mechanically superior, but cast alnico magnets are generally magnetically stronger. The nonoriented or isotropic alnico alloys (alnico-1, alnico-2, alnico-3, alnico-4) are less expensive and magnetically weaker than the oriented alloys (alnico-5, alnico-6...alnico-9). Alnico is too hard and brittle to be shaped except by grinding. Maximum energy products range from 1.3 to 10 x10^6
- **Ceramic.** These magnets contain barium or strontium (or another element from that group) ferrite in a matrix of ceramic material that is compacted and sintered. They are poor conductors of heat and electricity, chemically inert, and have high values of coercive force. As with alnico, ceramic magnets can be fabricated with partial or complete orientation for additional magnetic strength. Less expensive than alnico, they are also too hard and brittle to shape except by grinding. Maximum energy products range from 1 to 1.3 x 10^6.
- **Cunife.** A ductile copper base alloy with nickel and iron, cunife can be stamped, swaged, drawn, or rolled into final stage. Maximum energy product is approximately 1.4 x 10^6.
- **Iron-Chromium.** These magnets have magnetic properties similar to alnico-5 but are soft enough to undergo machining operations before the final aging treatment hardens them. Maximum energy product is approximately 5.25 x 10^6.
- **Plastic and Rubber.** These magnets consist of barium and strontium ferrite in a plastic matrix material. They are very inexpensive and can be formed in numerous ways, including stamping, molding, and machining, depending on the particular matrix material. Since synthetic rubber is a plastic, the distinction between the two materials is not very precise. If a plastic magnet is flexible like rubber, it is generally called a rubber magnet. Maximum energy products range from 0.2 to 1.2 x 10^6.

HALL-EFFECT IC APPLICATIONS GUIDE

Allegro Microsystems uses the latest bipolar integrated circuit technology in combination with the century-old Hall effect to produce Hall effect ICs. These are contactless, magnetically activated switches and sensors with the potential to simplify and improve systems.

LOW-COST SIMPLIFIED SWITCHING

Simplified switching is a Hall sensor's strong point. Hall effect IC switches combine Hall voltage generators, signal amplifiers, Schmitt trigger circuits, and transistor output circuits on single integrated circuit chips. Output is clean, fast, and switched without bounce—an inherent problem with mechanical contact switches. A Hall effect switch typically operates at up to a 100 kHz repetition rate, and costs less than many common electromechanical switches.

EFFICIENT, EFFECTIVE, LOW-COST LINEAR SENSORS

The linear Hall effect sensor detects the motion, position, or change in field strength of an electromagnet, a permanent magnet, or a ferromagnetic material with an applied magnetic bias. Energy consumption is very low. The output is linear and temperature-stable. The sensor's frequency response is flat up to approximately 25 kHz.

A Hall effect sensor is more efficient and effective than inductive or optoelectronic sensors, and at a lower cost.

SENSITIVE CIRCUITS FOR RUGGED SERVICE

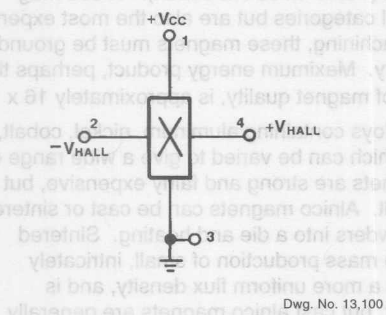
The Hall effect sensor is virtually immune to environmental contaminants and is suitable for use under severe service conditions. The circuit is very sensitive and provides reliable, repetitive operation in close tolerance applications. The Hall effect sensor can see precisely through dirt and darkness.

CURRENT APPLICATIONS

Current applications for Hall effect ICs include use in ignition systems, speed controls, security systems, alignment controls, micrometers, mechanical limit switches, computers, printers, disk drives, keyboards, machine tools, key-switches, and pushbutton switches. They are also used as tachometer pickups, current limit switches, position detectors, selector switches, current sensors, linear potentiometers and brushless dc motor commutators.

THE HALL EFFECT SENSOR: HOW DOES IT WORK?

The basic Hall sensor is a small sheet of semiconductor material represented by Figure 1.



FIGURE

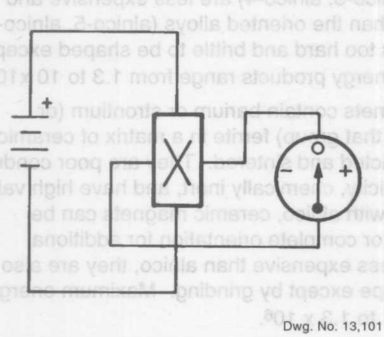


FIGURE 2

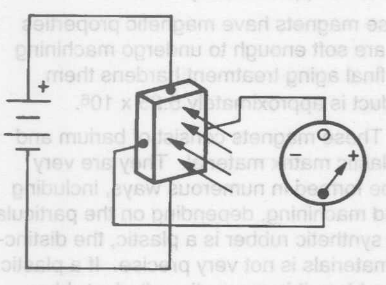


FIGURE 3

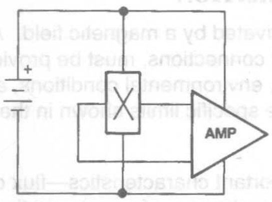


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FIGURE 4

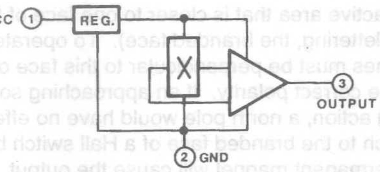

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FIGURE 5

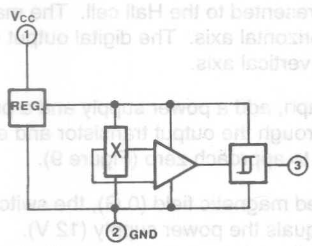

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FIGURE 6

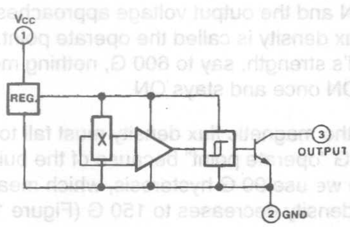

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FIGURE 7

A constant voltage source, as shown in Figure 2, will force a constant bias current to flow in the semiconductor sheet. The output will take the form of a voltage measured across the width of the sheet that will have negligible value in the absence of a magnetic field.

If the biased Hall sensor is placed in a magnetic field with flux lines at right angles to the Hall current (Figure 3), the voltage output is directly proportional to the strength of the magnetic field. This is the Hall effect, discovered by E. F. Hall in 1879.

LINEAR OUTPUT HALL EFFECT DEVICES.

The output voltage of the basic Hall effect sensor (Hall element) is quite small. This can present problems, especially in an electrically noisy environment. Addition of a stable high-quality dc amplifier and voltage regulator to the circuit (Figures 4 and 5) improves the transducer's output and allows it to operate over a wide range of supply voltages. The modified device provides an easy-to-use analog output that is linear and proportional to the applied magnetic flux density.

The UGN3503 is this type of linear output device. The A3506/07/08 have improved sensitivity and temperature-stable characteristics. The output is ratiometric; that is, its output is proportional to its supply voltage.

DIGITAL OUTPUT HALL EFFECT SWITCHES

The addition of a Schmitt trigger threshold detector with built-in hysteresis, as shown in Figure 6, gives the Hall effect circuit digital output capabilities. When the applied magnetic flux density exceeds a certain limit, the trigger provides a clean transition from OFF to ON without contact bounce. Built-in hysteresis eliminates oscillation (spurious switching of the output) by introducing a magnetic dead zone in which switch action is disabled after the threshold value is passed.

An open-collector NPN output transistor added to the circuit (Figure 7) gives the switch digital logic compatibility. The transistor is a saturated switch that shorts the output terminal to ground wherever the applied flux density is higher than the ON trip point of the device. The switch is compatible with all digital families. The output transistor can sink enough current to directly drive many loads, including relays, triacs, SCRs, LEDs, and lamps.

The circuit elements in Figure 7, fabricated on a monolithic silicon chip and encapsulated in a small epoxy or ceramic package, are common to all Hall effect digital switches. Differences between device types are generally found in specifications such as magnetic parameters, operating temperature ranges, and temperature coefficients.

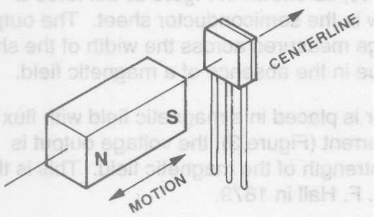

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FIGURE 8

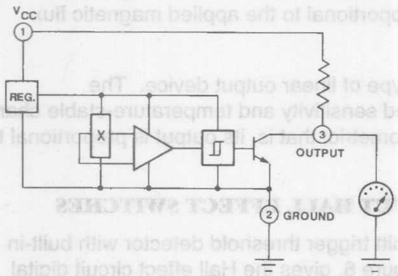

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FIGURE 9

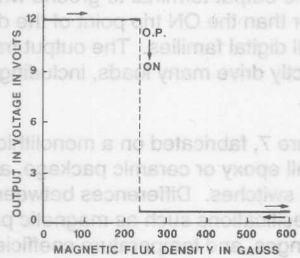

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FIGURE 10

OPERATION

All Hall effect devices are activated by a magnetic field. A mount for the the devices, and electrical connections, must be provided; Parameters such as load current, environmental conditions, and supply voltage must fall within the specific limits shown in the appropriate documentation.

Magnetic fields have two important characteristics—flux density and polarity (or orientation). In the absence of any magnetic field, most Hall effect digital switches are designed to be OFF (open circuit at output). They will turn ON only if subjected to a magnetic field that has both sufficient density and the correct orientation.

Hall switches have an active area that is closer to one face of the package (the face with the lettering, the branded face). To operate the switch, the magnetic flux lines must be perpendicular to this face of the package, and must have the correct polarity. If an approaching south pole would cause switching action, a north pole would have no effect. In practice, a close approach to the branded face of a Hall switch by the south pole of a small permanent magnet will cause the output transistor to turn ON (Figure 8).

A Transfer Characteristics Graph (Figures 10 and 11) plots this information. It is a graph of output as a function of magnetic flux density (measured in gauss) presented to the Hall cell. The magnetic flux density is shown on the horizontal axis. The digital output of the Hall switch is shown along the vertical axis.

To acquire data for this graph, add a power supply and a pull-up resistor that will limit current through the output transistor and enable the value of the output voltage to approach zero (Figure 9).

In the absence of an applied magnetic field (0 G), the switch is OFF, and the output voltage equals the power supply (12 V). A permanent magnet's south pole is then moved perpendicularly toward the active area of the device. As the magnet's south pole approaches the branded face of the switch, the Hall cell is exposed to increasing magnetic flux density. At some point (240 G in this case), the output transistor turns ON and the output voltage approaches zero (Figure 10). That value of flux density is called the operate point. If we continue to increase the field's strength, say to 600 G, nothing more happens. The switch turns ON once and stays ON.

To turn the switch OFF, the magnetic flux density must fall to a value far lower than the 240 G "operate point" because of the built-in hysteresis. For this example we use 90 G hysteresis, which means the device turns OFF when flux density decreases to 150 G (Figure 11). That value of flux density is called the "release point".

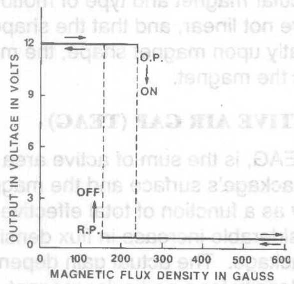

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FIGURE 11

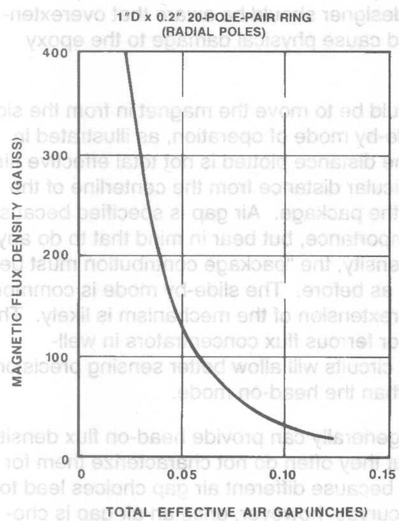

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FIGURE 12A

CHARACTERISTICS AND TOLERANCES

The exact magnetic flux density values required to turn Hall switches ON and OFF differ for several reasons, including design criteria and manufacturing tolerances. Extremes in temperature will also somewhat affect the operate and release points.

For each device type, worst-case magnetic characteristics for the operate value, the release value, and hysteresis are provided.

All switches are guaranteed to turn ON at or below the maximum operate point flux density. When the magnetic field is reduced, all devices will turn OFF before the flux density drops below the minimum release point value. Each device is guaranteed to have at least the minimum amount of hysteresis to ensure clean switching action. This hysteresis ensures that, even if mechanical vibration or electrical noise is present, the switch output is fast, clean, and occurs only once per threshold crossing.

GETTING STARTED

Since the electrical interface is usually straightforward, the design of a Hall effect system should begin with the physical aspects. In position-sensing or motion-sensing applications, the following questions should be answered:

How much and what type of motion is there?

What angular or positional accuracy is required?

How much space is available for mounting the sensing device and activating magnet?

How much play is there in the moving assembly?

How much mechanical wear can be expected over the lifetime of the machine?

Will the product be a mass-produced assembly, or a limited number of machines that can be individually adjusted and calibrated?

What temperature extremes are expected?

A careful analysis will pay big dividends in the long term.

THE ANALYSIS

The field strength of the magnet should be investigated. The strength of the field will be the greatest at the pole face, and will decrease with increasing distance from the magnet. The strength of the magnetic field can be measured with a gaussmeter or a calibrated linear Hall sensor.

A plot of field strength (magnetic flux density) is a function of distance along the intended line of travel of the magnet. Hall device

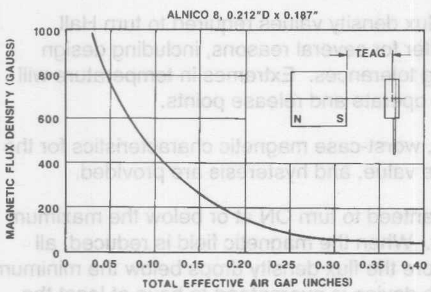

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FIGURE 12B

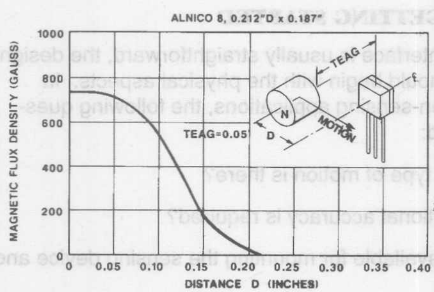

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FIGURE 13

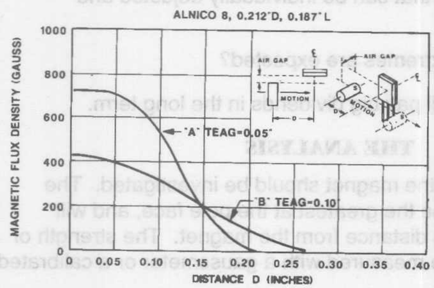

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FIGURE 14

specifications (sensitivity in mV/G for a linear device, or operate and release points in gauss for a digital device) can be used to determine the critical distances for a particular magnet and type of motion. Note that these field strength plots are not linear, and that the shape of the flux density curve depends greatly upon magnet shape, the magnetic circuit, and the path traveled by the magnet.

TOTAL EFFECTIVE AIR GAP (TEAG)

Total effective air gap, or TEAG, is the sum of active area depth and the distance between the package's surface and the magnet's surface. A graph of flux density as a function of total effective air gap (Figure 12A) illustrates the considerable increase in flux density at the sensor provided by a thinner package. The actual gain depends on the characteristic slope of flux density for a particular magnet.

MODES OF OPERATION

Even with a simple bar or rod magnet, there are several possible paths for motion. The magnetic pole could move perpendicularly straight at the active face of the Hall device. This is called the head-on mode of operation. The curve of Figure 12B illustrates typical flux density (in gauss) as a function of TEAG for a cylindrical magnet.

The head-on mode is simple, works well, and is relatively insensitive to lateral motion. The designer should be aware that overextension of the mechanism could cause physical damage to the epoxy package of the Hall device.

A second possibility would be to move the magnet in from the side of the Hall device in the slide-by mode of operation, as illustrated in Figure 13. Note that now the distance plotted is not total effective air gap, but rather the perpendicular distance from the centerline of the magnet to the centerline of the package. Air gap is specified because of its obvious mechanical importance, but bear in mind that to do any calculations involving flux density, the "package contribution must be added and the TEAG used, as before. The slide-by mode is commonly used to avoid contact if overextension of the mechanism is likely. The use of strong magnets and/or ferrous flux concentrators in well-designed slide-by magnetic circuits will allow better sensing precision with smaller magnet travel than the head-on mode.

Magnet manufacturers generally can provide head-on flux density curves for their magnets, but they often do not characterize them for slide-by operation, possibly because different air gap choices lead to an infinite number of these curves; however, once an air gap is chosen, the readily available head-on magnet curves can be used to find the peak flux density (a single point) in the slide-by application by noting the value at the total effective air gap.

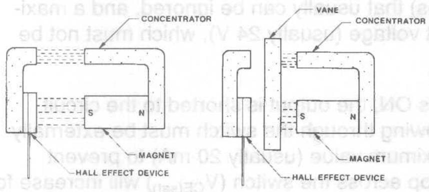

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FIGURE 15

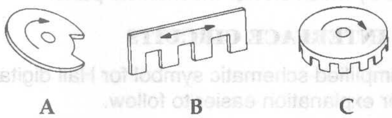

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FIGURE 16

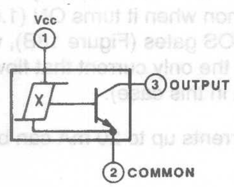

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FIGURE 17

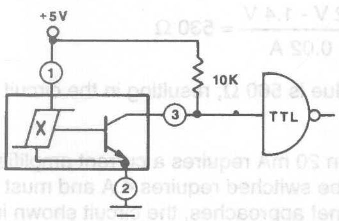

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FIGURE 18A

STEEP SLOPES—HIGH FLUX DENSITIES

For linear Hall devices, greater flux changes for a given displacement give greater outputs, clearly an advantage. The same property is desirable for digital Hall devices, but for more subtle reasons. To achieve consistent switching action in a given application, the Hall device must switch ON and OFF at the same positions relative to the magnet.

To illustrate this concept, consider the flux density curves from two different magnet configurations in Figure 14. With an operate point flux density of 200 G, a digital Hall effect device would turn ON at a distance of approximately 0.14 inches in either case. If manufacturing tolerances or temperature effects shifted the operate point to 300 G, notice that for curve A (steep slope) there is very little change in the distance at which switching occurs. In the case of curve B, the change is considerable. The release point (not shown) would be affected in much the same way. The basic principles illustrated in this example can be modified to include mechanism and device specification tolerances and can be used for worse-case design analysis. Examples of this procedure are shown in later sections.

VANE INTERRUPTER SWITCHING

In this mode, the activating magnet and the Hall device are mounted on a single rigid assembly with a small air gap between them. In this position, the Hall device is held in the ON state by the activating magnet. If a ferromagnetic plate, or vane is placed between the magnet and the Hall device, as shown in Figure 15, the vane forms a magnetic shunt that distorts the flux field away from the Hall device.

Use of a movable vane is a practical way to switch a Hall device. The Hall device and magnet can be molded together as a unit, thereby eliminating alignment problems, to produce an extremely rugged switching assembly. The ferrous vane or vanes that interrupt the flux could have linear motion, or rotational motion, as in an automotive distributor. Ferrous vane assemblies, due to the steep flux density/distance curves that can be achieved, are often used where precision switching over a large temperature range is required.

The ferrous vane can be made in many configurations, as shown in Figure 16. With a linear vane similar to that of Figure 16B, it is possible to repeatedly sense position within 0.002" over a 125°C temperature range.

ELECTRICAL INTERFACE FOR DIGITAL HALL DEVICES

The output stage of a digital Hall switch is simply an open-collector NPN transistor. The rules for use are the same as those for any similar switching transistor.

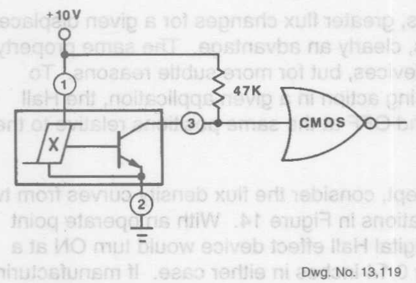

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FIGURE 18B

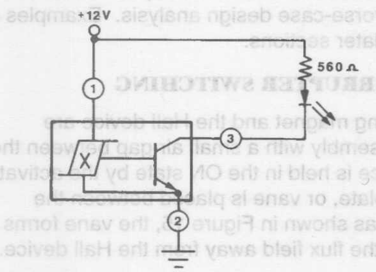

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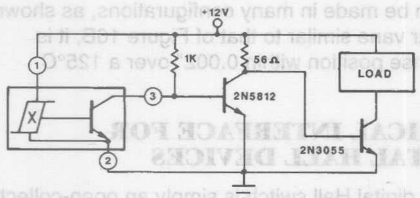
FIGURE 19



Dwg. No. 13,121

FIGURE 20

When the transistor is OFF, there is a small output leakage current (typically a few nanoamps) that usually can be ignored, and a maximum (breakdown) output voltage (usually 24 V), which must not be exceeded.

When the transistor is ON, the output is shorted to the circuit common. The current flowing through the switch must be externally limited to less than a maximum value (usually 20 mA) to prevent damage. The voltage drop across the switch ($V_{CE(sat)}$) will increase for higher values of output current. You must make certain this voltage is compatible with the OFF, or "logic zero," voltage of the circuit you wish to control.

Hall devices switch very rapidly, with typical rise and fall times in the 400 ns range. This is rarely significant, since switching times are almost universally controlled by much slower mechanical parts.

COMMON INTERFACE CIRCUITS

Figure 17 illustrates a simplified schematic symbol for Hall digital switches. It will make further explanation easier to follow.

Interface for digital logic integrated circuits usually requires only an appropriate power supply and pull-up resistor.

With current-sinking logic families, such as DTL or the popular 7400 TTL series (Figure 18A), the Hall switch has only to sink one unit-load of current to the circuit common when it turns ON (1.6 mA maximum for TTL). In the case of CMOS gates (Figure 18B), with the exception of switching transients, the only current that flows is through the pull-up resistor (about 0.2 mA in this case).

Loads that require sinking currents up to 20 mA can be driven directly by the Hall switch.

A good example is a light emitting diode (LED) indicator that requires only a resistor to limit current to an appropriate value. If the LED drops 1.4 V at a current of 20 mA, the resistor required for use with a 12 V power supply can be calculated as:

$$\frac{12\text{ V} - 1.4\text{ V}}{0.02\text{ A}} = 530\ \Omega$$

The nearest standard value is 560 Ω, resulting in the circuit of Figure 19.

Sinking more current than 20 mA requires a current amplifier. For example, if a certain load to be switched requires 4 A and must turn ON when the activating magnet approaches, the circuit shown in Figure 20 could be used.

When the Hall switch is OFF (insufficient magnetic flux to operate), about 12 mA of base current flows through the kΩ resistor to the 2N5812 transistor, thereby saturating it and shorting the base of the 2N3055 to ground, which keeps the load OFF. When a magnet is brought near the Hall switch, it turns ON, shorting the base of the 2N5812 to ground and turning it OFF. This allows:

$$\frac{12\ \text{V}}{56\ \Omega} = 210\ \text{mA}$$

of base current to flow to the 2N3055, which is enough to saturate it for any load current of 4 A or less.

The Hall switch cannot source current to a load in its OFF state, but it is no problem to add a transistor that can. For example, consider using a 40669 triac to turn ON a 115 V or 230 V ac load. This triac would require about 80 mA of gate current to trigger it to the ON condition. This could be done with a 2N5811 PNP transistor, as shown below in Figure 21.

When the Hall switch is turned ON, 9 mA of base current flows into the 2N5811, thereby saturating it and allowing it to supply 80 mA of current to trigger the triac. When the Hall switch is OFF, no base current flows in the 2N5811, which turns it OFF and allows no gate current to pass to the triac. The 4.7 kΩ and the 1 kΩ resistors were added as a safeguard against accidental turn-on by leakage currents, particularly at elevated temperatures.

Note that the +12 V supply common is connected to the low side of the ac line, and in the event of a mixup, the Hall switch and associated low-voltage circuitry would be 115 V above ground. ***Be careful!***

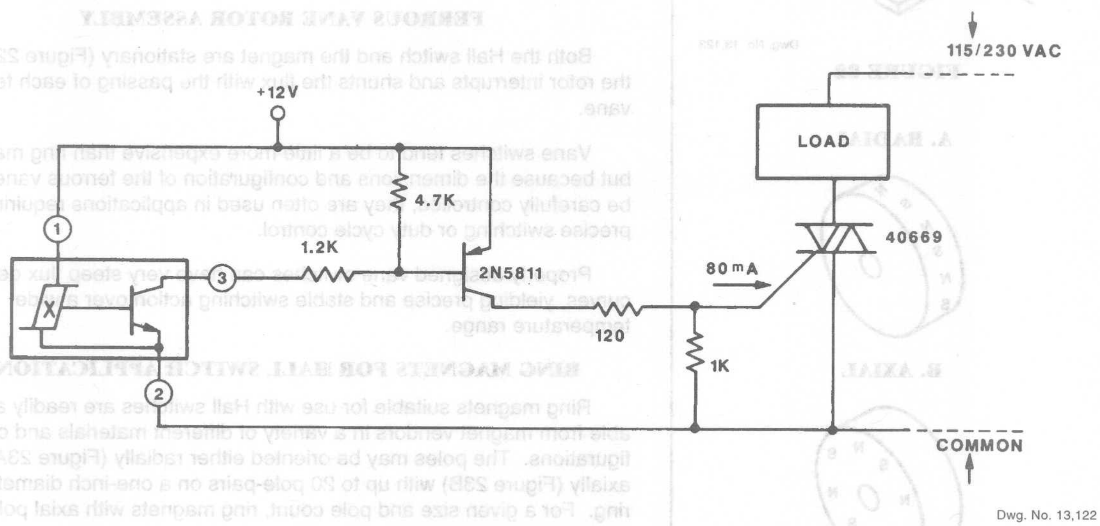


FIGURE 21

A. MAGNETIC ROTOR

B. FERROUS VANE ROTOR

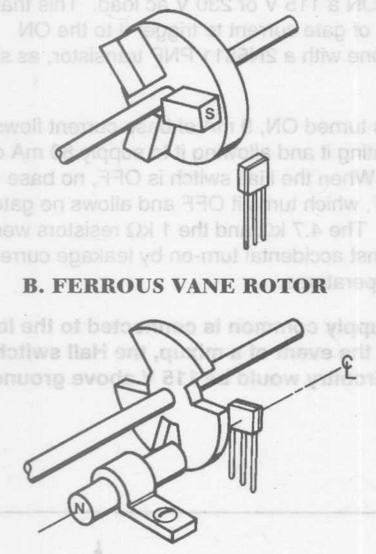


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FIGURE 22

A. RADIAL

B. AXIAL

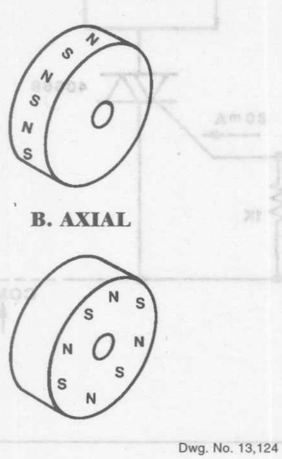

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FIGURE 23

ROTARY ACTIVATORS FOR HALL SWITCHES

A frequent application involves the use of Hall switches to generate a digital output proportional to velocity, displacement, or position of a rotating shaft. The activating magnetic field for rotary applications can be supplied in either of two ways:

MAGNETIC ROTOR ASSEMBLY

The activating magnet(s) are fixed on the shaft and the stationary Hall switch is activated with each pass of a magnetic south pole (Figure 22A). If several activations per revolution are required, rotors can sometimes be made inexpensively by molding or cutting plastic or rubber magnetic material. Ring magnets can also be used. Ring magnets are commercially available disc-shaped magnets with poles spaced around the circumference. They will operate Hall switches dependably and at reasonable costs.

Ring magnets do have limitations:

The accuracy of pole placement (usually within 2 or 3 degrees).

Uniformity of pole strength (±5%, or worse).

These limitations must be considered in applications requiring precision switching.

FERROUS VANE ROTOR ASSEMBLY

Both the Hall switch and the magnet are stationary (Figure 22B); the rotor interrupts and shunts the flux with the passing of each ferrous vane.

Vane switches tend to be a little more expensive than ring magnets, but because the dimensions and configuration of the ferrous vanes can be carefully controlled, they are often used in applications requiring precise switching or duty cycle control.

Properly designed vane switches can have very steep flux density curves, yielding precise and stable switching action over a wide temperature range.

RING MAGNETS FOR HALL SWITCH APPLICATIONS

Ring magnets suitable for use with Hall switches are readily available from magnet vendors in a variety of different materials and configurations. The poles may be oriented either radially (Figure 23A) or axially (Figure 23B) with up to 20 pole-pairs on a one-inch diameter ring. For a given size and pole count, ring magnets with axial poles have somewhat higher flux densities.

Materials most commonly used are various Alnicos, Ceramic 1, and barium ferrite in a rubber or plastic matrix material. Manufacturers usually have stock sizes with a choice of the number of pole pairs. Custom configurations are also available at a higher cost.

Alnico is a name given to a number of aluminum nickel-cobalt alloys that have a fairly wide range of magnetic properties. In general, Alnico ring magnets have the highest flux densities, the smallest changes in field strength with changes in temperature, and the highest cost. They are generally too hard to shape except by grinding and are fairly brittle, which complicates the mounting of bearings or arbor.

Ceramic 1 ring magnets (trade names Indox, Lodex) have somewhat lower flux densities (field strength) than the Alnicos, and their field strength changes more with temperature; however, they are considerably lower in cost and are highly resistant to demagnetization by external magnetic fields. The ceramic material is resistant to most chemicals and has high electrical resistivity. Like Alnico, they can withstand temperatures well above that of Hall switches and other semiconductors, and must be ground if reshaping or trimming is necessary. They may require a support arbor to reduce mechanical stress.

The rubber and plastic barium ferrite ring magnets are roughly comparable to Ceramic 1 in cost, flux density, and temperature coefficient, but are soft enough to shape using conventional methods. It is also possible to mold or press them onto a shaft for some applications. They do have temperature limitations ranging from 70°C to 150°C, depending on the particular material, and their field strength changes more with temperature than Alnico or Ceramic 1.

Regardless of material, ring magnets have limitations on the accuracy of pole placement and uniformity of pole strength which, in turn, limit the precision of the output waveform. Evaluations have shown that pole placement in rubber, plastic, and ceramic magnets usually falls within 2° or 3° of target, but 5° errors have been measured. Variations of flux density from pole to pole will commonly be ±5%, although variations of up to ±30% have been observed.

Figure 24 is a graph of magnetic flux density as a function of angular position for a typical 4 pole-pair ceramic ring magnet, one inch

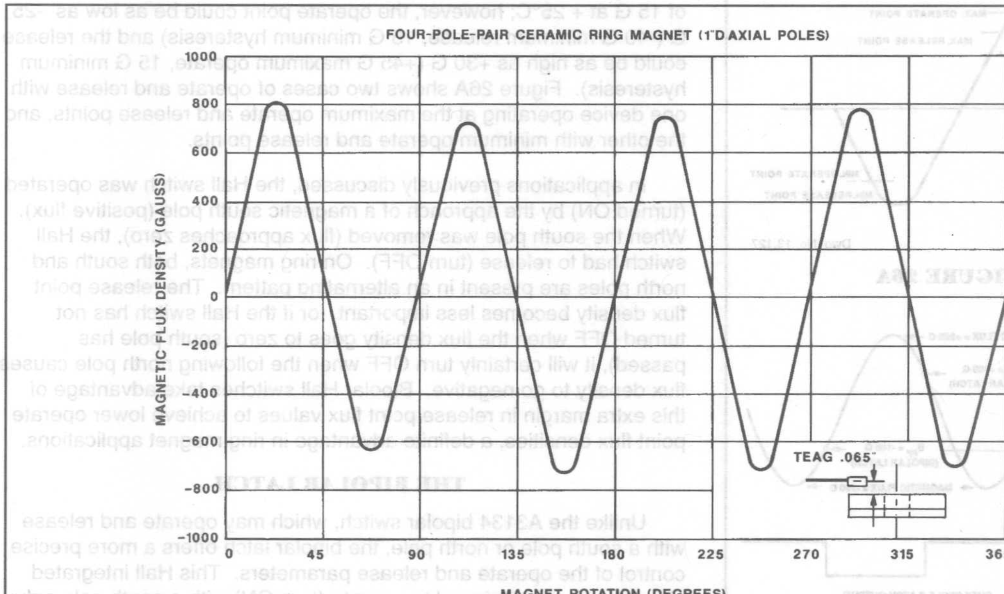

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FIGURE 24

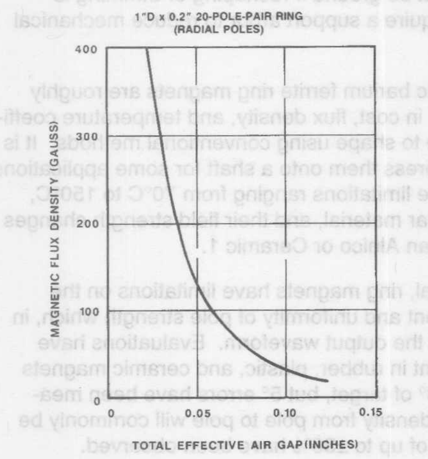

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FIGURE 25

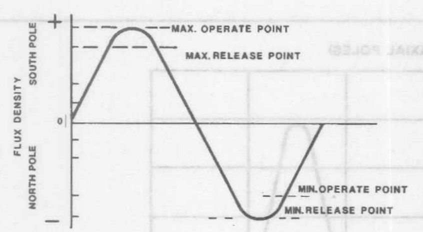

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FIGURE 26A

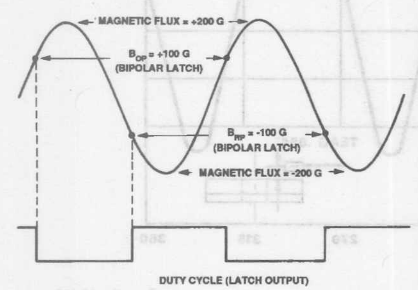

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FIGURE 26B

in diameter, with a total effective air gap of 0.065" (0.050" clearance plus 0.015" package contribution). It shows quite clearly both the errors in pole placement and variations of strength from pole to pole.

A frequent concern with ring magnets is ensuring sufficient flux density for reliable switching. There is a trade-off between the number of pole-pairs and the flux density for rings of a given size. Thus, rings with large numbers of poles have lower flux densities. It is important that the total effective air gap (TEAG) is kept to a minimum, since flux density at the Hall active area decreases by 5 G or 6 G per 0.001" for many common ring magnets. This is clearly shown in Figure 25, a graph of flux density at a pole as a function of TEAG for a typical 20-pole-pair plastic ring magnet. Also shown in Figure 25 is the effect of "package contribution" to the TEAG. The standard "U" package contributes about 0.016". The other factor contributing to TEAG is mechanical clearance, which should be as small as possible, consistent with dimensional tolerances of the magnet, bearing tolerances, bearing wear, and temperature effects on the Hall switch mounting bracket.

WHAT IS A BIPOLAR SWITCH?

A bipolar switch, the A3134, has a maximum operate point of +45 G, a minimum release point of -40 G, and a minimum hysteresis of 15 G at + 25°C; however, the operate point could be as low as -25 G (-40 G minimum release, 15 G minimum hysteresis) and the release could be as high as +30 G (+45 G maximum operate, 15 G minimum hysteresis). Figure 26A shows two cases of operate and release with one device operating at the maximum operate and release points, and the other with minimum operate and release points.

In applications previously discussed, the Hall switch was operated (turned ON) by the approach of a magnetic south pole (positive flux). When the south pole was removed (flux approaches zero), the Hall switch had to release (turn OFF). On ring magnets, both south and north poles are present in an alternating pattern. The release point flux density becomes less important, for if the Hall switch has not turned OFF when the flux density goes to zero (south pole has passed), it will certainly turn OFF when the following north pole causes flux density to go negative. Bipolar Hall switches take advantage of this extra margin in release point flux values to achieve lower operate point flux densities, a definite advantage in ring magnet applications.

THE BIPOLAR LATCH

Unlike the A3134 bipolar switch, which may operate and release with a south pole or north pole, the bipolar latch offers a more precise control of the operate and release parameters. This Hall integrated circuit has been designed to operate (turn ON) with a south pole only; it will then remain ON when the south pole has been removed. In

order to have the bipolar latch release (turn OFF), it must be presented with a north magnetic pole. This alternating south pole-north pole operation, when properly designed, will produce a duty cycle approaching 50%.

The UGN3175 was designed specifically for applications requiring a tightly controlled duty cycle, such as in brushless dc motor commutation. This was accomplished with the introduction of the bipolar latch in 1982. The 3175 has become very popular as a brushless dc motor commutator, shaft encoder, speedometer element, and tachometer sensor.

Duty cycle is controlled with an alternating magnetic field, as shown in Figure 26B.

DESIGN EXAMPLE

Given:

Operating temperature range of -20° to +85°C.

Bipolar Hall switch in standard "U" package:

Maximum operate point +200 G from -20° to + 85°C.

Minimum release point -200 G from -20°C to + 85°C.

Air gap package contribution 0.016".

Necessary mechanical clearance 0.030".

First, find the total effective air gap:

TEAG = clearance + package contribution

TEAG = 0.030" + 0.016" = 0.046"

Now, determine the necessary flux density sufficient to operate the Hall switch, plus 40%.

To operate the Hall switch, the magnet must supply a minimum of ±200 G at a distance of 0.046" over the entire temperature range. Good design practice requires the addition of extra flux to provide some margin for aging, mechanical wear, and other imponderables. If we add a pad of 100 G, a reasonable number, the magnet required must supply ±300 G at a distance of 0.046" over the temperature range.

TEMPERATURE EFFECTS

Unfortunately, magnet strength is affected by temperature to some degree. Temperature coefficients of some common magnetic materials are given below:

Material	Temperature Coefficient
Rubber/Plastic	-0.2% to -0.3% per °C
Ceramic 1	-0.15% to -0.2% per °C
Alnico 2, 5	-0.02% to -0.03% per °C
Alnico 8	±0.01% per °C

If we are considering a ceramic ring magnet with a worst-case temperature coefficient of -0.2%/°C, we must add some extra flux density to the requirement at room temperature to ensure that we still have +300 G per south pole at +85°C. This amount is:

[(85°C - 25°C) x 0.2%/°C] 300 G = +36 G

Thus, the flux density that will ensure that the Hall switch will operate over temperature is 300 G + 36 G = 336 G per south pole at +25°C.

Follow the same procedure for the north pole requirements. If the magnet will supply +300 G per south pole and -300 G per north pole at +85°C, it will supply even more flux density per north pole at -20°C because of the negative temperature coefficient.

In applications where temperature conditions are more severe, Alnico magnets are considerably better than the ceramic magnets we considered. It is also possible to order custom Hall switches with specifications tailored to your application. For example, you can specify a range of operate and release points at a particular temperature, with temperature coefficients for operate and release points, if that is better suited to your application. On a custom basis, Hall switches are available with operate and release point temperature coefficients of less than 0.3 G/°C, and with operate flux densities of less than 100 G.

If you intend to use a low-cost, low flux density ring magnet, then a device in the 0.060" package would be a good choice. The package contribution is 0.016", which results in a significant improvement in peak flux density from a magnet, as shown in Figure 25.

If the rotor drive can withstand an increased torque requirement, consider a ferrous flux concentrator. Flux density can be increased by 10% to 40% in this manner. A concentrator of 0.03125" mild steel

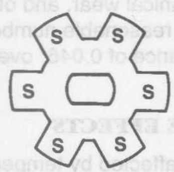

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FIGURE 27

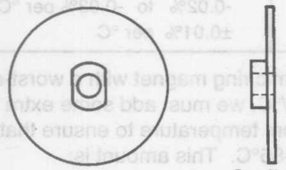

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FIGURE 28

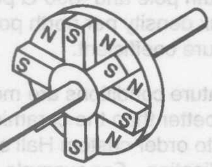

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FIGURE 29

Dwg. No. 13,132

FIGURE 30

having the same dimensions as, and cemented to, the back surface of the Hall switch, will increase flux density by about 10%. A return path of mild steel from the back side of the device to the adjacent poles can add even more. Often the functions of mounting bracket and flux concentrator can be combined. Additional information can be found in the section on flux concentrators.

RING MAGNETS —DETAILED DISCUSSION

AN INEXPENSIVE ALTERNATIVE

Innovative design can produce surprisingly good results. Rubber and plastic magnet stock comes in sheets. One side of the sheet is magnetic north; the other side is south. This material is relatively inexpensive and can easily be stamped or die-cut into various shapes.

These properties prompted one designer to fabricate an inexpensive magnetic rotor assembly that worked very well. The rubber magnet stock was die-cut into a star-shaped rotor form, as shown in Figure 27. A nylon bushing formed a bearing, as shown in Figure 28.

Finally, a thin mild steel backing plate was mounted to the back of the assembly to give mechanical strength and to help conduct the flux back from the north poles on the opposite side. This actually served to form apparent north poles between the teeth; the measured flux between south pole teeth is negative. Figure 29 shows the completed magnetic rotor assembly, essentially a ring magnet with axial poles.

The Hall switch was mounted with its active surface close to the top of the rotor assembly, facing the marked poles. There is some versatility in this approach, as asymmetrical poles can be used to fabricate a rotor that wll allow trimmable ON time and, thus, work as a timing cam. Figure 30 illustrates a cam timer adjusted to 180° ON and 180° OFF.

RING MAGNET SELECTION

When you discuss your application with a magnet vendor, the following items should be considered:

Mechanical Factors

- Dimensions and tolerances
- Mounting hole type and maximum eccentricity
- Rotational speed
- Mechanical support required
- Coefficient of expansion

Magnetic Factors

- Poles: number, orientation, and placement accuracy
- Flux density at a given TEAG (remember to add the Hall switch package contribution to the clearance figure)
- Magnetic temperature coefficient

Environmental Factors

- Tolerance of the material to the working environment (temperature, chemical solvents, electric potentials)

Flux density curves from several typical ring magnets are included to present an idea of what can be expected from various sizes and materials. Figure 31 shows the curve for a ring similar in size and material to that of Figure 25, but with 10 pole-pairs instead of 20

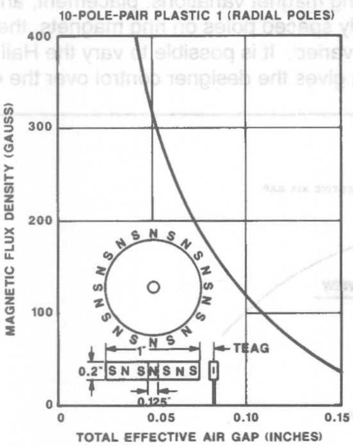

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FIGURE 31

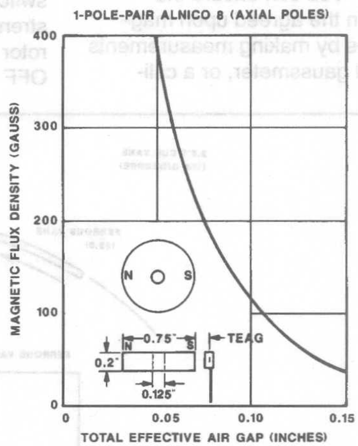

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FIGURE 32

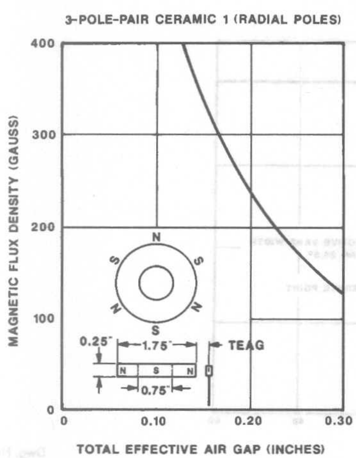

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FIGURE 33

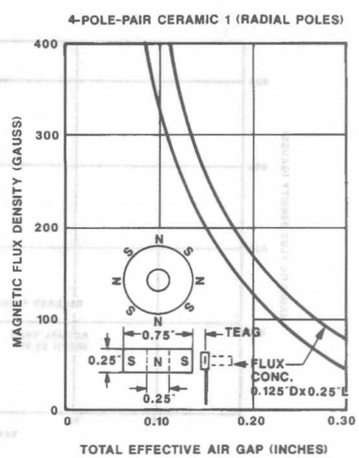

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FIGURE 34

(note increased flux density values). Figure 32 shows the curve from a one pole-pair Alnico 8 ring. Figure 33 shows the curve from a three-pole-pair Ceramic 1 ring. Figure 34 shows the curves from a four-pole-pair Ceramic 1 ring, with and without a ferrous flux concentrator.

Incoming inspection of ring magnets is always advisable. You can ensure the magnets are within the agreed upon magnetic specifications by making measurements with a commercial gaussmeter, or a calibrated linear Hall device mounted in a convenient test fixture. Calibrated UGN3503U Hall devices and technical assistance are available.

FERROUS VANE ROTARY ACTIVATORS

A ferrous vane rotor assembly is the alternative to magnetic rotors for rotary Hall switch applications. As shown previously, a single magnet will hold a Hall switch ON except when one of the rotor vanes interrupts the flux path and shunts the flux path away from the Hall switch. The use of a single stationary magnet allows very precise switching by eliminating ring magnet variations, placement, and strength. Unlike the evenly spaced poles on ring magnets, the width of rotor vanes can easily be varied. It is possible to vary the Hall switch OFF and ON times, which gives the designer control over the duty

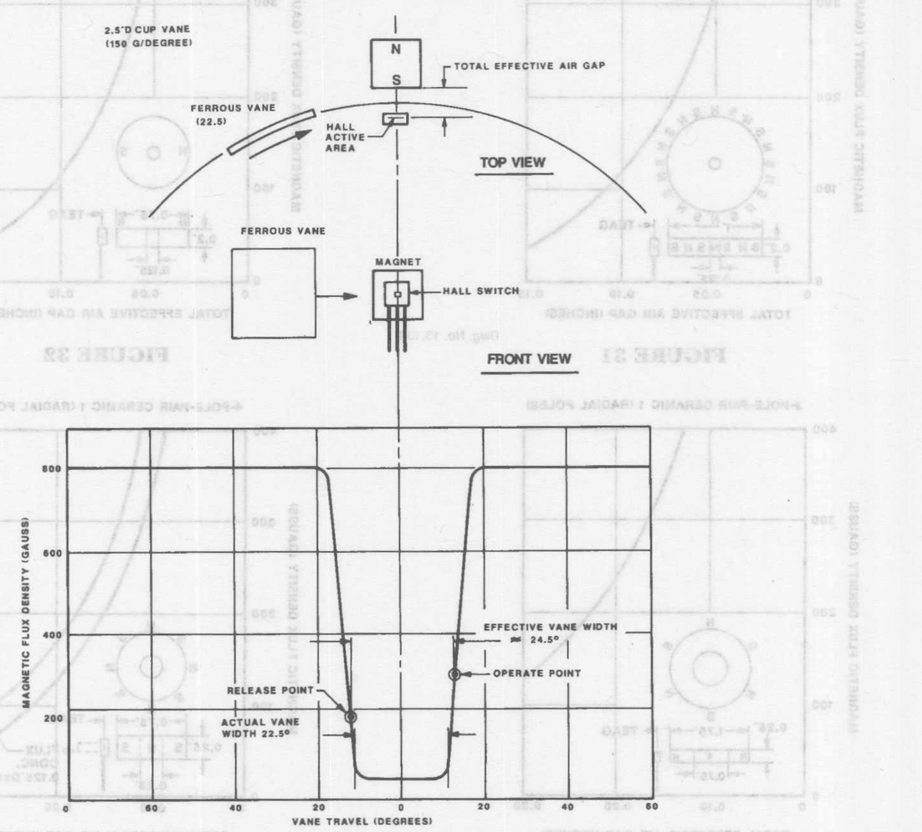

FIGURE 35

cycle of the output waveform. Ferrous vane rotors are a good choice where precise switching is desired over a wide range of temperatures. As the vane passes between magnet and Hall switch, progressively more flux will be blocked or shunted. Small variations in lateral position have a very small effect on the transition point.

A FERROUS VANE IN OPERATION

Figure 35 combines top and front views of a ferrous vane magnet/Hall switch system with the graph of flux density as a function of vane travel produced by this system. Note that the drawings and the graph are vertically aligned along the horizontal axis. Position is measured from the leading edge of the vane to the centerline of the magnet/Hall device.

Initially, when the vane is located entirely to the left of the magnet, the vane has no effect and the flux density at the sensor is at a maximum of 800 G. As the leading edge of the vane nears the magnet, the shunting effect of the vane causes the flux density to decrease in a nearly linear fashion. There, the magnet is covered by the vane and flux density is at a minimum. As the vane travels on it starts to uncover the magnet. This allows the flux to increase to its original value. After that, additional vane travel has no further influence on flux density at the sensor.

A Hall switch located in the position of the sensor would initially be ON because of the presence of the magnetic field. Somewhere in the linearly decreasing region, the flux would fall below the release point, and

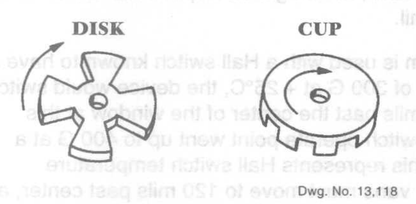

FIGURE 36

the Hall switch would turn OFF. It would remain OFF until the increasing flux reaches the operate point for that particular Hall switch. Recall that the operate point flux density is greater than the release point flux density by the amount of hysteresis for that particular Hall switch.

The interval during which the Hall switch remains OFF is determined by the actual width of the vane and the steepness of the magnetic slope, as well as by the operate and release point flux density values for the Hall switch. This interval is called the effective vane width, and it is always somewhat greater than the physical vane width.

ROTOR DESIGN

Two commonly used rotor configurations are the disk and the cup, as shown in Figure 36.

The disk is easily fabricated and, hence, is often used for low-volume applications such as machine control. Axial movement of the rotor must be considered. Vane activated switches tolerate this quite well, but the rotor must not hit the magnet or the Hall switch.

Cup rotors are somewhat more difficult to fabricate and so are more expensive, but dealing with a single radial distance simplifies calculations and allows precise control of the output waveforms. For cup rotors, radial bearing wear or play is the significant factor in determining the clearances, while axial play is relatively unimportant. Cup rotors have been used very successfully in automotive ignition systems. The dwell range is determined by the ratio of the vane-to-window widths when the rotor is designed. Firing point stability may be held to ±0.005 distributor degrees per degree Celsius in a well-designed system.

MATERIAL

Vanes are made of a low carbon steel to minimize the residual magnetism and to give good shunting action. The vane thickness is chosen to avoid magnetic saturation for the value of flux density it must shunt. Vanes usually are between 0.03" and 0.06" thick.

VANE/WINDOW WIDTHS, ROTOR SIZE

Generally, the smallest vanes and window on a rotor should be at least one and one-half times the width of the magnet pole to provide adequate shunting action and to maintain sufficient differential between the OFF and ON values of flux density.

In Table 1, the maximum flux density (obtained with window centered over the magnet, the minimum flux density (vane centered over the magnet), and the difference between the two values are tabulated for three cases:

1. Vane and window width the same as magnet pole width.

2. Vane and window width one and one-half times magnet pole width.

3. Vane and window width two times the magnet pole width.

In each case the magnet is 0.25" x 0.25" x 0.125" samarium cobalt; the air gap is 0.1"; the rotor vanes are made of 0.04" mild steel stock.

TABLE 1

Window Vane Width Factor	1.0	1.5	2.0
Flux Density with Window Centered	630 G	713 G	726 G
Flux Density with Vane Centered	180 G	100 G	80 G
Flux Change Density	450 G	613 G	646 G

If a small rotor with many windows and vanes is required, a miniature rare earth magnet must be used to ensure sufficient flux density for reliable operation. For example, a 0.1" cubical samarium cobalt magnet makes it practical to fabricate a .25" diameter rotor with as many as 10 windows and vanes. With fewer vanes, even further size reduction is possible.

TABLE 2

Curve	Magnet	Air Gap	Slope G/mil	*Concentrator
A	0.25"D, 0.25"L Samarium Cobalt	0.1"	14	Yes
B	0.25"D, 0.25"L Samarium Cobalt	0.1"	9.85	No
C	0.25"D, 0.125"L Samarium Cobalt	0.1"	9.0	Yes
D	0.25"D, 0.125"L Samarium Cobalt	0.125"	8.7	Yes
E	0.25"D, 0.125"L Samarium Cobalt	0.1"	7.8	No
F	0.25"D, 0.125"L Samarium Cobalt	0.125"	6.3	No
G	0.25"D, 0.125"L Samarium Cobalt	0.125"	5.6	Yes
H	0.25"D, 0.125"L Samarium Cobalt	0.125"	4.5	No

NOTE: The "U" package is used for all measurements.*

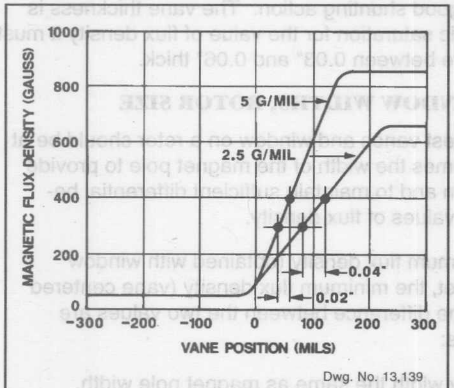

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FIGURE 37

STEEP MAGNETIC SLOPES FOR CONSISTENT SWITCHING

The flux density vane travel graph for most common vane configurations (Figure 35), is very nearly linear in the transition regions. The Hall switch operate and release points fall in these linear transition regions, and it is easily seen that if these values change, the position of the vane which causes the switching must change also. Figure 37 shows the flux density as a function of vane position for two different magnetic circuits. In one case, the magnetic slope is 2.5 G/mil. In the second case, it is 5.0 G/mil.

If the 2.5 G/mil system is used with a Hall switch known to have an operate point flux density of 300 G at +25°C, the device would switch ON when the vane is 85 mils past the center of the window at this temperature. If the Hall switch operate point went up to 400 G at a temperature of +125°C (this represents Hall switch temperature coefficient of 1 G/°C), the vane must move to 120 mils past center, a change in switching position of 45 mils. If the same Hall switch is used in the second system having the 5 mil/G slope, the operate point would shift only 20 mils, or half as much, since the slope is twice as steep.

Slopes in typical vane systems range from 1 G/mil to 15 G/mil, and are affected by magnet type and size, the magnetic circuit, and the total effective air gap. It is interesting to note that, although slide-by operation can give very steep slopes, the transition point is much affected by lateral motion (change in air gap); therefore, vanes are often preferred for applications involving play or bearing wear.

SMALL AIR GAPS FOR STEEP SLOPES

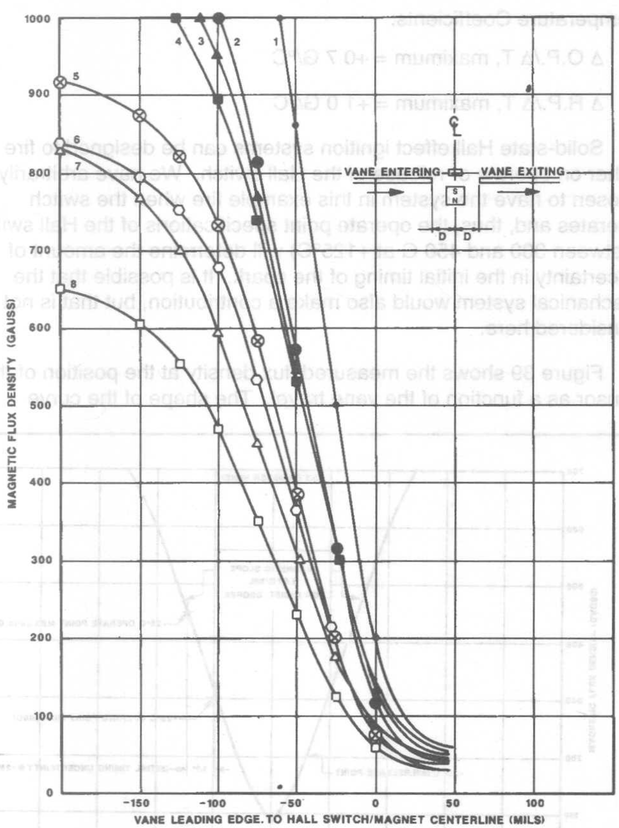
The air gap should be as small as the mechanical system allows. Factors to be considered are:

Vane material thickness and vane radius.

Maximum eccentricity for cup vanes.

Bearing tolerance and wear.

Change in air gap with temperature due to mounting considerations.



SYMBOL	MAGNET	AIR GAP	SLOPE (G/MIL)	*CONC.
1 •	0.25"D, 0.25"L SAM.CO.	0.1"	14	YES
2 ●	0.25"D, 0.25"L SAM.CO.	0.1"	9.85	NO
3 ▲	0.25"D, 0.125"L SAM.CO.	0.1"	9.0	YES
4 ■	0.25"D, 0.25"L SAM.CO.	0.125"	8.7	YES
5 ⊗	0.25"D, 0.125"L SAM.CO.	0.1"	7.8	NO
6 ○	0.25"D, 0.25"L SAM.CO.	0.125"	6.3	NO
7 △	0.25"D, 0.125"L SAM.CO.	0.125"	5.6	YES
8 □	0.25"D, 0.125"L SAM.CO.	0.125"	4.5	NO

NOTE - THE "U" PACKAGE IS USED FOR ALL MEASUREMENTS

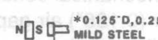


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FIGURE 38

In Figure 38, two different samarium cobalt magnets are used in a vane system to illustrate the effects of changes in air gap and magnet size. Note that only the falling transition region is shown (transition regions are symmetrical). The distances on the horizontal axis have been measured from the leading edge of the vane.

The term "air gap" as used in Figure 38 is not the total effective air gap; but is simply the distance from the face of the magnet to the surface of the Hall switch. It does not include the package contribution. The "U" package is often used in ferrous vane applications because it has a shallow active area depth.

FLUX CONCENTRATORS PAY DIVIDENDS

What if economic or size considerations dictated the smaller magnet used in Figure 38, and mechanical considerations dictated the larger (0.125") air gap, but the resulting flux density and slope (Curve 8) were not good enough? Curve 7 in Figure 38 shows the very substantial improvement that can be achieved by adding simple flux concentrators. Those used in the example were 0.125" in diameter by 0.250" long, and were fastened behind the Hall switch.

DESIGN EXAMPLE

The magnet/concentrator configuration we just considered (Curve 7, Figure 38) seems to offer a high performance/cost ratio. Following is an evaluation of its use in an automotive ignition system using a 2.5" diameter cup rotor.

The initial timing and wide operating temperature range requirements for this application have generally led designers to specify custom Hall switches in terms of the minimum and maximum operate or release point at +25°C, plus a maximum temperature coefficient on these parameters over the operating temperature range. Representative specifications might be:

+25°C Operate Point, Minimum .... 300 G

+25°C Operate Point, Maximum .... 450 G

+25°C Release Point, Minimum .... 200 G

Temperature Coefficients:

Δ O.P./Δ T, maximum = +0.7 G/°C

Δ R.P./Δ T, maximum = +1.0 G/°C

Solid-state Hall effect ignition systems can be designed to fire either on operate or release of the Hall switch. We have arbitrarily chosen to have the system in this example fire when the switch operates and, thus, the operate point specifications of the Hall switch (between 300 and 450 G at +125°C) will determine the amount of uncertainty in the initial timing of the spark. It is possible that the mechanical system would also make a contribution, but that is not considered here.

Figure 39 shows the measured flux density at the position of the sensor as a function of the vane travel. The shape of the curve

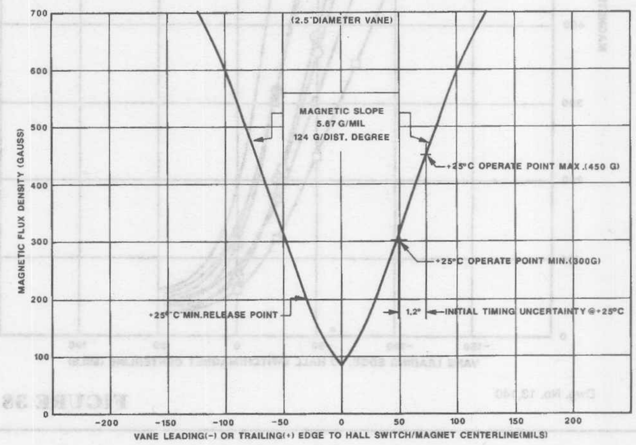

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FIGURE 39

requires explanation: Because the flat minimum and maximum flux regions are irrelevant, it is convenient to measure from the vane's leading edge to edge of the vane to the magnet centerline while plotting data for the rising transition. (The same presentation would result if all data were plotted while a vane passed the magnet the center low flux areas were snipped out, and the ends containing the linear transitions were pulled together.) From this graph, we can identify the magnetic slope of the transition regions for our system— approximately 5.67 G per 0.001" of vane travel.

Calculations based on the rotor diameter (2.5") show we have 22 mils of vane travel per distributor degree. The 5.67 G/mil slope obtained from Figure 39 is equivalent to 125 G per distributor degree. From the specifications, it is known that the Hall switch will operate when flux is between 300 and 450 G, leaving a 150 G window of uncertainty. At +25°C, this will be:

$$150\text{ G} \times \frac{\text{Distributor Degree}}{125\text{ G}} =$$

$$1.2\text{ Distributor Degrees}$$

Additional contributions to the initial timing uncertainty will result if the total effective air gap is changed, as that would affect the shape or slopes of the magnetic flux density/vane travel curve of Figure 39. Factors to be considered are the magnet peak energy product tolerances, as well as manufacturing tolerances in the final Hall switch/magnet assembly.

TEMPERATURE STABILITY OF OPERATE POINT

An early Hall switch operate-point temperature coefficient was approximately 0.2 G/°C. To translate this into distributor degrees per degree Celsius, we take:

$$\frac{0.2\text{ G}}{1°\text{C}} \times \frac{\text{Distributor Degrees}}{125\text{ G}} =$$

$$0.0016\text{ Distributor Degrees/°C}$$

The distributor timing would, therefore, change 0.16 degrees for a temperature change of 100°C.

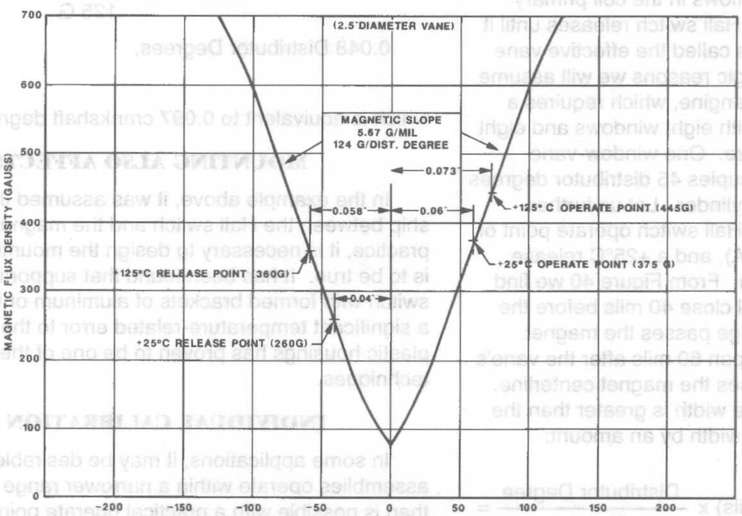

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FIGURE 40

A typical samarium cobalt magnet temperature coefficient is -0.04%/°C. A magnetic field of 375 G at +25°C would decrease to 360 G at +125°C. For Figure 40, our system has a magnetic slope of 5.67 G/mil, giving an additional vane travel requirement at +125°C of:

$$(375\text{ G}-360\text{ G}) \times \frac{1\text{ mil}}{5.67\text{ G}} = 2.7\text{ mils}$$

This translates to timing change of:

$$2.7\text{ mils} \times \frac{\text{Distributor Degree}}{22\text{ mils}} =$$

0.12 Distributor Degrees

for a temperature change of 100°C.

CALCULATING DWELL ANGLE AND DUTY CYCLE VARIATIONS

The dwell angle in a conventional system is the number of distributor degrees during which the points are closed, which corresponds to the amount of time current can flow in the coil's primary winding. In our example, current flows in the coil primary from the time the Hall switch releases until it operates, which is called the effective vane width. For nostalgic reasons we will assume an eight-cylinder engine, which requires a distributor rotor with eight windows and eight vanes of equal size. One window-vane segment thus occupies 45 distributor degrees and will fire one cylinder. Let us further assume a typical Hall switch operate point of 375 G at +25°C (A), and a +25°C release point of 260 G (B). From Figure 40 we find that the points will close 40 mils before the vane's leading edge passes the magnet centerline; they open 60 mils after the vane's trailing edge passes the magnet centerline. The effective vane width is greater than the mechanical vane width by an amount:

$$(60\text{ mils} + 40\text{ mils}) \times \frac{\text{Distributor Degree}}{22\text{ mils}} =$$

4.54 Distributor Degrees

This gives a dwell angle of (45° + 4.54°) = 49.54 distributor degrees at +25°C. The duty cycle is:

$$\frac{49.54°}{90°} = 55.0\% \text{ at } +25°\text{C}.$$

Using the specified worst-case temperature coefficients, we calculate the new operate and release points at +125°C to be 445 G (C) and 360 G (D), also shown in Figure 40. The dwell angle at +125°C would then be:

$$45° + \left[(73\text{ mils} + 58\text{ mils}) \times \frac{\text{Distributor Degree}}{22\text{ mils}}\right] =$$

50.9 Distribution Degrees

The duty cycle is then:

$$\frac{50.9°}{90°} = 56.6\%$$

EFFECTS OF BEARING WEAR

A ±10 mil radial movement of the vane, with its position adjusted to the approximate operate point of the Hall switch, gave a measured change of ±6 G. This translates into a change of:

$$6\text{ G} \times \frac{\text{Distributor Degrees}}{125\text{ G}} =$$

0.048 Distributor Degrees,

which is equivalent to 0.097 crankshaft degrees.

MOUNTING ALSO AFFECTS STABILITY

In the example above, it was assumed that the physical relationship between the Hall switch and the magnet was absolutely stable. In practice, it is necessary to design the mountings with some care if this is to be true. It has been found that supporting the magnet or Hall switch with formed brackets of aluminum or brass will often contribute a significant temperature-related error to the system. Use of molded plastic housings has proven to be one of the better mounting techniques.

INDIVIDUAL CALIBRATION TECHNIQUES

In some applications, it may be desirable to have the vane switch assemblies operate within a narrower range of vane edge positions than is possible with a practical operate point specification for the Hall switch; for example, if it were necessary to reduce the initial timing window in the previous case. One solution would be individual

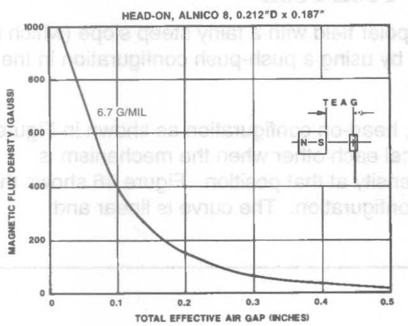

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FIGURE 41

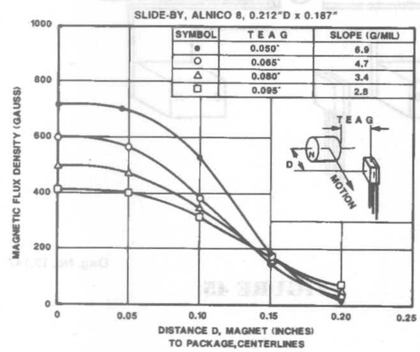

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FIGURE 42

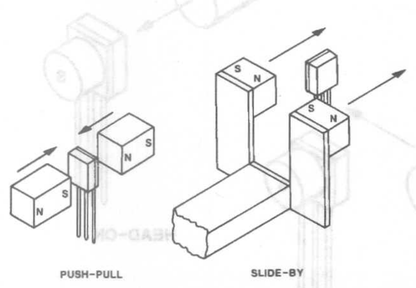

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FIGURE 43

calibration. Possible techniques include:

1) Adjusting the air gap by changing the magnet position.
2) Adjusting the position of a flux concentrator behind the Hall switch.
3) Adjusting the position of a small bias magnet mounted behind the Hall switch.
4) Demagnetizing the magnet in small increments that would decrease the magnetic slope and, thus, increase the temperature effects.
5) Adjusting the position of the Hall switch-magnet assembly relative to the rotor in a manner similar to rotating an automotive distributor to change the timing.

OPERATING MODES

HEAD-ON AND SLIDE-BY MODES

The most common operating modes are head-on and slide-by. The head-on mode is simple and relatively insensitive to lateral motion, but cannot be used where overextension of the mechanism might damage the Hall switch. The flux density plot for a typical head-on operation (Figure 41) shows that the magnetic slope is quite shallow for low values of flux density, a disadvantage that generally requires extreme mechanism travel and extreme sensitivity to flux changes in operate and release points of the Hall switch. This problem can be overcome by selecting Hall switches with higher operate and release properties.

The slide-by mode is also simple, can have reasonably steep slopes (to about 10 G/mil) and has no problem with mechanism over-travel. It is, however, very sensitive to lateral play, as the flux density varies dramatically with changes in the air gap. This can be seen clearly in the curves of Figure 42, in which the flux density curves are plotted for actual slide-by operation with various air gaps. It is apparent that the operating mechanism can have little side play if precise switching is required.

OPERATING MODE ENHANCEMENTS —COMPOUND MAGNETS

PUSH-PULL

Because the active area of a Hall switch is close to the branded face of the package, it is usually operated by approaching this face with a magnetic south pole. It is also possible to operate a Hall switch by applying a magnetic north pole to the back side of the package. While a north pole alone is seldom used, the push-pull configuration (simultaneous application of a south pole to the branded side and a north pole to the back side) can give much greater field strengths

than are possible with any single magnet (Figure 43). Perhaps more important, push-pull arrangements are quite insensitive to lateral motion and are worth considering if a loosely fitting mechanism is involved.

Figure 44 shows the flux density curve for an actual push-pull slide-by configuration that achieves a magnetic slope of about 8 G/mil.

PUSH-PUSH

Another possibility, a bipolar field with a fairly steep slope (which is also linear), can be created by using a push-push configuration in the head-on mode. (Figure 45)

In the push-push mode, head-on configuration as shown in Figure 45, the magnetic fields cancel each other when the mechanism is centered, giving zero flux density at that position. Figure 46 shows the flux density plot of such a configuration. The curve is linear and

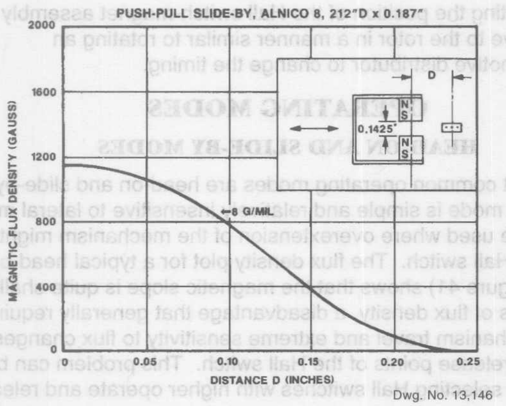

FIGURE 44

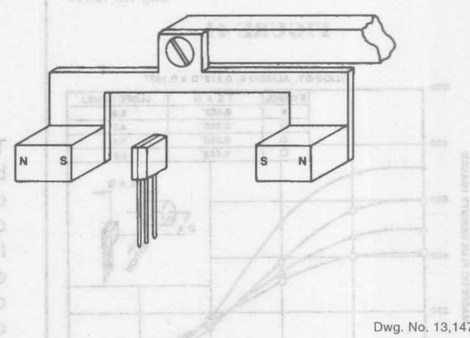

FIGURE 45

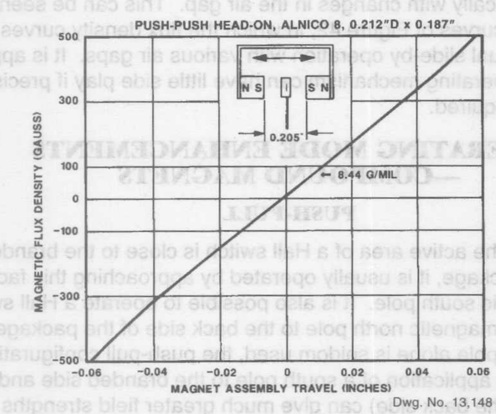

FIGURE 46

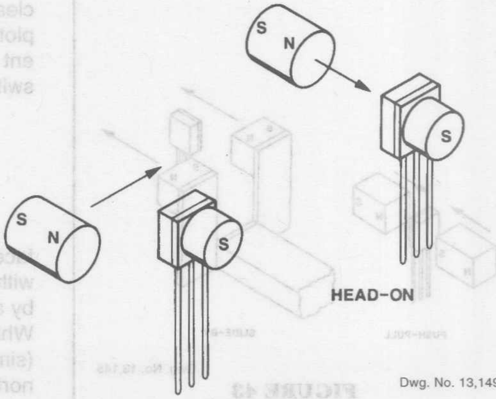

FIGURE 47

moderately steep at better than 8 G/mil. The mechanism is fairly insensitive to lateral motion.

BIASED OPERATION

It is also possible to bias the Hall switch by placing a stationary north or south pole behind it to alter the operate and release points. For example, a north pole attached to the reverse face would turn the device normally ON until a north pole providing a stronger field in the opposite direction approached the opposite face. (Figure 47)

Figures 48-51 demonstrate four additional slide-by techniques. Compound magnets are used in push-pull, slide-by, edgewise configurations to achieve a magnetic slope of 17.4 G/mil. Rare earth magnets may be used to obtain substantially steeper slopes. A flux density curve of up to 100 G/mil is obtainable.

INCREASING FLUX DENSITY BY IMPROVING THE MAGNETIC CIRCUIT

Magnetic flux can travel through air, plastic, and most other materials only with great difficulty. Since there is no incentive for flux from the activating magnet to flow through the (plastic and silicon) Hall device, only a portion of it actually does. The balance flows around the device and back to the other pole by whatever path offers the least resistance. (Figure 52)

However, magnetic flux easily flows through a ferromagnetic material such as mild steel. The reluctance of air is greater by a factor of several thousand than that of mild steel.

In a Hall device application, the goal is to minimize the reluctance of the flux path from the magnetic south pole, through the Hall device, and back to the north pole. The best possible magnetic circuit for a Hall device would provide a ferrous path for the flux, as shown in Figure 53, with the only "air gap" being the Hall device itself.

While a complete ferrous flux path is usually impractical, unnecessary, and even impossible in applications requiring an undistorted or undisturbed flux field, it is a useful concept that points the way to a number of very practical compromises for improving flux density.

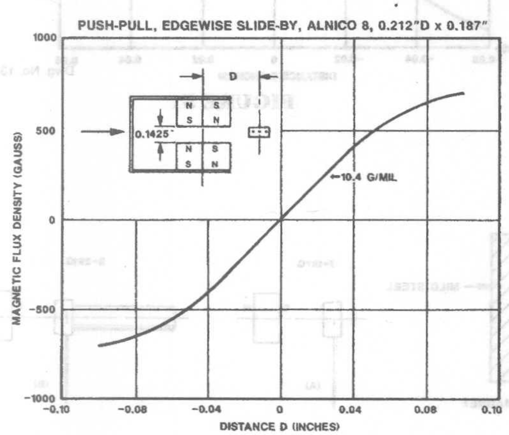

FIGURE 48

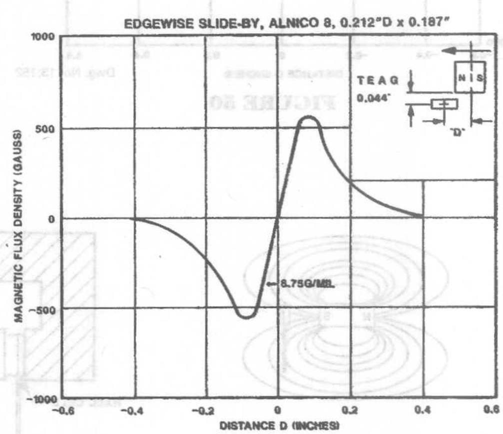

FIGURE 49

FLUX CONCENTRATORS

Flux concentrators are low carbon (cold-rolled) steel magnetic conductors. They are used to provide a low reluctance path from a magnet's south pole, through the Hall sensor, and back to the north pole. Flux concentrators can take many forms and will often allow use of smaller or less expensive magnets (or less expensive, less sensitive Hall devices) in applications where small size or economy are important. They are of value whenever it is necessary or desirable to increase flux density at the Hall device. Increases of up to 100% are possible.

An example of the effectiveness of a concentrator is illustrated in Figures 54(A) and 54(B).

(A) The south pole of a samarium cobalt magnet 0.25" square and 0.125" long, is spaced 0.25" from the Hall switch. There is a flux density of 187 G at the active area.

(B) With a concentrator 0.125" in diameter and 0.5" long, the flux density increases to 291 G.

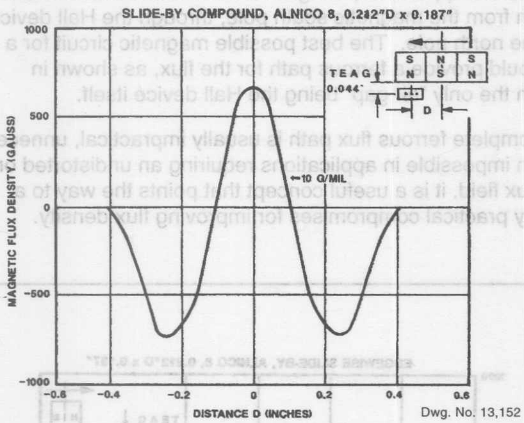

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FIGURE 50

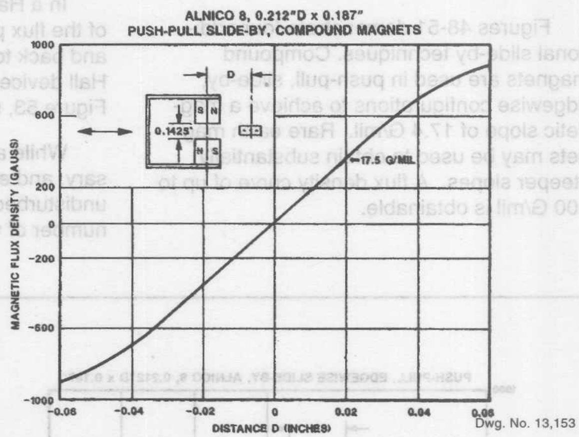

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FIGURE 51

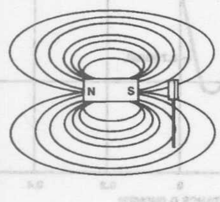
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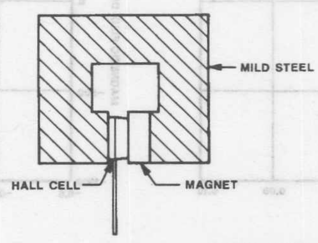
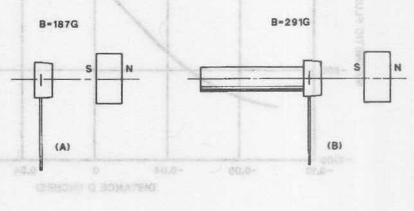
FIGURE 52



Dwg. No. 13,155

FIGURE 53



Dwg. No. 13,156

FIGURE 54

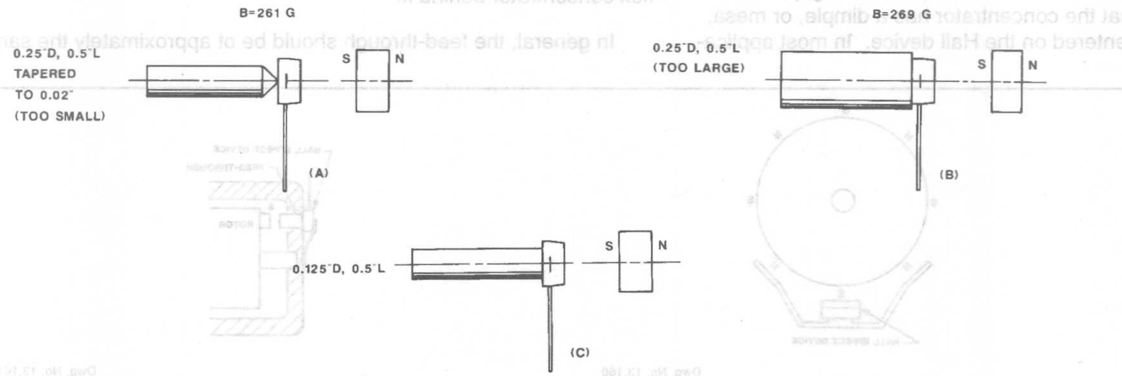
SIZE OF THE CONCENTRATOR

The active area of the Hall device is typically 0.01" square. Best results are obtained by tapering the end of the concentrator to approximately the same dimensions. With the "U" package, however, there is 0.044" from the active area to the rear surface of the package. Due to this 0.044" distance, a slightly larger end to the concentrator results in higher values of flux density at the active area. If the end is too large, the flux is insufficiently concentrated. Figure 55(A), (B), and (C) illustrates these effects using cylindrical flux concentrators and a 0.25" gap.

The length of the concentrator also has an effect on the flux density. This is illustrated in Figure 56.

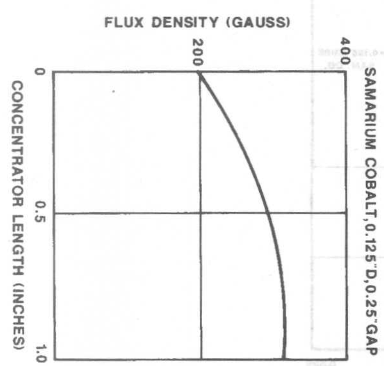
Cylindrical concentrators were used here for convenience, but the body of the concentrator has little effect. The important factors are the shape, position, and surface area of the magnet end nearest the Hall sensor.

The effectiveness of other concentrator configurations can be measured easily by using a calibrated linear Hall device, such as the UGN3503U, or a commercial gaussmeter.



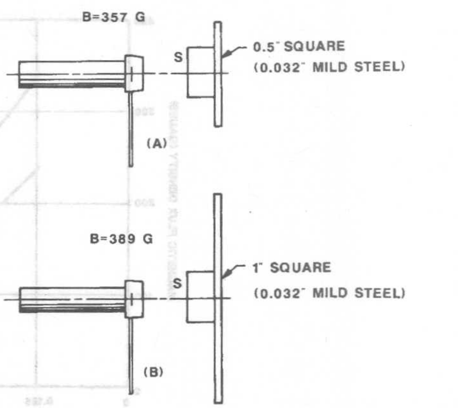
Dwg. No. 13,157

FIGURE 55



Dwg. No. 13,158

FIGURE 56



Dwg. No. 13,159

FIGURE 57

MOUNTING THE MAGNET TO A FERROUS PLATE

Mounting the magnet to a ferrous plate will give an additional increase in flux density at the Hall element. Using the same configuration as in Figure 55(C), which produced 291 G, note the available flux attained in Figure 57(A) and (B) with the addition of the ferrous plate.

Figure 58 shows a possible concentrator for a ring magnet application. Using a flux concentrator that extends to both of the adjacent north poles, flux density increases from 265 G to 400 G (0.015" air gap). Note that the concentrator has a dimple, or mesa, centered on the Hall device. In most applications, the mesa will give a significant increase in flux density over a flat mounting surface.

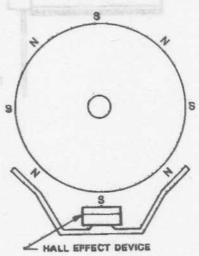
ATTRACTIVE FORCE AND DISTORTED FLUX FIELD

Whenever a flux concentrator is used, an attractive force exists between magnet and concentrator. That may be undesirable.

FEED-THROUGHS

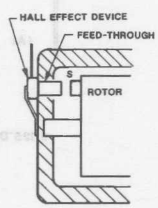
An example of the use of a magnetic conductor to feed flux through a nonferrous housing is shown in Figure 59. A small electric motor has a 0.125" cube samarium cobalt magnet mounted in the end of its rotor, as shown. A 0.125" cube ferrous conductor extends through the alloy case with a 0.031" air gap between it and the magnet's south pole. The Hall switch is mounted at the other end with a flux concentrator behind it.

In general, the feed-through should be of approximately the same



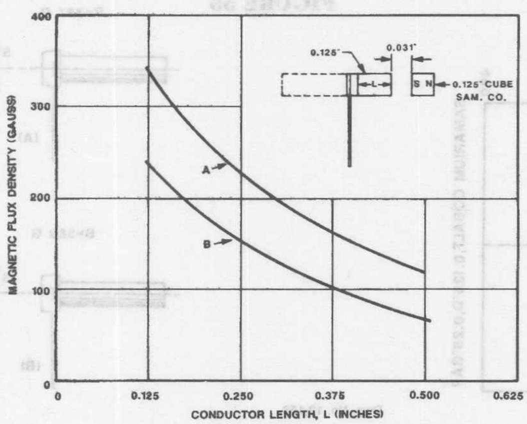
Dwg. No. 13,160

FIGURE 58



Dwg. No. 13,161

FIGURE 59



Dwg. No. 13,162

FIGURE 60

cross-sectional area and shape as is the magnet pole.

This concept can be used to feed flux through any non-ferrous material, such as a pump case, pipe, or panel.

The two curves of Figure 60 illustrate the effects on flux density of increasing the length of the feed-through, as well as the contribution by the flux concentrator behind the Hall switch. Values for curve A were obtained with the flux concentrator in place, those for curve B without it. In both cases, the highest flux densities were achieved with the shortest feed-through dimension L, which was 0.125". Peak flux density was 350 G with flux concentrator in place, 240 G without it.

MAGNET SELECTION

A magnet must operate reliably with the total effective air gap in the working environment. It must fit the available space. It must be mountable, affordable, and available.

FIGURES OF MERIT

The figures of merit commonly applied to magnetic materials are:

Residual Induction (B_r) in gauss: How strong is the magnetic field?

Coercive Force (H_c) in oersteds: How well will the magnet resist external demagnetizing forces?

Maximum Energy Product (BH_{max}) in gauss-oersteds times 10^6. A strong magnet that is also very resistant to demagnetizing forces has a high maximum energy product. Generally, the larger the energy product, the better, stronger, and more expensive the magnet.

Temperature Coefficient: The rate of change of the operate or elease point over temperature, measured in gauss per degree Celsius. How much will the strength of the magnet change as temperature changes?

MAGNETIC MATERIALS

Neodymium (Ne-Fe B)—The new neodymium-iron-boron alloys fill the need for a high maximum-energy product, moderately priced magnet material. The magnets are produced by either a powdered-metal technique called orient-press-sinter or a new process incorporating jet casting and conventional forming techniques. Current work is being directed toward reducing production costs, increasing operating temperature ranges and decreasing temperature coefficients. Problems relating to oxidation of the material can be overcome through the use of modern coatings technology. Maximum energy products range from 7.0 to 15.0 MGOe depending on the process used to produce the material.

Rare Earth—Cobalt is an alloy of a rare earth metal, such as samarium, with cobalt (abbreviated RE cobalt). These magnets are the best in all categories, but are also the most expensive by about the same margins. Too hard for machining, they must be ground if shaping is necessary. Maximum energy product, perhaps the best single measure of magnet quality, is approximately 16 x 10^6.

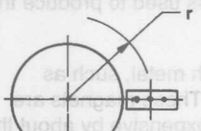
Alnico is a class of alloys containing aluminum, nickel, cobalt, iron, and additives that can be varied to give a wide range of properties. These magnets are strong and fairly expensive, but less so than RE cobalt. Alnico magnets can be cast, or sintered by pressing metal powders in a die and heating them. Sintered Alnico is well suited to mass production of small, intricately shaped magnets. It has more uniform flux density, and is mechanically superior. Cast Alnico magnets are generally somewhat stronger. The non-oriented or isotropic Alnico alloys (1, 2, 3, 4) are less expensive and magnetically weaker than the oriented alloys (5, 6, 5-7, 8, 9). Alnico is too hard and brittle to be shaped except by grinding. Maximum energy product ranges from 1.3 x 10^6 to 10 x 10^6.

Ceramic magnets contain barium or strontium ferrite (or another element from that group) in a matrix of ceramic material that is compacted and sintered. They are poor conductors of heat and electricity, are chemically inert, and have-high values of coercive force. As with Alnico, ceramic magnets can be fabricated with partial or complete orientation for additional magnetic strength. Less expensive than Alnico, they also are too hard and brittle to shape except by grinding. Maximum-energy product ranges from 1 x 10^6 to 3.5 x 10^6.

Cunife is a ductile copper base alloy with nickel and iron. It can be stamped, swaged, drawn, or rolled into final shape. Maximum energy product is approximately 1.4 x 10^6.

Iron-Chromium magnets have magnetic properties similar to Alnico 5, but are soft enough to undergo machining operations before the final aging treatment hardens them. Maximum energy product is approximately 5.25 x 10^6.

Plastic and rubber magnets consist of barium or strontium ferrite in a plastic matrix material. They are very inexpensive and can be formed in numerous ways including stamping, molding, and machining, depending upon the particular matrix material. Since the rubber used is synthetic, and synthetic rubber is also plastic, the distinction between the two materials is imprecise. In common practice, if a plastic magnet is flexible, it is called a rubber magnet. Maximum energy product ranges from 0.2 x 10^6 to 1.2 x 10^6.



$$B\ (GAUSS) \approx \frac{I\ (AMPS)}{4\ \pi\ r\ (INCHES)}$$

Dwg. No. 13,163

FIGURE 61

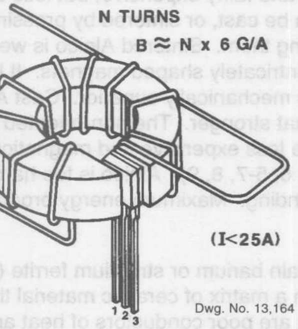


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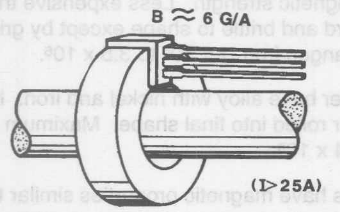
FIGURE 62(A)



Dwg. No. 13,165

FIGURE 62(B)

CHOOSING MAGNET STRENGTH

A magnet must have sufficient flux density to reach the Hall switch maximum operate point specification at the required air gap. Good design practice suggests the addition of another 50 G to 100 G for insurance and a check for sufficient flux at the expected temperature extremes.

If the Hall switch data sheet specifies a 350 G maximum operate point at +25°C. After adding a pad of 100 G, we have 450 G at +25°C. If operation to +70°C is needed, the requirement is 450 G + 45 G = 495 G. (For calculations, we use 0.7 G/°C operate point coefficient and 1 G/°C release point coefficient.) Since the temperature coefficient of most magnets is negative, this factor would also require some extra flux at room temperature to guarantee high-temperature operation.

COERCIVE FORCE

Coercive force becomes important if the operating environment will subject the magnet to a strong demagnetizing field, such as that encountered near the rotor of an ac motor. For such applications, a permanent magnet with high coercive force (ceramic, Alnico 8, or, best of all, RE cobalt) is clearly indicated.

PRICE AND PEAK ENERGY PRODUCT

The common permanent magnet materials and their magnetic properties are summarized in Table 4. The cost column shows the relationship between the price paid for a magnet and its peak energy product.

CURRENT LIMITING AND MEASURING

CURRENT SENSORS

Hall effect devices are excellent current-limiting or measuring sensors. Their response ranges from dc to the kHz region. The conductor need not be interrupted in high-current applications.

The magnetic field about a conductor is normally not intense enough to operate a Hall effect device (Figure 61).

The radius, r, is measured from the center of the conductor to the active area of the Hall device. With a radius of 0.5" and a current of 1,000 A, there would be a magnetic flux density of 159 G at the Hall device. At lower current, use a toroid or closed magnetic circuit to increase the flux density, as illustrated in Figure 62(A) and (B).

With a 0.06" air gap for the "U" package, there would be 6 G/A per turn for Figure 62(A), and 6 G/A for Figure 62(B).

The core material can be of either ferrite or mild steel (C-1010) for low-frequency applications, and ferrite for high-frequency measurements.

The main concerns are:

That the core retains minimal field when the current is reduced to zero.

That the flux density in the air gap is a linear function of the current.

And that the air gap is stable over the operating temperaturerange.

The cross-sectional dimensions of the core are at least twice the air gap dimension to ensure a reasonably homogeneous field in the gap. For example, a toroid with a 0.06" gap would have at least a 0.12" x 0.12" cross-section.

Another simple and inexpensive application is illustrated in Figure 63. A toroid of the appropriate diameter is formed from mild steel stock, 0.0625" thick and 0.1875" wide. The ends are formed to fit on each side of the central portion of the Hall device. One advantage of this technique is that the toroid can be placed around a conductor without disconnecting the conductor.

MULTI-TURN APPLICATIONS

There are several considerations in selecting the number of turns for a toroid such as the one in Figure 62(A):

Hall Switches

Keep the flux density in the 100 G to evices can be supplied with a narrow distribution of magnetic parameters within this range. If, for example, you want the Hall switch to turn ON at 10 A:

$$N = \frac{300\ \text{G}}{6\ \text{G/A} \times 10\ \text{A}} = 5\ \text{turns}$$

Hall Linears

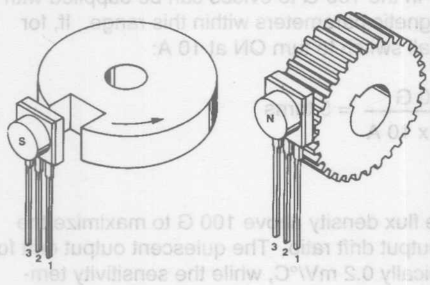
It is desirable to have flux density above 100 G to maximize the output signal/quiescent output drift ratio. The quiescent output drift for ratiometric sensors is typically 0.2 mV/°C, while the sensitivity tem-

TABLE 4
Properties of Magnetic Materials

Material	Maximum Energy Product (Gauss-Oersted)	Residual Induction (Gauss)	Coercive Force (Oersteds)	Temperature Coefficient	Cost	Comments
R.E. Cobalt	16×10^6	8.1×10^3	7.9×10^3	-0.05%/°C	Highest	Strongest, smallest, resists demagnetizing best
Alnico 1, 2, 3, 4	$1.3 - 1.7 \times 10^6$	$5.5 - 7.5 \times 10^3$	$0.42 - 0.72 \times 10^3$	-0.02%/°C to -0.03%/°C	Medium	Non-oriented
Alnico 5, 6, 5-7	$4.0 - 7.5 \times 10^6$	$10.5 - 13.5 \times 10^3$	$0.64 - 0.78 \times 10^3$	-0.02%/°C to -0.03%/°C	Medium-High	Oriented
Alnico 8	$5.0 - 6.0 \times 10^6$	$7 - 9.2 \times 10^3$	$1.5 - 1.9 \times 10^3$	-0.01%/°C to +0.01%/°C	Medium-High	Oriented, high coercive force, best temperature coefficient
Alnico 9	10×10^6	10.5×10^3	1.6×10^3	-0.02%/°C	High	Oriented, highest energy product
Ceramic 1	1.0×10^6	2.2×10^3	1.8×10^3	-0.2%/°C	Low	Non-oriented, high coercive force, hard, brittle, non-conductor
Ceramic 2, 3, 4, 6	$1.8 - 2.6 \times 10^6$	$2.9 - 3.3 \times 10^3$	$2.3 - 2.8 \times 10^3$	-0.2%/°C	Low-Medium	Partially oriented, very high coercive force, hard, brittle, non-conductor
Ceramic 5, 7, 8	$2.8 - 3.5 \times 10^6$	$3.5 - 3.8 \times 10^3$	$2.5 - 3.3 \times 10^3$	-0.2%/°C	Medium	Fully oriented, very high coercive force, hard, brittle, non-conductor
Cunife	1.4×10^6	5.5×10^3	0.53×10^3	—	Medium	Ductile, can cold form and machine
Fe-Cr	5.25×10^6	13.5×10^3	0.60×10^3	—	Medium-High	Can machine prior to final aging treatment
Plastic	$0.2 - 1.2 \times 10^3$	$1.4 - 3 \times 10^3$	$0.45 - 1.4 \times 10^3$	-02%/°C	Lowest	Can be molded, stamped, machined
Rubber	$0.35 - 1.1 \times 10^6$	$1.3 - 2.3 \times 10^3$	$1 - 1.8 \times 10^3$	-0.2%/°C	Lowest	Flexible
Neodymium	$7 - 15 \times 10^6$	$6.4\ 11.75 \times 10^3$	$5.3 - 6.5 \times 10^3$	-.157%/°C to -.192%/°C	Medium-High	Non-oriented

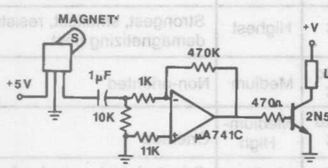
perature coefficient is typically 0.02%/°C.

For low-current applications in which many turns are required, one can wind a bobbin, slip it over a core, and complete the magnetic circuit through the Hall device with a bracket-shaped pole piece, as shown in Figure 64.



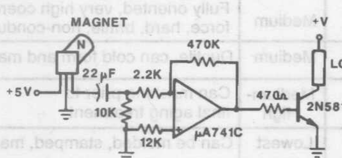
Dwg. No. 13,168

FIGURE 65



Dwg. No. 13,169

FIGURE 66



Dwg. No. 13,170

FIGURE 67

With this bobbin-bracket configuration, it is possible to measure currents in the low milliampere range or to replace a relay using a Hall switch. To activate a Hall switch at 10 mA (±20%), using a device with a 200 G (±40 G) operate point, bobbin windings require:

$$N = \frac{200\ \text{G}}{6\ \text{G/A} \times 0.01\ \text{A}} = 3333\ \text{turns}$$

It would be practical to tweak the air gap for final, more precise calibration. In all cases, *be careful not to stress the package.*

OTHER APPLICATIONS FOR LINEAR SENSORS

Hall Effect linear sensors are used primarily to sense relatively small changes in magnetic field—changes too small to operate a Hall Effect switching device. They are customarily capacitively coupled to an amplifier, which boosts the output to a higher level.

As motion detectors, gear tooth sensors, and proximity detectors (Figure 65), they are magnetically driven mirrors of mechanical events. As sensitive monitors of electromagnets, they can effectively measure a system's performance with negligible system loading while providing isolation from contaminated and electrically noisy environments.

Each Hall effect integrated circuit includes a Hall sensing element, linear amplifier, and emitter-follower output stage. Problems associated with handling tiny analog signals are minimized by having the Hall cell and amplifier on a single chip.

The output null voltage is nominally one-half the supply voltage. A south magnetic pole presented to the branded face of the Hall effect sensor will drive the output higher than the null voltage level. A north magnetic pole will drive the output below the null level.

In operation, instantaneous and proportional output-voltage levels are dependent on magnetic flux density at the most sensitive area of the device. Greatest sensitivity is obtained with the highest supply voltage allowed, but at the cost of increased supply current and a slight loss of output symmetry. The sensor's output is usually capacitively coupled to an amplifier that boosts the output above the millivolt level.

In the two applications shown in Figures 66 and 67, permanent bias magnets are attached with epoxy glue to the back of the epoxy packages. The presence of ferrous material at the face of the package then acts as a flux concentrator.

The south pole of a magnet is attached to the back of the package if the Hall effect IC is to sense the presence of ferrous material. The north pole of a magnet is attached to the back surface if the integrated circuit is to sense the absence of ferrous material.

Calibrated linear Hall devices, which can be used to determine the

actual flux density presented to the sensor in a particular application, are available.

FERROUS METAL DETECTORS

Two similar detector designs are illustrated in Figures 68 and 69. The first senses the presence of a ferrous metal; the other senses an absence of the metal. The two sensing modes are accomplished simply by reversing the magnet poles relative to the sensor. The pole of the magnet is affixed to the unbranded side of the sensor in both cases.

Frequency response characteristics of this circuit are easily controlled by changing the value of the input decoupling capacitor for the low-frequency break-point. If high-frequency attenuation is desired, a capacitor can be used to shunt the feedback resistor.

METAL SENSOR

The north pole of the magnet is affixed to the back side of a linear sensor. The sensor is in contact with the bottom of a 0.09375" epoxy board. An output change (decrease) is produced as a 1" steel ball rolls over the sensor. This signal is amplified and inverted by the µA741C operational amplifier and drives the 2N8512 ON.

NOTCH SENSOR

The south pole of the magnet is fixed to the backside of a linear sensor. The sensor is 0.03125" from the edge of a steel rotor. A 0.0625" wide by 0.125' deep slot in the rotor edge passing the sensor causes an output change (decrease). This signal is amplified and inverted by the µA741C op amp and drives the 2N5812 ON.

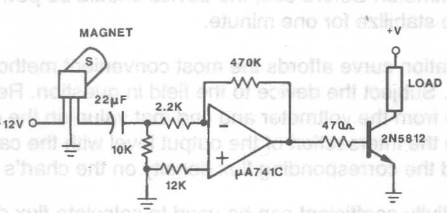


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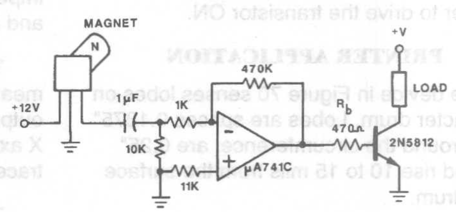
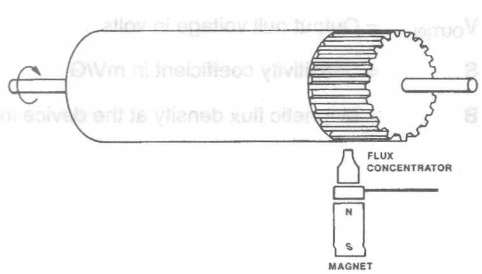
FIGURE 68



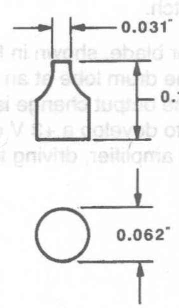
Dwg. No. 13,172

FIGURE 69



Dwg. No. 13,173

FIGURE 70



Dwg. No. 13,174

FIGURE 71

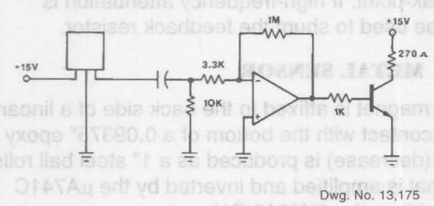


FIGURE 72

Note that, in both examples, the branded side of the sensor faces the material (or lack of material) to be sensed. In both cases, the presence (or absence) of the ferrous metal changes the flux density at the Hall Effect sensor so as to produce a negative going output pulse. The pulse is inverted by the amplifier to drive the transistor ON.

PRINTER APPLICATION

The device in Figure 70 senses lobes on a character drum. Lobes are spaces 0.1875" apart around the circumference, are 0.25" long and rise 10 to 15 mils from the surface of the drum.

A Hall effect linear IC sensor is used with an Indiana General Magnet Products Company SR8522 magnet. The north pole is affixed to the reverse side of the package. A flux concentrator is affixed to the branded face. Though it does not provide a flux return path, a concentrator will focus the magnetic field through the switch.

The concentrator blade, shown in Figure 71, is aligned with the drum lobe at an air gap distance of 0.01". The output change is amplified as shown to develop a +3 V output from the operational amplifier, driving the transistor ON, as illustrated in Figure 72.

Sensitivity is so great in this configuration that the output signal's baseline quite closely tracks eccentricities in the drum. This affects lobe resolution, but lobe position can still be measured.

USING CALIBRATED DEVICES

The calibrated linear sensor is an accurate, easy-to-use tool for measuring magnetic flux densities. Each device is individually calibrated and furnished with a calibration curve and sensitivity coefficient. Although calibration is performed in a south and north 800 G field, the sensor is useful for measuring fields in both polarities.

A closely regulated (±10 mV) power supply is necessary to preserve accuracy in calibrated flux measurements. An ambient temperature range of 21°C to 25°C must also be maintained.

Connect Pin 1 to voltage V_{CC}, Pin 2 to ground, and Pin 3 to a high-impedance voltmeter. Before use, the device should be powered-up and allowed to stabilize for one minute.

The calibration curve affords the most convenient method of flux measurement. Subject the device to the field in question. Read the output voltage from the voltmeter and find that value on the chart X axis. Locate the intersection of the output level with the calibration trace and read the corresponding flux density on the chart's Y axis.

The sensitivity coefficient can be used to calculate flux densities somewhat more precisely. First, determine the null output voltage of the device under 0 G or null field condition. Then, read the output of the device under an applied field condition by subjecting it to the flux in question. Magnetic flux density at the device may be calculated by:

$$B = \Delta V_{OUT(B)} - V_{OUT(0)} * 1000/S$$

where

$\Delta V_{OUT(B)}$ = Output voltage under applied field in volts.

$V_{OUT(0)}$ = Output null voltage in volts.

S = Sensitivity coefficient in mV/G.

B = Magnetic flux density at the device in gauss.

GLOSSARY

Active Area — The site of the Hall element on the encapsulated IC chip.

Air Gap — The distance from the face of the magnetic pole to the face of the sensor.

Ampere-turn (NI) — The mks unit of magnetomotive force.

Ampere-turns/meter (NI/m) — The mks unit of magnetizing force. One ampere turn per meter equals 79.6 oersteds.

Bipolar — A method of operating a Hall sensor using both north and south magnetic poles.

Coercive Force (H_c) — The demagnetizing force that must be applied to reduce the magnetic flux density in a magnetic material to zero. Measured in oersteds.

Concentrator — Any ferrous metal used to attract magnetic lines of force.

Gauss (G) — The CGS unit of magnetic flux density. Equivalent to one maxwell per square centimeter (Mx/cm^2). One gauss equals 10^{-4} tesla.

Gilbert — The CGS unit of magnetomotive force.

Head-On — A method by which the Hall sensor is actuated. The magnetic field is increased and decreased by moving the magnetic pole toward and away from the sensor face.

Maximum Energy Product (BH_{max}) — The highest product of B and H from the demagnetization curve of a magnetic material. Given in gauss-oersteds x 10^6 (MGOe).

Maxwell (Mx) — The CGS unit of total magnetic flux. One maxwell equals 10^{-8} webers.

Oersteds (Oe) — The CGS unit of magnetizing force. Equivalent to gilberts per centimeter (Gilberts/cm). One oersted equals 125.7 ampere-turns per meter.

Remanent Induction (B_d) — The magnetic induction that remains in a magnetic circuit after removal of an applied magnetomotive force. When there is no air gap in the magnetic circuit, remanent and residual induction are equal. With an air gap, remanence will be less than residual induction. Measured in gauss.

Residual Induction (B_r) — The flux density remaining in a closed magnetic circuit of magnetic material when the magnetizing force adequate to saturate the material is reduced to zero. Measured in gauss.

Slide-by — A method which a Hall sensor is actuated. The magnetic field is increased and decreased as a permanent magnet is moved laterally past the sensor face.

Tesla (T) — The mks unit of magnetic flux density. Equivalent to one weber per square meter (Wb/m^2). One tesla equals 10^4 gauss.

Toroid — A doughnut-shaped ring often composed of iron, steel or ferrite.

Total Effective Air Gap (TEAG) — The distance from the face of a magnetic pole to the active area of a Hall Effect sensor.

Unipolar — A method of operating a Hall sensor using a single magnetic pole, usually the south pole.

Vane — Any ferrous metal used to shunt a magnetic field away from the Hall sensor (at least 1.5 times the width of an associated magnet).

Window — An opening in a vane at least 1.5 times the width of an associated magnet.

SOURCES FOR FERRITE TOROIDS AND MAGNETS

As a convenience, some sources for ferrite toroids and magnets are listed below.
Addresses and telephone numbers are correct to the best of our knowledge at time of printing.

TOROID SUPPLIERS

J.W. Miller Co.
Division of Bell Industries
19070 Reyes Avenue
P.O. Box 5825
Rancho Dominguez, CA 90224
213/537-5200

Fair-Rite Products Corp.
P.O. Box J
Wallkill, NY 12589-0288
914/895-2055

Magnetics
900 East Butler Road
P.O. Box 391
Butler, PA 16001
412/282-8282

Dexter Magnetic Materials Division
10 Fortune Drive
Billerica, MA 01865
508/663-7500

Neosid Inc.
28 Main Street
Eatontown, NJ 07724
201/389-4411

Ferrox/Division of Amperex Corp.
5083 Kings Highway
Saugerties, NY 12477
914/246-2811

MAGNET SUPPLIERS

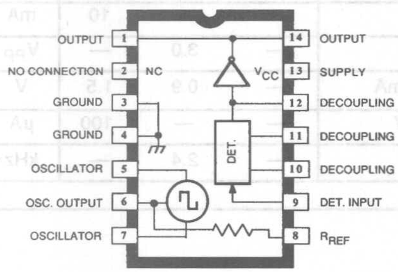
MAGNET SUPPLIERS	Types
Arnold Engineering P.O. Box G Marengo, IL 60152 815/568-2000	Alnico, Ceramic, Multipole Ring
Bunting Magnetics Company 1165 Howard St. Elk Grove Village, IL 60007 312/593-2060	Alnico, Ceramic, Plastic
Ceramic Magnetics, Inc. 87 Fairfield Road Fairfield, NJ 07006 201/227-4222	Ceramic, Multipole Ring
Crucible Magnetics 101 Magnet Dr. Elizabethtown, NJ 42701 502/769-1333	Alnico, Rare Earth
Hitachi Magnetics 7800 Neff Road Edmore, MI 48829 517/427-5151	Alnico, Ceramic, Rare Earth
IG Technolog 405 Elm Street Valparaiso, IN 46383 219/462-3131	Alnico, Ceramic, Multipole Ring, Rare Earth
Ogallala Electronics P.O. Box 59 Ogallala, NE 69153 308/284-4093	Ceramic, Multipole Ring
Dexter Magnetic Materials Division 400 Karin Lane Hicksville, NY 11801 516/822-3311	Representatives of various manufacturers. Dexter Magnetic also does custom grinding.
Recoma, Inc. 2 Stewart Place Fairfield, NJ 07006 201/575-6970	Rare Earth
Stackpole Carbon Co. Magnet Division 700 Elk Ave. Kane, PA 16735 814/837-7000	Ceramic, Flexible Plastic
TDK Corporation of America Head Office 1600 Feehanville Drive Mount Prospect, IL 60056 312/803-6100	Rare Earth
The Electrodyne Company 4188 Taylor Road Batavia, OH 45103 513/732-2822	Plastic
Xolox Corporation 6932 Gettysburg Pike Ft. Wayne, IN 46804 219/432-0661	Plastic, Multipole Ring
3-M Plastiform 3-M Center Industrial Electric Products Div. Building 225-4N St. Paul, MN 55144 Attn: James Fenwick 800/328-1373	Plastic
Magnaquench Div. of Gen. Motors 6435 S. Scatterfield Rd. Anderson, IN 46011 317/646-2763	Neodymium
Dynacast Co. 921 Albion Ave. Schaumburg, IL 60193 312/351-6100	

SECTION 5. TECHNICAL DATA FOR AUTOMOTIVE POWER & SIGNAL-PROCESSING ICs

2429

27461

FLUID DETECTOR



Dwg. No. PS - 017

Primarily designed for use as an automotive low coolant detector, the ULN2429A monolithic bipolar integrated circuit is ideal for detecting the presence or absence of many different types of liquids in automotive, home, or industrial applications. Especially useful in harsh environments, reverse voltage protection, internal voltage regulation, temperature compensation, and high-frequency noise immunity are all incorporated in the design.

A simple probe, immersed in the conductive fluid being monitored, is driven with an ac signal to prevent plating problems. The presence, absence, or condition of the fluid is determined by comparing the loaded probe resistance with an internal (pin 8) or external (pin 6) resistance. Typical conductive fluids which can be sensed are tap water, sea water, weak acids and bases, wet soil, wine, beer, and coffee.

The high-current output is typically a square wave signal for use with an LED, incandescent lamp, or loudspeaker. A capacitor can be connected (pin 12) to provide a dc output for use with inductive loads such as relays and solenoids.

These devices are furnished in an improved 14-lead dual in-line plastic package with a copper alloy lead frame for superior thermal characteristics. However, in order to realize the maximum current-handling capability of these devices, both of the output pins (1 and 14) and both ground pins (3 and 4) should be used.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}
- (continuous) . . . . -50 V to +16 V
- (1 hr. at +25°C) . . . . 24 V
- (10 μs) . . . . 50 V

Output Voltage, V_{OUT} . . . . 30 V

Output Current, I_{OUT}
- (continuous) . . . . 700 mA
- (1 hr. at +25°C) . . . . 1.0 A

Package Power Dissipation, P_D . . . 1.33 W*

Operating Temperature Range,
- T_A . . . . -40°C to +85°C

Storage Temperature Range,
- T_S . . . . -65°C to +150°C

* Derate at the rate of 16.67 mW/°C above T_A= +70°C.

FEATURES

- High Output Current
- AC or DC Output
- Single-Wire Probe
- Low External Parts Count
- Internal Voltage Regulator
- Reverse Voltage Protection

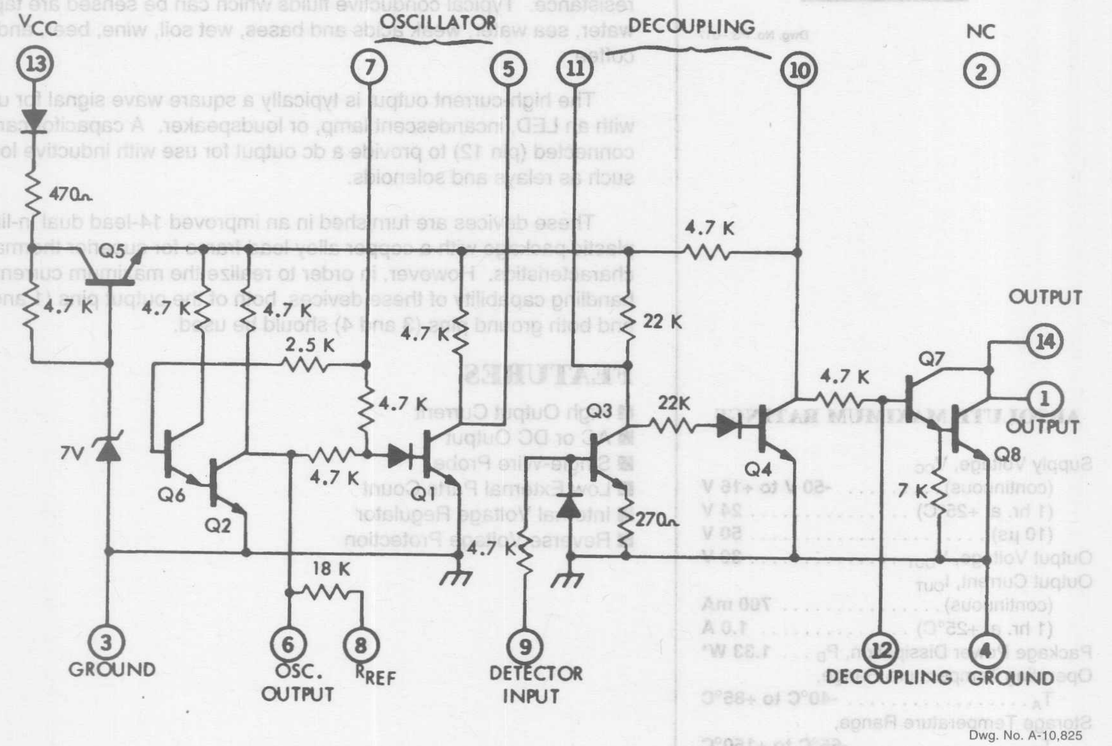
Always order by complete part number: ULN2429A

2429
FLUID DETECTOR

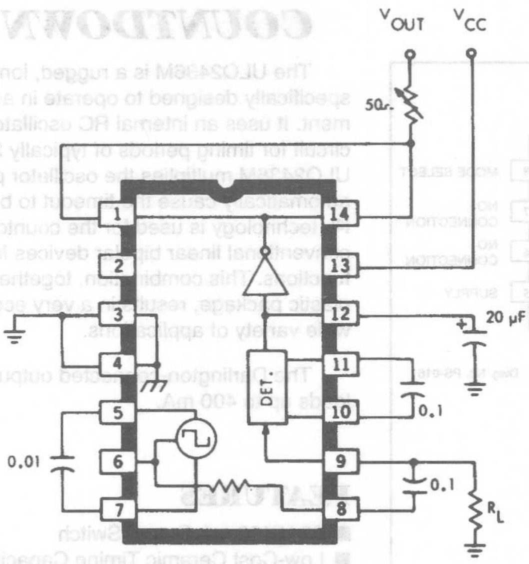
ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = V_{OUT} = 12 V (UNLESS OTHERWISE SPECIFIED).

Characteristic	Symbol	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	13	Operating	10	—	16	V
Supply Current	I_{CC}	13	V_{CC} = 16 V	—	—	10	mA
Oscillator Output Voltage	V_{OSC}	6	R_L = 18 kΩ	—	3.0	—	V_{PP}
Output ON Voltage	V_{OUT}	1, 14	$R_L \geq$ 30 kΩ, I_{OUT} = 500 mA	—	0.9	1.5	V
Output OFF Current	I_{OUT}	1, 14	$R_L \leq$ 10 kΩ, V_{OUT} = 30 V	—	—	100	μA
Oscillator Frequency	f_{OSC}	6	R_L = 18 kΩ	—	2.4	—	kHz

CIRCUIT SCHEMATIC

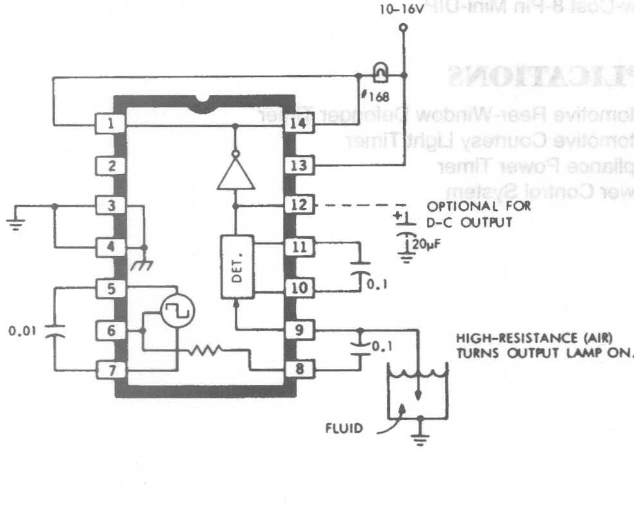


TEST CIRCUIT

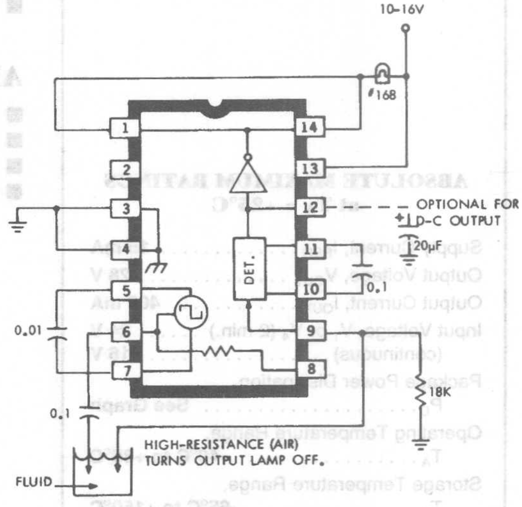


Dwg. No. A-10,707

TYPICAL APPLICATIONS



Dwg. No. A-10,706

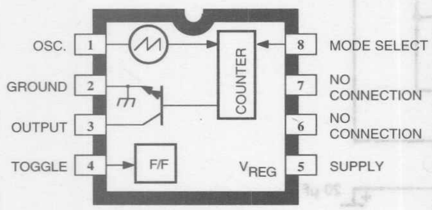


Dwg. No. A-10,711

2436

27462.20A

COUNTDOWN POWER TIMER



Dwg. No. PS-016

The ULQ2436M is a rugged, long-duration countdown timer specifically designed to operate in an automotive or industrial environment. It uses an internal RC oscillator to drive a digital countdown circuit for timing periods of typically 2-1/2 to 5 minutes. The ULQ2436M multiplies the oscillator period by 4064. Internal logic can automatically cause the timeout to be halved for successive timeouts. I^2L technology is used for the countdown and logic circuitry and conventional linear bipolar devices for the oscillator and output power functions. This combination, together with the low-cost 8-pin mini-DIP plastic package, results in a very economical power timer suitable for a wide variety of applications.

The Darlington-connected output driver is capable of switching loads up to 400 mA.

FEATURES

- 28 V/400 mA Output Switch
- Low-Cost Ceramic Timing Capacitor
- Dual-Mode Timing Operation
- -40°C to +85°C Operation
- 10 V to 16 V Operation
- Internal Stabilizing Regulator
- Low-Cost 8-Pin Mini-DIP

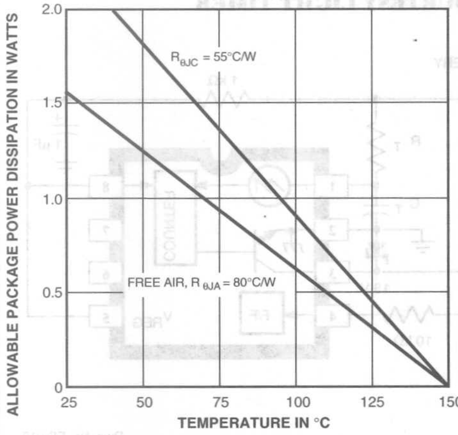
APPLICATIONS

- Automotive Rear-Window Defogger Timer
- Automotive Courtesy Light Timer
- Appliance Power Timer
- Power Control System

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

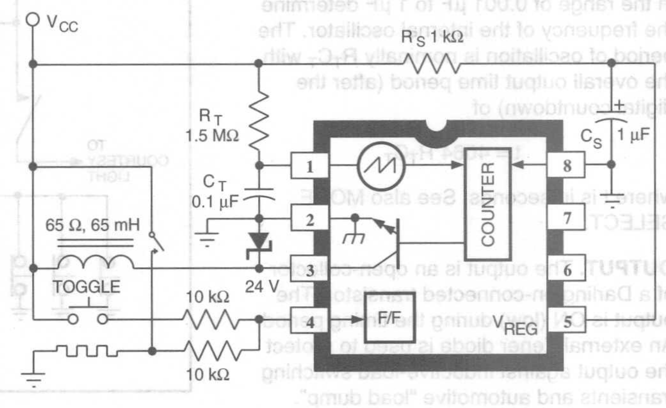
Supply Current, I_{REG}	**15 mA**
Output Voltage, V_{OUT}	**28 V**
Output Current, I_{OUT}	**400 mA**
Input Voltage, V_1 or V_4 (2 min.)	**24 V**
(continuous)	**16 V**
Package Power Dissipation, P_D	**See Graph**
Operating Temperature Range, T_A	**-40°C to +85°C**
Storage Temperature Range, T_S	**-65°C to +150°C**

Always order by complete part number: **ULQ2436M**



Dwg. GP-009-1B

TEST CIRCUIT AND TYPICAL REAR-WINDOW DEFOGGER APPLICATION



Dwg. ES-012A

ELECTRICAL SPECIFICATIONS at T_A = -40°C to +85°C, V_{CC} = 12 V (unless otherwise specified).

Characteristic	Test Conditions	Limits Min.	Limits Max.	Units
Regulator Voltage	I_{REG} = 12 mA, Output Off	7.0	9.0	V
Output Saturation Voltage	I_{OUT} = 400 mA, T_A = +25°C	—	2.5	V
	I_{OUT} = 250 mA, T_A = +25°C	—	1.35	V
Output Leakage Current	V_{OUT} = 28 V, V_{CC} = 12 V	—	100	µA
	V_{OUT} = 22 V, V_{CC} = Open Circuit	—	100	µA
Input Threshold Voltage	10 kΩ Series Resistor	1.0	5.0	V
Oscillator Tolerance	T_A = +25°C	—	±3.0	%
	T_A = -40°C to +85°C	—	±6.0	%
Divider Count (V_{CC} = 10 V to 16 V)	Initial Timeout	4064	4064	—
	Subsequent Timeouts	2032	2032	—

2436
COUNTDOWN POWER TIMER

CIRCUIT DESCRIPTION

OSC. An external resistor in the range of 200 kΩ to 2 MΩ and an external capacitor in the range of 0.001 μF to 1 μF determine the frequency of the internal oscillator. The period of oscillation is nominally R_TC_T with the overall output time period (after the digital countdown) of

$$t = 4064\ R_TC_T$$

where t is in seconds. See also MODE SELECT.

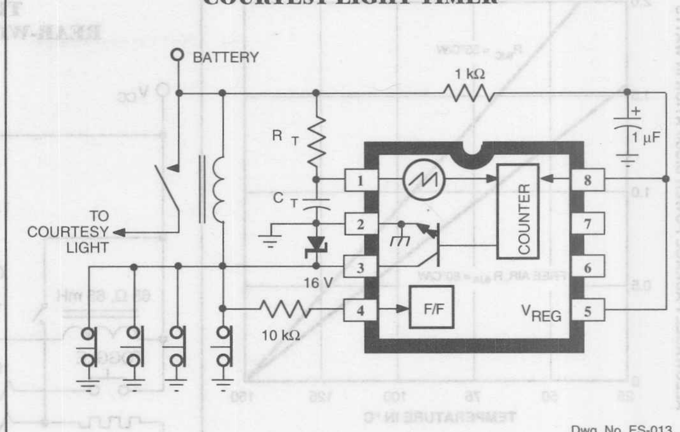
OUTPUT. The output is an open-collector of a Darlington-connected transistor. The output is ON (low) during the timing period. An external Zener diode is used to protect the output against inductive-load switching transients and automotive "load dump".

TOGGLE. A push-button, momentary-action switch at this input toggles the timer from the OFF to the ON state. The oscillator and countdown circuitry are started on the rising edge of the input pulse. Internal de-bounce circuitry is included.

SUPPLY. The timer requires a supply current applied to this pin through a current-limiting resistor (R_S). An internal 8 volt Zener diode shunt regulator provides a stable supply to the device over wide supply voltage variations. Capacitor C_S is used to provide decoupling.

MODE SELECT. With MODE SELECT connected to GROUND, the first activation will run for the preset time delay. All activations after the first will time out at half of the initial preset time. This sequence is reset each time the supply is interrupted. With MODE SELECT connected to SUPPLY (V_{REG}), the timer will repeat the preset time delay each time it is activated.

COURTESY LIGHT TIMER



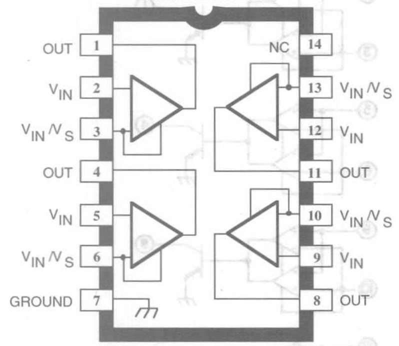
Dwg. No. ES-013

2454 AND 2455

27460.10A

AUTOMOTIVE LAMP MONITORS

ULN2455A



Dwg. No. PS-013

Capable of monitoring all types of automotive lamps, the ULN2454L, ULQ2454M, and ULN2455A lamp monitors provide multiple LED outputs to pinpoint the area in which a lamp has failed. The ULN2455A is a quad comparator capable of monitoring eight individual lamps or groups of lamps. The ULN/UL2454L/M are dual comparators featuring an additional output to trigger an alarm if either of the comparators detects a lamp failure. This output can be used to drive an audible signaling device or centrally located warning indicator. All devices can be used to monitor lamps, multiple low-voltage power supplies, or, with appropriate sensors, industrial processes.

Installation and operation of these lamp monitors has no effect on normal lamp operation. Comparators sense the normal voltage drop in the lamp wiring (approximately 20 mV) for each of the monitored lamp circuits. Little additional wiring is necessary for installation because the system can be completely integral to the wiring assembly. No standby power is required...the operating voltage is obtained from the sense leads; the system is energized only when the lamps are turned ON.

All devices are designed for use in the severe automotive environment. Lateral PNP transistors provide high-frequency noise immunity and differential transient-voltage protection. Reverse voltage protection, internal regulators, and temperature compensation are all embodied in the circuit designs. A failure within a device will not affect lamp operation.

These versatile lamp monitors are packaged in 14-pin plastic DIPs (suffix A), 8-lead surface-mountable SOICs (suffix L), or 8-pin mini-DIPs (suffix M) and are rated for operation over the temperature range of -40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Supply Voltage, V_{CC} . . . . **30 V**
Peak Supply Voltage, V_{CC}(100 ms) . . **80 V**
Peak Reverse Voltage, V_R . . . . **30 V**
Output Current, I_{OUT} . . . . **35 mA**
Package Power Dissipation, P_D **See Graph**
Operating Temperature Range,
T_A . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

FEATURES

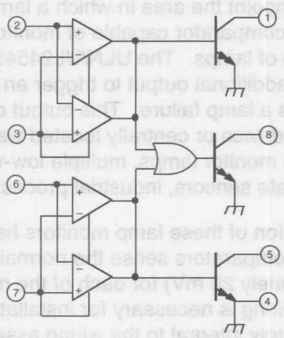
- No Standby Power
- Integral to Wiring Assembly
- Internal Transient Protection
- Fail-Safe
- Reverse Voltage Protected
- DIP or SOIC Plastic Packages

Always order by complete part number:

Part Number	Function	Style
ULN2454L	Dual Comparator with OR Output	8-Lead SOIC
UL2454M	Dual Comparator with OR Output	8-Pin Mini-DIP
ULN2455A	Quad Comparator	14-Pin DIP

PIN OUT & FUNCTIONAL BLOCK DIAGRAMS

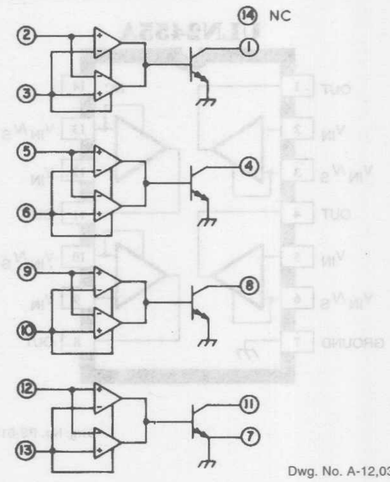
ULN2454L and ULQ2454M



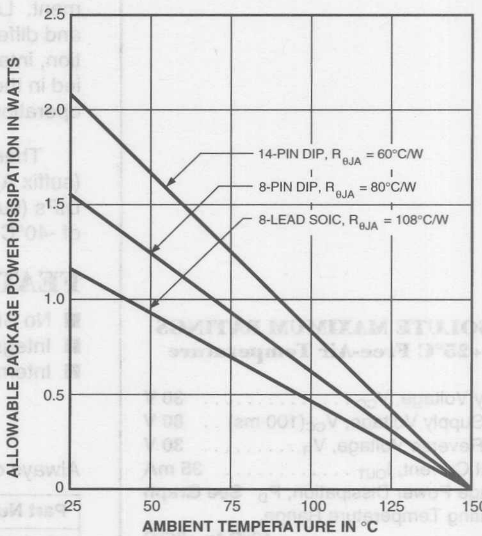
Dwg. No. FS-010A

Note that the dual in-line package and the small-outline IC package are electrically identical and share a common pin number assignment.

ULN2455A

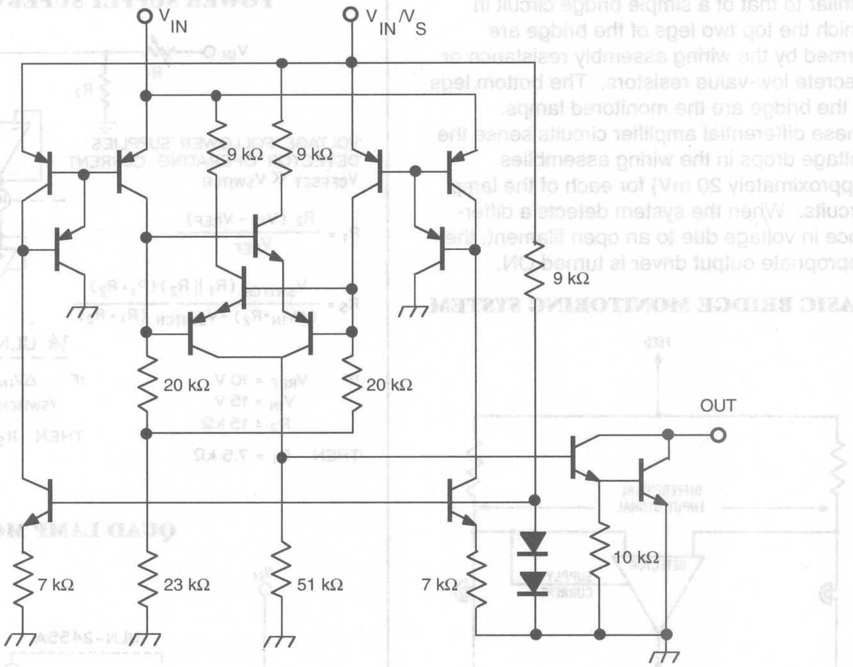


Dwg. No. A-12,033A



Dwg. No. GS-008-1A

SIMPLIFIED SCHEMATIC
(SINGLE DIFFERENTIAL SENSE AMPLIFIER)



Dwg. No. ES-011

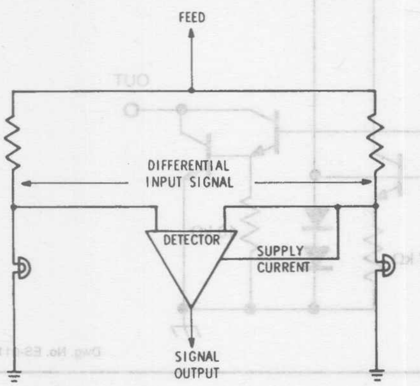
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{IN} = 10 to 16 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V, ΔV_{IN} < 7 mV	—	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 5 mA, ΔV_{IN} > 20 mV	—	0.8	1.0	V
		I_{OUT} = 30 mA, ΔV_{IN} > 20 mV	—	1.4	2.0	V
Differential Switch Voltage	ΔV_{IN}	V_{IN}-V_{IN}/V_S	7.0	13	20	mV
Input Current	I_{IN}	ΔV_{IN} = V_{IN}-V_{IN}/V_S = +30 mV	150	300	800	µA
	I_{IN}/I_S	ΔV_{IN} = V_{IN}-V_{IN}/V_S = -30 mV	0.5	1.7	3.5	mA

PRINCIPLE OF OPERATION

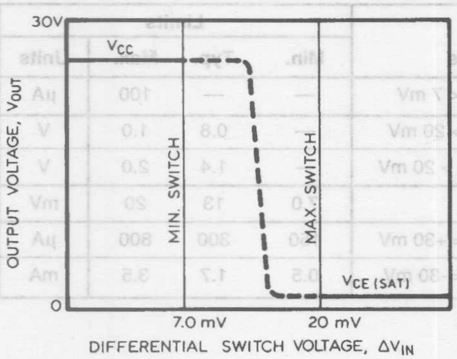
Operation of these lamp monitors is similar to that of a simple bridge circuit in which the top two legs of the bridge are formed by the wiring assembly resistance or discrete low-value resistors. The bottom legs of the bridge are the monitored lamps. These differential amplifier circuits sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

BASIC BRIDGE MONITORING SYSTEM



Dwg. No. A-11,473A

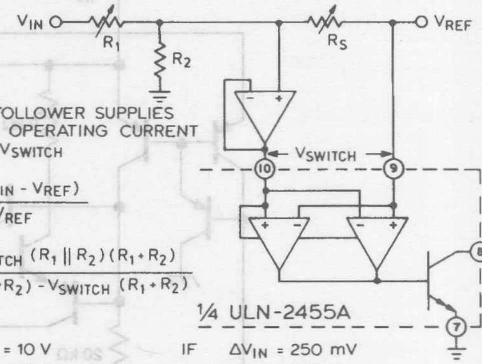
TYPICAL SWITCH CHARACTERISTICS



Dwg. No. A-12,187

TYPICAL APPLICATIONS

POWER SUPPLY SUPERVISORY CIRCUIT



VOLTAGE FOLLOWER SUPPLIES DETECTOR OPERATING CURRENT
$V_{OFFSET} \ll V_{SWITCH}$

$$R_1 = \frac{R_2\ (V_{IN} - V_{REF})}{V_{REF}}$$

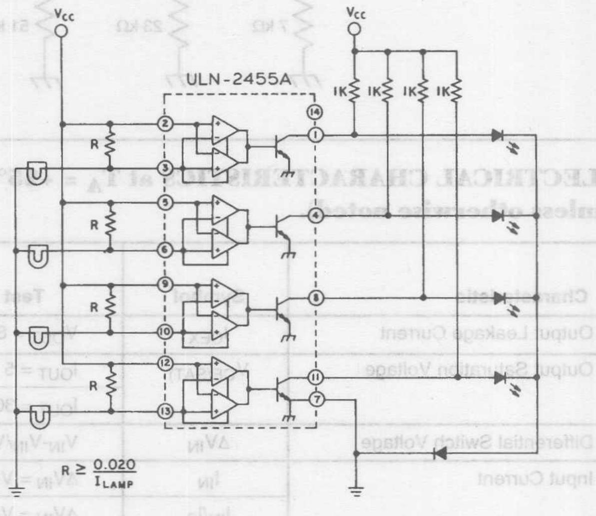
$$R_S = \frac{V_{SWITCH}\ (R_1 \parallel R_2)(R_1 + R_2)}{(\Delta V_{IN} \cdot R_2) - V_{SWITCH}\ (R_1 + R_2)}$$

IF $V_{REF} = 10$ V, $V_{IN} = 15$ V, $R_2 = 15\ k\Omega$
THEN $R_1 = 7.5\ k\Omega$

IF $\Delta V_{IN} = 250$ mV, $V_{SWITCH} = 13$ mV
THEN $R_S = 423\ \Omega$

Dwg. No. B-1524

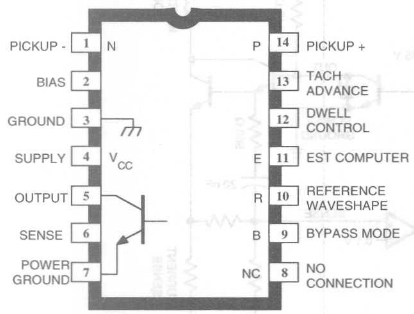
QUAD LAMP MONITOR



Dwg. No. A-12,035A

ELECTRONIC IGNITION TIMING

ULQ2460A



Dwg. No. PS-014

The ULQ2460A, ULQ2460C, and ULQ2460LW electronic ignition timing circuits are intended to interface between conventional electro-magnetic pick-ups, a computer-controlled electronic spark timing (EST) computer, and a high-efficiency ignition coil.

In application, the devices are designed to withstand various load dump and battery supply transients and to protect their output. They provide a positive shut down feature if battery supply voltages exceed 35 V. In the event of an open or shorted signal input, they provide a fail-safe mode that shuts off the output. If the EST computer fails or is disconnected, the ULQ2460A/C/LW will continue to process the pickup signal and thus allow the engine to continue to operate in a “limp” or soft-failure mode. For additional reliability improvement, a constant-current ignition coil drive eliminates the need for the usual ballast resistor.

The ULQ2460A is furnished in a 14-pin dual in-line plastic package. The ULQ2460LW is supplied in a surface-mountable 16-lead wide-body SOIC. The ULQ2460C is an unpackaged, passivated, chip for hybrid applications. All devices are rated for operation over the automotive/industrial temperature range of -40°C to +85°C.

FEATURES

- Improved System Reliability
- Internal Bypass Mode
- Constant-Current Drive to Ignition Coil
- 180 mJ Primary Coil Energy

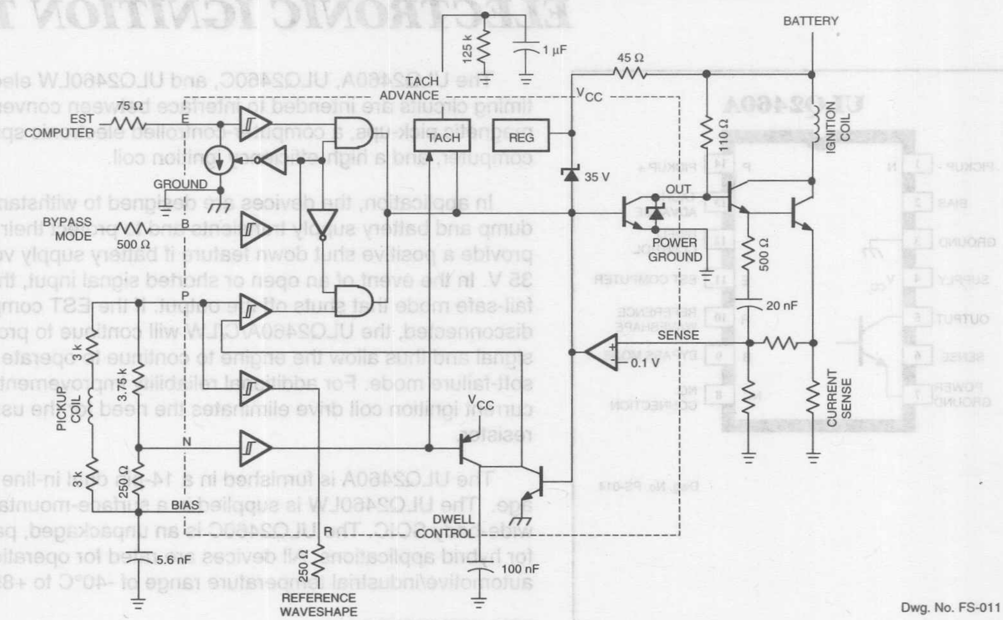
ABSOLUTE MAXIMUM RATINGS in Typical Application

Supply Voltage, V_{CC} (100 ms) . . . . **80 V**
(5 min.) . . . . **25 V**
(continuous) . . . . **16 V**
Peak Reverse Voltage, V_R . . . . **-5.0 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

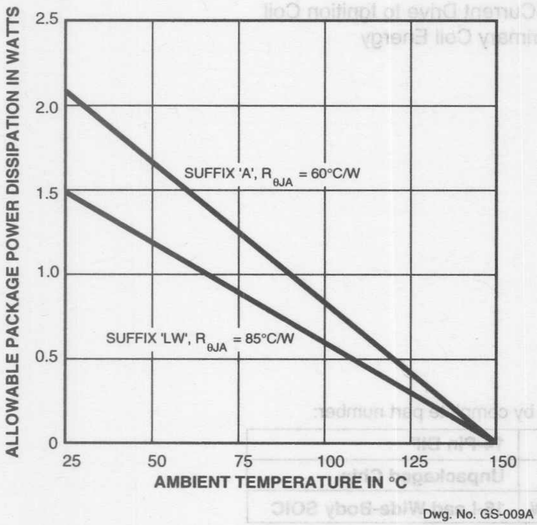
Always order by complete part number:

ULQ2460A	**14-Pin DIP**
ULQ2460C	**Unpackaged Chip**
ULQ2460LW	**16-Lead Wide-Body SOIC**

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATIONS

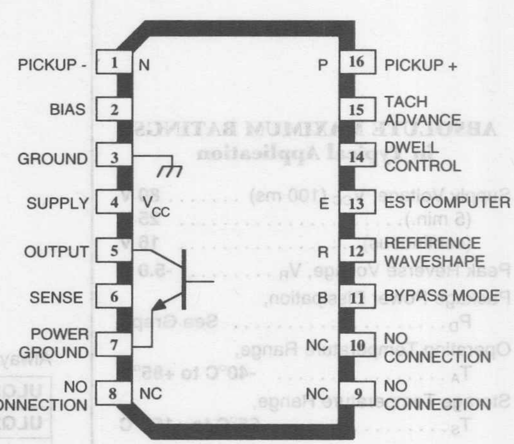


Dwg. No. FS-011



Dwg. No. GS-009A

ULQ2460LW



Dwg. No. PS-015

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 16 V, in typical application (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	4.0	—	16	V
Bypass Threshold	$V_{B(ON)}$	V_{11} = 2.3 V, 160 µA ≤ I_{11} ≤ 360 µA	1.4	1.8	2.3	V
	$V_{B(OFF)}$	V_{11} = 2.3 V, 3 mA ≤ I_{11} ≤ 15 mA	0.7	1.0	1.3	V
Bypass Hysteresis	ΔV_B		0.45	1.0	—	V
Bypass Input Current	I_B	V_9 = 2.3 V	160	—	360	µA
EST Threshold	$V_{E(ON)}$	V_9 = 2.3 V, Output HIGH	1.4	1.8	2.3	V
	$V_{E(OFF)}$	V_9 = 2.3 V, Output LOW	0.7	1.0	1.3	V
EST Hysteresis	ΔV_E		0.45	1.0	—	V
EST Input Current	I_E	V_{11} = 2.3 V, V_9 = 2.3 V	160	—	360	µA
		V_{11} = 2.3 V, V_9 = 0 V	3.0	—	15	mA
Reference Output	$V_{R(HI)}$	I_{10} = -10 µA, V_9 = 0 V, V_{PN} = 700 mV	—	—	6.0	V
		I_{10} = -1 mA, V_{PN} = 700 mV	2.4	—	—	V
	$V_{R(LO)}$	I_{10} = 1 mA, V_{PN} = 30 mV	—	—	0.75	V
Input Threshold	$V_{PN(ON)}$	V_{CC} = 4 V, V_6 = 0 V, Output HIGH	70	250	500	mV
		V_{10} ≥ 2.4 V, V_9 = 0 V	130	275	650	mV
		V_{10} ≥ 2.4 V, V_9 = 5 V	275	900	1500	mV
	$V_{PN(OFF)}$	V_{CC} = 4 V, V_6 = 0 V, Output LOW	5.0	100	—	mV
		V_{10} ≤ 0.75 V	40	100	—	mV
Input Hysteresis	ΔV_{PN}	V_6 = 0 V, V_{CC} = 4 V	30	150	—	mV
		V_9 = 0 V	75	150	—	mV
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 150 mA	—	200	500	mV
		Load Dump, I_{OUT} = 750 mA	—	—	1.0	V
Output Leakage Current	I_{OUT}	V_{OUT} = 3 V	—	—	2.0	µA
Output Current Limit Threshold Voltage	V_{SENSE}	4 V ≤ V_{CC} ≤ 26 V	65	100	135	mV
Output Current Temperature Coefficient	I_{OUT}	V_{CC} = 14.5 V, V_{PN} = 2 V	—	—	±2000	ppm/°C
Dwell Control Charge Current	I_{DWELL}	V_{PN} = 7 V, V_6 = 0 V, V_9 = 0 V, V_{12} = 4 V	15	—	70	µA
Dwell Control Discharge Current	I_{DWELL}	V_{PN} = 2.5 V, V_6 = 200 mV, V_B = 0 V, V_{12} = 4 V	30	—	80	µA

NOTE: Pin numbers apply to ULQ2460A.

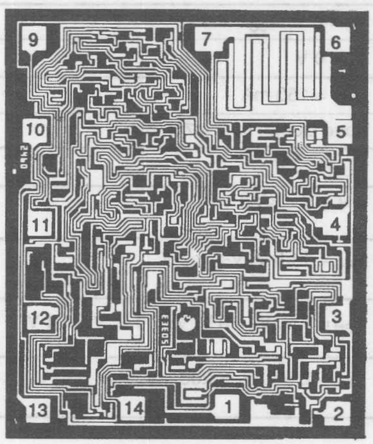
Continued next page...

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Dwell ON Threshold Control	V_{PN}	V_6 = 0 V, V_{12} = 4 V, Output HIGH	-0.8	—	-2.4	V
Dwell Threshold Control Clamp	V_{PN}	V_6 = 0 V, V_{12} = 7.5 V, Output HIGH	-3.5	—	-5.7	V
Advance Control Charge	V_P	V_{PN} = 7 V ⌊ 2.5 V, V_{12} = 0 V	1.7	—	3.0	V
Advance Control Discharge	V_P	V_{PN} = 2.5 V ⌊ 0 V, V_{12} = 0 V	—	—	900	mV
Advance Control Comparator Enabled	$V_{P(ON)}$	V_{PN} = 8 V, Output LOW	—	—	1.3	V
Advance Control Comparator Disabled	$V_{P(OFF)}$	V_{PN} = 8 V, Output HIGH	0.5	—	—	V
Advance Control Differential Voltage	ΔV_P		1.2	—	1.7	V
Input Signal Clamp	I_{13}	V_2 = -0.5 V	-0.5	—	-3.5	mA
Zener Clamp Current	I_{CC}	V_{CC} = 35 V, pulse test	29	—	77	mA

NOTE: Pin numbers apply to ULQ2460A.

ULQ2460C
(Pad numbers apply to ULQ2460A)



CIRCUIT DESCRIPTION & TYPICAL APPLICATION

The ULQ2460A, ULQ2460C, or ULQ2460LW electronic ignition timing circuit is connected to the electronic spark timing computer at three points:

REFERENCE WAVESHAPE (R). Sends engine crankshaft position and speed information to the electronic spark timing computer as determined by the state of the bypass control input.

ELECTRONIC SPARK TIMING (E). Receives dwell and timing information from the electronic spark timing computer for the initiation of primary coil current and spark timing. When the EST computer is in control (input B pulled high), a constant-current sink at this input turns ON as confirmation back to the computer.

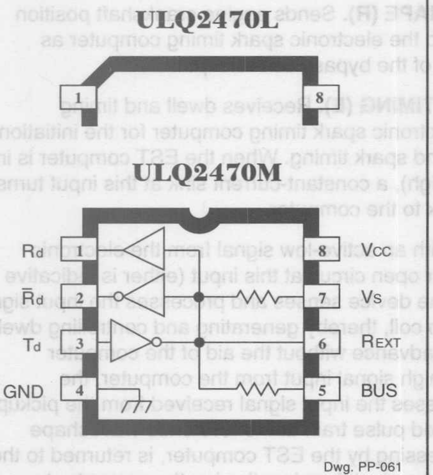
BYPASS MODE (B). With an active-low signal from the electronic spark timing computer or open circuit at this input (either is indicative of a computer failure), the device senses and processes the input signal received from the pickup coil, thereby generating and controlling dwell, spark timing, and spark advance without the aid of the computer (bypass mode). With a high signal input from the computer, the ULQ2460A/C/LW processes the input signal received from the pickup coil, generating a modified pulse train at the reference waveshape output which, after processing by the EST computer, is returned to the device through the EST terminal thereby allowing the computer to determine dwell, spark timing, and spark advance (EST mode).

The floating, ground-isolated signal generated by the electromagnetic pick-up is connected to the circuit through the P (positive) and N (negative) inputs.

The output of the circuit is connected through an external Darlington-connected power driver and the primary winding of a high-efficiency ignition coil to the battery without the need for ballast resistor protection and provides the following functions:

1. Stores energy in the magnetic field of the ignition coil based on the available dwell time.
2. Limits the maximum energy stored in the magnetic field of the ignition coil by limiting the maximum current that can be achieved (typically 5.5 A).
3. At the required time, it rapidly shuts off the coil current causing a collapse of the magnetic field and dumping the stored energy through the secondary winding at a very-high voltage into the spark plug.

In the EST mode of operation, the output is totally under the control of the computer.

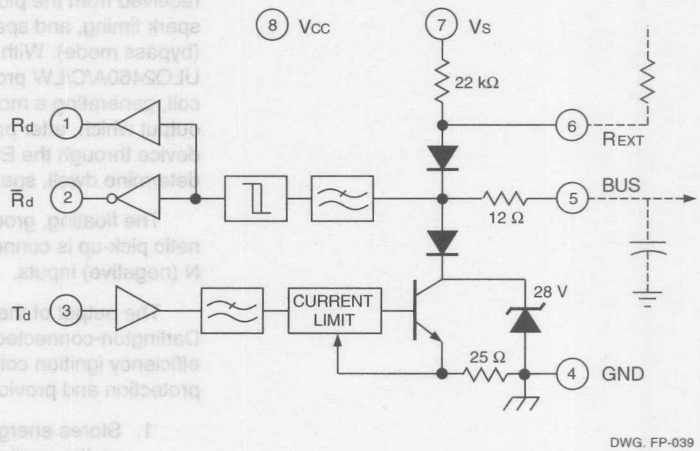


BUS DRIVER / RECEIVER

The ULQ2470L and ULQ2470M are bi-directional bus driver / receivers designed specifically for automotive applications. They are intended to be used as an interface between a microprocessor and a single-wire multiplex data bus operating from the A-line or battery. Each device consists of a wave-shaped open-collector driver, a pull-up resistor, and an input filter and buffer.

Output driver protection circuitry provides output shutdown if currents in excess of 25 to 30 mA occur. Additionally, over-voltage shutdown occurs when the bus voltage exceeds approximately 22 volts.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Bus Supply Voltage Range,
(V_{BAT}) .... **-13.5 V to 27 V**

Logic Supply Voltage Range,
(V_{CC}) .... **-0.3 V to 9.0 V**

Input Voltage Range,
(V_{BUS}) .... **-3.0 V to 24 V**

Operating Temperature Range,
T_A .... **-40°C to +85°C**

Junction Temperature Range,
T_J .... **-40°C to 150°C**

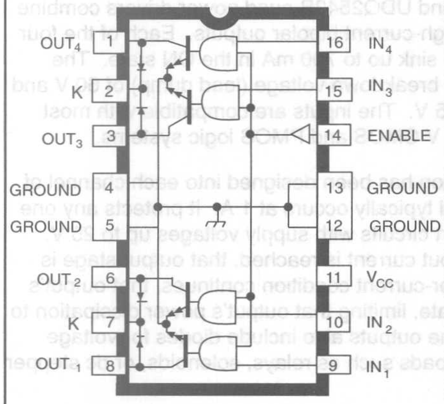
Storage Temperature Range,
T_S .... **-65°C to 150°C**

FEATURES AND BENEFITS

- Over-Voltage Protection
- Diode Isolation from both Ground and Supply
- Reverse-Battery Protection
- Low Supply Current
- High Noise Immunity
- Output Current Limiting
- Low Standby Current—24 µA Max.
- Open-Ground Protection
- Under-Voltage Lockout

2540

QUAD DARLINGTON POWER DRIVER



Dwg. No. A-11,561A

Combining AND logic gates and inverting high-current bipolar outputs, the UDQ2540B quad Darlington power driver provides interface between low-level signal-processing circuits and power loads totaling 360 W. Each of the four independent outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive leads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

Typical applications include print heads, relays, solenoids, and dc stepping motors. The UDQ2540B can also be used to drive high-current incandescent lamps, LEDS, and heaters. A similar device, specifically intended for driving a unipolar stepper motor in the two-phase drive format, is the UDQ2544B.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2540B are shown in Section 3. Complete, detailed technical information on the UDQ2540B is available on request.

The UDQ2540B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} .... **50 V**
Output Current, I_{OUT} (peak) .... **2.5 A**
(continuous) .... **1.8 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} .... **7.0 V**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

FEATURES

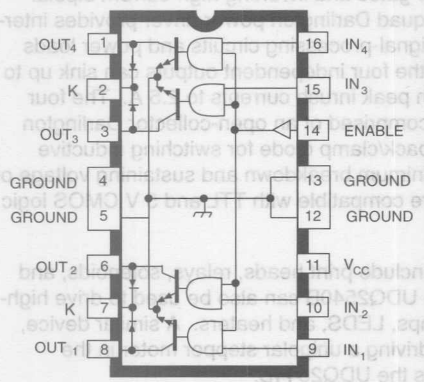
- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- TTL and 5 V CMOS Compatible Inputs
- Efficient Input/Output Pinning
- Integral Transient-Suppression Diodes
- Replaces L6221A

Always order by complete part number: **UDQ2540B**.

2543

29317.2A

PROTECTED QUAD POWER DRIVERS



Dwg. No. A-11,561A

Providing interface between low-level logic and power loads to 100 W, the UDN2543B and UDQ2543B quad power drivers combine NAND logic gates and high-current bipolar outputs. Each of the four independent outputs can sink up to 700 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 35 V. The inputs are compatible with most TTL, DTL, LSTTL, and 5 V CMOS and PMOS logic systems.

Over-current protection has been designed into each channel of the UDN/UDQ2543B and typically occurs at 1 A. It protects any one channel from output short circuits with supply voltages up to 25 V. When the maximum output current is reached, that output stage is driven linearly. If the over-current condition continues, that output's thermal limiting will operate, limiting that output's power dissipation to approximately 2.4 W. The outputs also include diodes for voltage clamping with inductive loads such as relays, solenoids, or dc stepper motors.

Both devices are supplied in a 16-pin power DIP of batwing construction to provide for maximum package power dissipation. They are rated for continuous operation over the temperature range of -20°C to +85°C (UDN2543B) or for use in automotive applications over an extended temperature range as the UDQ2543B. These devices are also available in a 28-lead PLCC. To order, change the suffix from 'B' to 'EB'.

FEATURES

- 700 mA Output Current per Channel
- Low Output-Saturation Voltage
- Integral Output Transient-Suppression Diodes
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Independent Over-Current Protection for Each Output

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

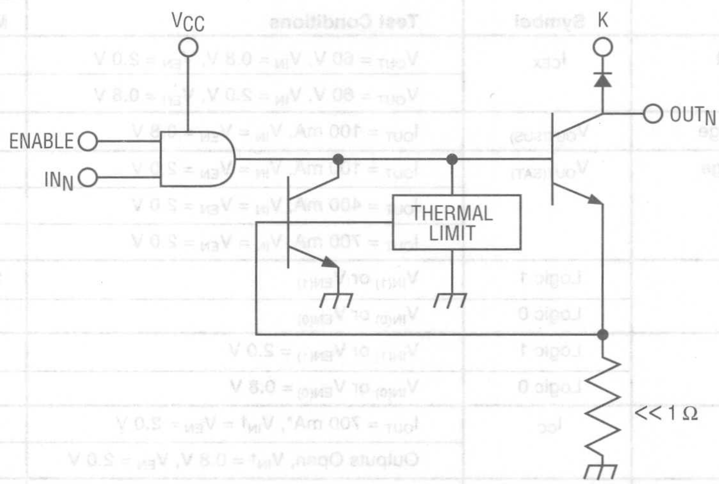
Output Voltage, V_{OUT} .... **60 V**
Over-Current Protected Output Voltage,
V_{OUT} .... **25 V**
Output Current, I_{OUT} .... **1.0 A***
Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} or V_{EN} .... **18 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range, T_A
(UDN2543B) .... **-20°C to +85°C**
(UDQ2543B) .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Applications for further information.

Always order by complete part number:

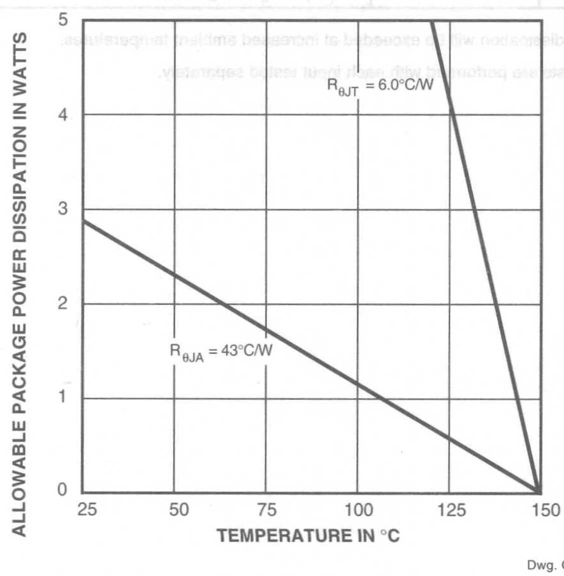
Part Number	Operating Temperature
UDN2543B	-20°C to +85°C
UDQ2543B	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM
(1 OF 4 CHANNELS)



Dwg. No. D-1005

NOTE: These devices do not include an absolute thermal shutdown. Package power dissipation under fault conditions (2.4 W in the faulted channel) must therefore be evaluated at maximum operating temperature.



Dwg. GP-010B

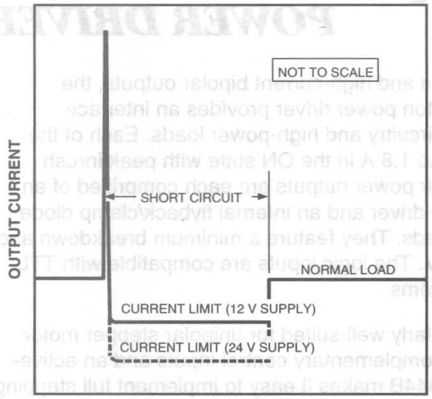
ELECTRICAL CHARACTERISTICS at T_A = +25°C (UDN2543B) or over operating temperature range (UDQ2543B only), V_{CC} = 4.75 V to 5.25 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	35	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 2.0 V	—	200	mV
		I_{OUT} = 400 mA, V_{IN} = V_{EN} = 2.0 V	—	400	mV
		I_{OUT} = 700 mA, V_{IN} = V_{EN} = 2.0 V	—	600	mV
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	20	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 700 mA*, V_{IN}† = V_{EN} = 2.0 V	—	65	mA
		Outputs Open, V_{IN}† = 0.8 V, V_{EN} = 2.0 V	—	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.6	V
		I_F = 1.5 A	—	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, V_{IN} = V_{EN} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$		50	µA

* Pulse test, allowable package power dissipation will be exceeded at increased ambient temperatures.

† All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT BEHAVIOR



Dwg. No. WP-013-1

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

For incandescent lamp applications, the UDN2549B/EB or UDN2559B/EB, with improved shortcircuit protection and thermal limiting, are recommended.

INDUCTIVE LOAD DRIVER

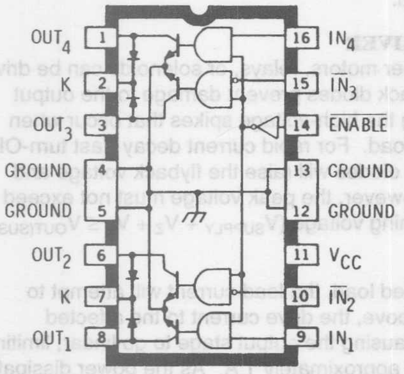
Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning OFF an inductive load. For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and improve performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F \leq V_{OUT(SUS)}$).

FAULT CONDITIONS

In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is diverted, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage ($I_{OUT} \approx 2.4/V_{SUPPLY}$). If the fault condition is corrected, the output stage will return to its normal saturated condition.

Due to the independent operation of the four channels, only a single channel should be shorted at a time. Multiple overload conditions may be tolerated provided rated package power dissipation is not exceeded.

QUAD DARLINGTON POWER DRIVER



Dwg. No. PP-017

Combining logic gates and high-current bipolar outputs, the UDQ2544B quad Darlington power driver provides an interface between low-level logic circuitry and high-power loads. Each of the four outputs can sink up to 1.8 A in the ON state with peak inrush currents to 2.5 A. The four power outputs are each comprised of an open-collector Darlington driver and an internal flyback/clamp diode for switching inductive loads. They feature a minimum breakdown and sustaining voltage of 50 V. The logic inputs are compatible with TTL and 5 V CMOS logic systems.

This device is particularly well-suited for unipolar stepper motor drive applications. With complementary control inputs and an active-low ENABLE, the UDQ2544B makes it easy to implement full stepping of a stepper motor with only two microcontroller/microprocessor control lines. Other typical applications include relay or solenoid driving and incandescent or LED lamp driving.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2544B are shown in Section 3. Complete, detailed technical information on the UDQ2544B is available on request.

The UDQ2544B is supplied in a 16-pin batwing power DIP. The batwing construction provides for maximum package power dissipation in a standard DIP construction. At 25°C, and with only 1 sq. in. of copper foil at the ground tabs, the package is capable of safely dissipating 3.8 W.

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT}	**50 V**
Output Current, I_{OUT}	
(Peak)	**2.5 A**
(Continuous)	**1.8 A**
Logic Supply Voltage, V_{CC}	**7.0 V**
Input Voltage, V_{IN}	**7.0 V**
Operating Temperature Range,	
T_A	**-40°C to +85°C**
Storage Temperature Range,	
T_S	**-55°C to +150°C**

FEATURES

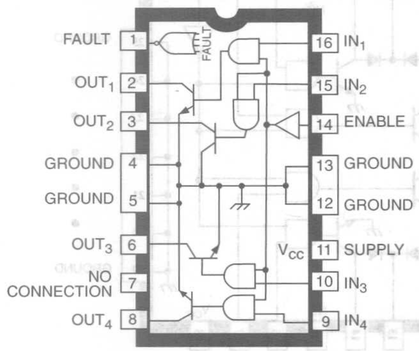
- 1.8 A Continuous Output Current
- Output Voltage to 50 V
- Inputs Configured for Unipolar Stepper Motors
- Active-Low Output Enable
- TTL and 5 V CMOS Compatible Inputs
- Integral Transient-Suppression Diodes

Always order by complete part number: **UDQ2544B** .

29317.4B

PROTECTED QUAD POWER DRIVERS

UDx2547B



Dwg. PP-018

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} .... **60 V**

Over-Current Protected Output Voltage, V_{OUT} .... **25 V**

Output Current, I_{OUT} .... **1.3 A***

FAULT Output Voltage, V_F .... **40 V**

Supply Voltage, V_{CC} .... **7.0 V**

Input Voltage, V_{IN} or V_{EN} .... **7.0 V**

Package Power Dissipation, P_D .... **See Graph**

Operating Temperature Range, T_A

Prefix 'UDK' .... **-40°C to +125°C**

Prefix 'UDN' .... **-20°C to +85°C**

Prefix 'UDQ' .... **-40°C to +85°C**

Storage Temperature Range, T_S .... **-55°C to +150°C**

*Outputs are current limited at approximately 1.3 A per driver and junction temperature limited if current in excess of 1.3 A is attempted. See Circuit Description and Application for further information.

Providing interface between low-level logic and power loads, the UDK/UDN/UDQ2547B and UDK/UDN/UDQ2547EB quad power drivers combine logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems and include internal pull-down resistors to ensure that the outputs remain OFF if the inputs are open-circuited.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1.3 A. It protects each output from short circuits with supply voltages up to 25 V. When a maximum driver output current is reached, that output drive is reduced linearly, maintaining a constant load current. If the over-current or short circuit condition continues, each channel has an independent thermal limit circuit which will sense the rise in junction temperature and turn OFF the individual channel that is at fault. Foldback circuitry decreases the output current if excessive voltage is present across the output and assists in keeping the device within its SOA (safe operating area).

Each output also includes diagnostics for increased device protection. If any output is shorted or opened, the diagnostics can signal the controlling circuitry through a common FAULT pin.

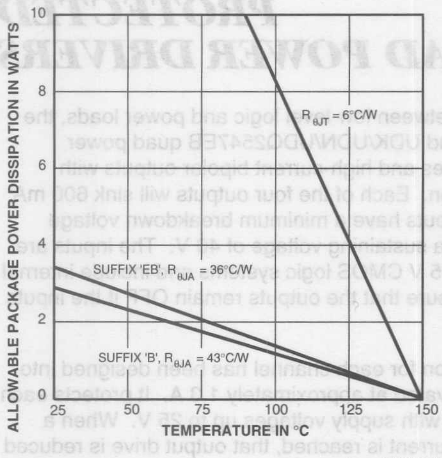
These devices can be used to drive various resistive loads including incandescent lamps (without warming or limiting resistors). With the addition of external output clamp diodes, they can be used to drive inductive loads such as relays, solenoids, or dc stepping motors.

The suffix 'B' devices are 16-pin power DIPs while the suffix 'EB' devices are 28-lead power PLCCs for surface-mount applications. Both packages are of batwing construction to provide for maximum package power dissipation.

FEATURES

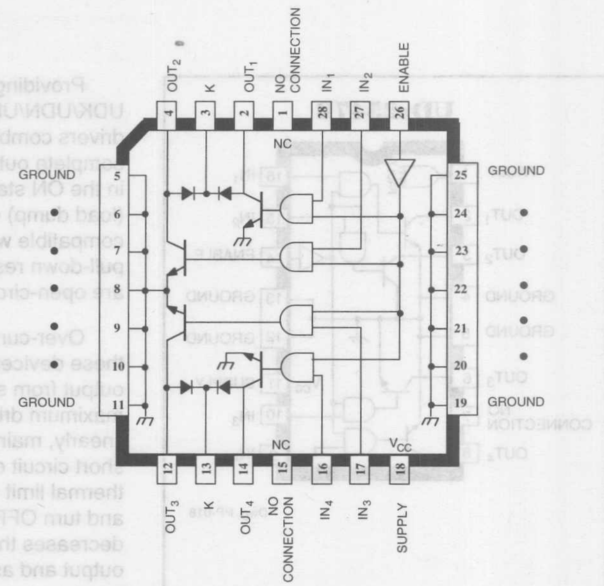
- Output SOA Protection
- Low Output-Saturation Voltage
- Diagnostic FAULT Output
- TTL and 5 V CMOS Compatible Inputs
- Independent Over-Current Protection for Each Driver
- Independent Thermal Protection for Each Driver
- 600 mA Output Current per Channel

Always order by complete part number: a prefix to indicate operating temperature range + the basic four-digit part number + a suffix to indicate package style, e.g.. $\boxed{\text{UDK2547EB}}$



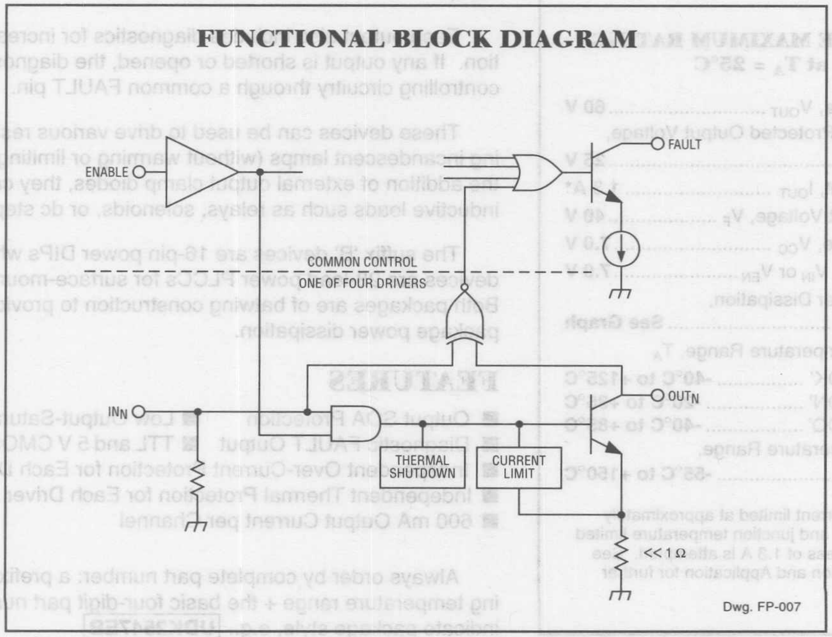
Dwg. GP-004-1A

UDx2547EB



Dwg. PP-019

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-007

ELECTRICAL CHARACTERISTICS at T_A = +25°C (prefix 'UDN') or over operating temperature range (prefix 'UDK' or 'UDQ'), V_{CC} = 4.75 V to 5.5 V

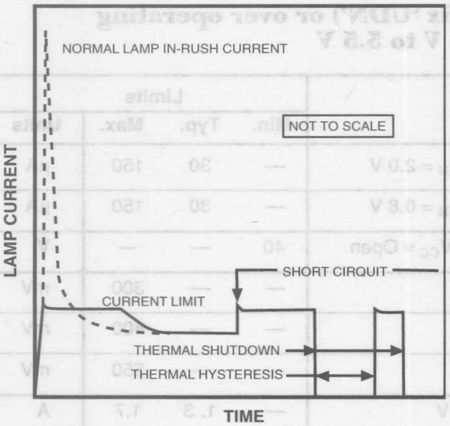
Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current*	I_{OUT}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	30	150	μA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	30	150	μA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = 0.8 V, V_{CC} = Open	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 400 mA	—	—	300	mV
		I_{OUT} = 500 mA	—	—	400	mV
		I_{OUT} = 600 mA	—	—	550	mV
Over-Current Limit	I_{OUT}	5 ms PulseTest, V_{OUT} = 5.0 V	—	1.3	1.7	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	60	μA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	10	—	—	μA
Fault Output Leakage Current	I_F	V_F = 40 V	—	<1.0	2.0	μA
Fault Output Current	I_F	V_F = 40 V, Driver Outputs Open, V_{IN} = 0.8 V, V_{EN} = 2.0 V	40	60	80	μA
Fault Output Saturation Voltage	$V_{F(SAT)}$	I_F = 30 μA	—	0.1	0.4	V
Total Supply Current	I_{CC}	All Outputs ON	—	45	50	mA
		All Outputs OFF	—	6.0	10	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	ΔT_J		—	15	—	°C

Typical Data is for design information only.
*Measurement includes XOR input current and other elements.

TRUTH TABLE

STATUS	IN_N	ENABLE	OUT_N	FAULT
Normal Load	H	H	L	H
	L	H	H	H
	X	L	H	H
Over-Current or Short to Supply	H	H	R	L
Thermal Fault	H	H	H	L
Open Load or Short to Ground	L	H	L	L

X = Don't care. R = Linear drive, current limited.



Dwg. WP-005A

CIRCUIT DESCRIPTION AND APPLICATION

These devices monitor their outputs for open or shorted conditions. Both conditions are sensed by comparing the input and output states. Note that the FAULT output is operational only if the ENABLE input is high. When a fault condition is sensed, the FAULT output will go to a low state. An external FAULT output filter capacitor (0.1µF) is recommended to eliminate erroneous switching.

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers.

Warming (parallel) or current-limiting (series) resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 600 mA can be driven without the need for warming or current-limiting resistors, if lamp turn-ON time is not a concern.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With these drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor, drive current to the output stage is diverted by the shunting transistor, the output stage operates in a linear mode, and the load current is limited to approximately 1.3 A. During lamp warmup, the filament resistance increases to its maximum value, the output driver goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

With the addition of external clamp diodes, bifilar (unipolar) stepper motors and other inductive loads can be driven directly. The external diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning OFF an inductive load. For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and improve performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F \leq V_{OUT(SUS)}$).

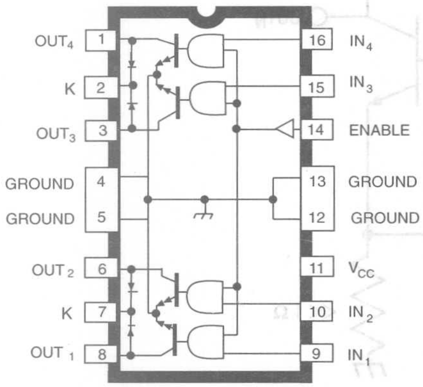
OVER-CURRENT CONDITIONS

In the event of a shorted load, or stalled motor, the load current will attempt to increase. As described above, the drive current to the affected output stage is linearly reduced (limiting the load current to about 1.3 A), causing the output stage to go linear. As the junction temperature of the output stage increases, the thermal shutdown circuit will shut OFF the affected output. If the fault condition is corrected, the output driver will return to its normal saturated condition.

2549

PROTECTED QUAD POWER DRIVERS

UDx2549B



Dwg. No. A-11,561A

Providing improved output current limiting, the UDK/UDN/UDQ2549B and UDK/UDN/UDQ2549EB quad power drivers combine NAND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 600 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short circuit condition continues, the thermal limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, the six devices in this family will tolerate short-circuits on all outputs, simultaneously.

These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

The suffix ‘B’ devices are 16-pin power DIPs while the suffix ‘EB’ devices are 28-lead power PLCCs for surface-mount applications. Both packages are of batwing construction to provide for maximum package power dissipation.

ABSOLUTE MAXIMUM RATINGS at $T_A = 25°C$

Output Voltage, V_{OUT} . . . . 60 V
Over-Current Protected Output Voltage,
V_{OUT} . . . . 25 V
Output Current, I_{OUT} . . . . 1.0 A*
Supply Voltage, V_{CC} . . . . 7.0 V
Input Voltage, V_{IN} or V_{EN} . . . . 7.0 V
Package Power Dissipation,
P_D . . . . See Graph
Operating Temperature Range, T_A
Prefix ‘UDK’ . . . . -40°C to +125°C
Prefix ‘UDN’ . . . . -20°C to +85°C
Prefix ‘UDQ’ . . . . -40°C to +85°C
Storage Temperature Range,
T_S . . . . -55°C to +150°C

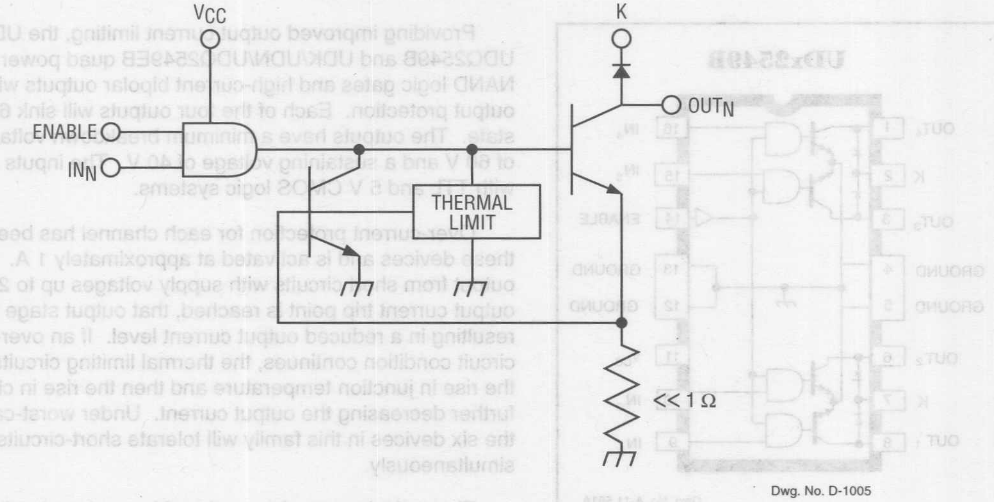
*Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Applications for further information.

FEATURES

- 600 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDN2543B/EB

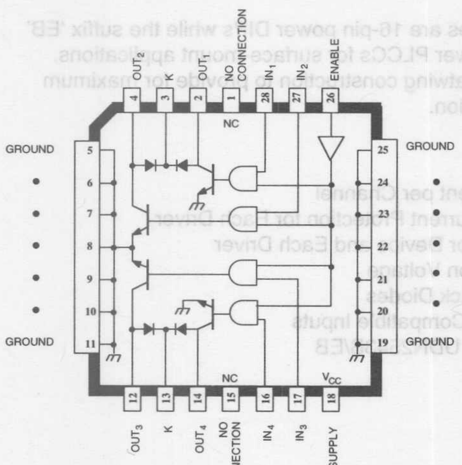
Always order by complete part number: a prefix to indicate operating temperature range + the basic four-digit part number + a suffix to indicate package style, e.g., UDK2549EB.

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)

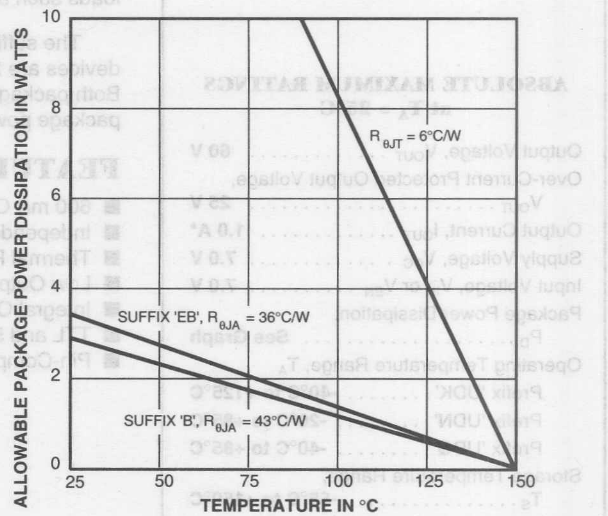


Dwg. No. D-1005

UDx2549EB



Dwg. No. PP-019-1



Dwg. No. GP-004-1A

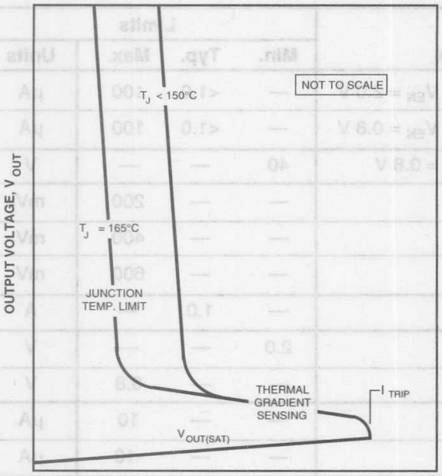
ELECTRICAL CHARACTERISTICS at T_A = +25°C (prefix 'UDN') or over operating temperature range (prefix 'UDK' or 'UDQ'), V_{CC} = 4.75 V to 5.25 V

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	<1.0	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 100 mA	—	—	200	mV
		I_{OUT} = 400 mA	—	—	400	mV
		I_{OUT} = 600 mA	—	—	600	mV
Over-Current Trip	I_{TRIP}		—	1.0	—	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 600 mA, V_{IN}* = V_{EN} = 2.0 V	—	—	65	mA
		All Outputs OFF	—	—	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	—	1.7	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, D_1 + D_2 or D_3 + D_4	—	—	50	µA
Thermal Limit	T_J		—	165	—	°C

Typical Data is for design information only.

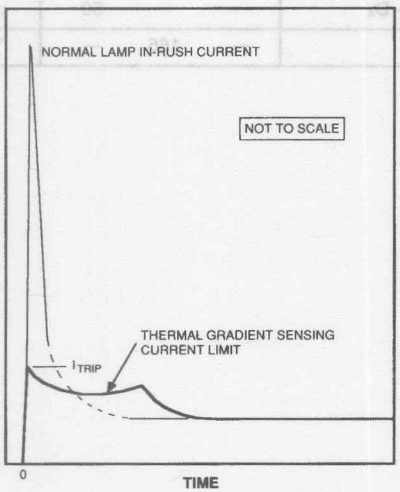
* All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT CHARACTERISTIC



Dwg. No. GP-013

TYPICAL OUTPUT BEHAVIOR



Dwg. No. WP-008

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 600 mA can be driven by these devices without the need for warming (parallel) or current-limiting (series) resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With the these drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor, and the load current is momentarily limited to approximately 1.0 A. During this short transition period, the output current is reduced to a value dependent on supply voltage and filament resistance. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load. For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and improve performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F \le V_{OUT(SUS)}$).

FAULT CONDITIONS

In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is reduced, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance.

Continuous or multiple overload conditions causing the chip temperature to reach approximately 165°C will result in an additional reduction in output current to maintain a safe level.

If the fault condition is corrected, the output stage will return to its normal saturated condition.

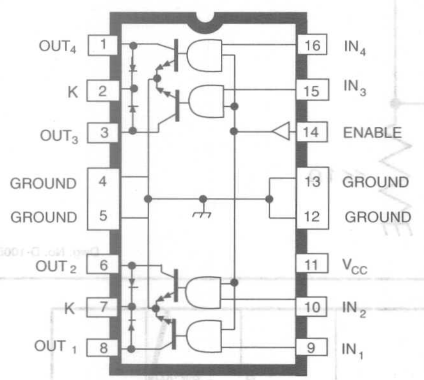
2559

29317.14

PROTECTED QUAD POWER DRIVERS

UDx2559LB

UDx2559B



Dwg. No. A-11,561A

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{OUT} . . . . **60 V**
Over-Current Protected Output Voltage,
V_{OUT} . . . . **25 V**
Output Current, I_{OUT} . . . . **1.0 A***
Supply Voltage, V_{CC} . . . . **7.0 V**
Input Voltage, V_{IN} or V_{EN} . . . . **7.0 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range, T_A
Prefix 'UDK' . . . . **-40°C to +125°C**
Prefix 'UDN' . . . . **-20°C to +85°C**
Prefix 'UDQ' . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

*Outputs are peak current limited at approximately 1.0 A per driver. See Circuit Description and Application for further information.

Providing improved output current limiting, the UDK, UDN, and UDQ2559B, EB, and LB quad power drivers combine NAND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 700 mA in the ON state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short-circuit condition continues, the thermal-limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, these devices will tolerate short circuits on all outputs, simultaneously.

These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

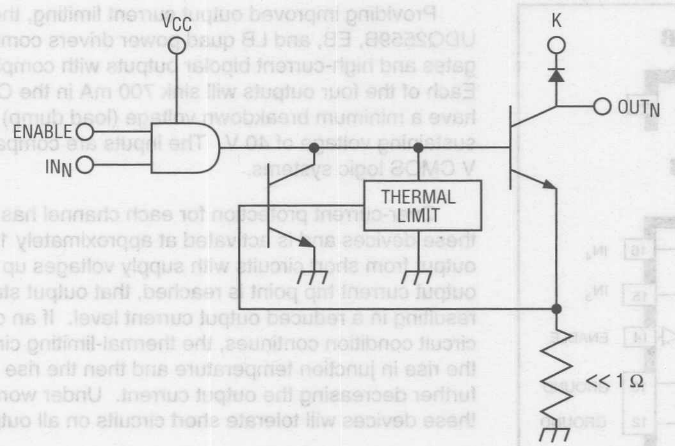
The suffix 'B' devices are 16-pin power DIPs, the suffix 'EB' devices are 28-lead power PLCCs and suffix 'LB' devices are 16-lead power SOICs for surface-mount applications. All three packages are of batwing construction to provide for maximum package power dissipation.

FEATURES

- 700 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDQ2543B/EB and UDK2549B/EB

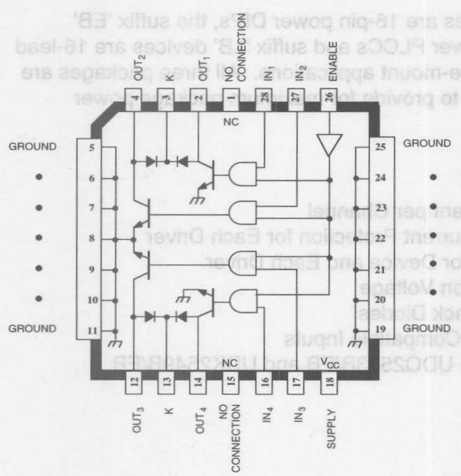
Always order by complete part number: a prefix to indicate operating temperature range + the basic four-digit part number + a suffix to indicate package style, e.g., UDK2559LB

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)

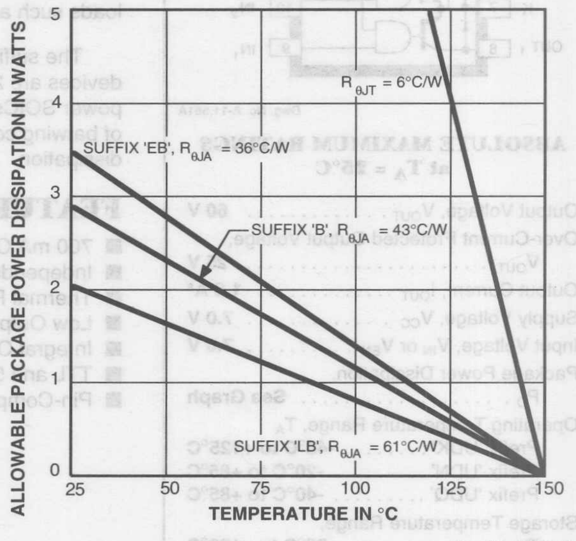


Dwg. No. D-1005

UDx2559EB



Dwg. No. PP-019-1



Dwg. No. GP-004-2

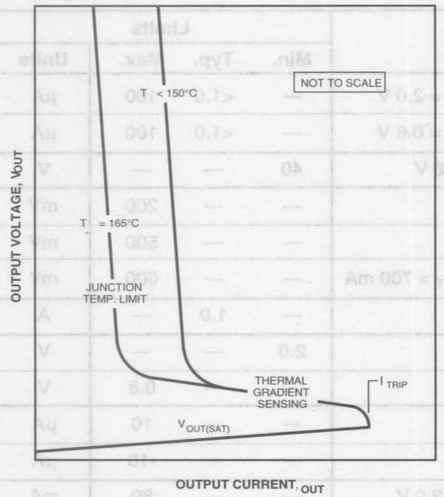
$$P_D = (V_{OUT1} \times I_{OUT1} \times dc) + \ldots + (V_{OUTn} \times I_{OUTn} \times dc) + (V_{CC} \times I_{CC})$$
$$= (T_J - T_A)/R_{\theta JA}$$

ELECTRICAL CHARACTERISTICS at T_A = +25°C (prefix 'UDN') or over operating temperature range (prefix 'UDK' or 'UDQ'), V_{CC} = 4.75 V to 5.25 V

			Limits			
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{EN} = 2.0 V	—	<1.0	100	μA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{EN} = 0.8 V	—	<1.0	100	μA
Output Sustaining Voltage	$V_{OUT(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 0.8 V	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	All Devices, I_{OUT} = 100 mA	—	—	200	mV
		All Devices, I_{OUT} = 500 mA	—	—	500	mV
		'B' & 'EB' Packages Only, I_{OUT} = 700 mA	—	—	600	mV
Over-Current Trip	I_{TRIP}		—	1.0	—	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$ = 2.0 V	—	—	10	μA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$ = 0.8 V	—	—	-10	μA
Total Supply Current	I_{CC}	I_{OUT} = 500 mA*, V_{IN}† = V_{EN} = 2.0 V	—	—	80	mA
		All Outputs OFF	—	—	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	—	1.7	V
		I_F = 1.5 A	—	—	2.1	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, D_1 + D_2 or D_3 + D_4	—	—	50	μA
Turn-On Delay	t_{PHL}	I_C = 500 mA	—	—	20	μs
	t_{PLH}	I_C = 500 mA	—	—	20	μs
Thermal Limit	T_J		—	165	—	°C

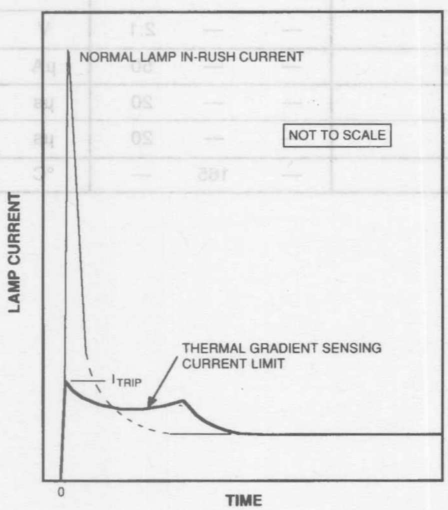
Typical Data is for design information only.
* Pulse test, four outputs simultaneously.
† All inputs simultaneously, all other tests are performed with each input tested separately.

TYPICAL OUTPUT CHARACTERISTIC



Dwg. No. GP-013

TYPICAL OUTPUT BEHAVIOR



Dwg. No. WP-008

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 700 mA can be driven by these devices without the need for warming (parallel) or current-limiting (series) resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With these drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor, and the load current is momentarily limited to approximately 1.0 A. During this short transition period, the output current is reduced to a value dependent on supply voltage and filament resistance. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning OFF an inductive load.

For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and inprove performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F \leq V_{OUT(SUS)}$).

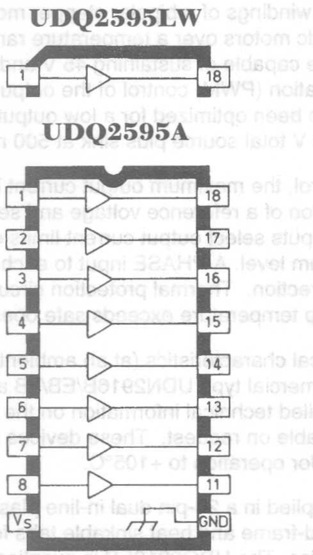
FAULT CONDITIONS

In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is reduced, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance.

Continuous or multiple overload conditions causing the chip temperature to reach approximately 165°C will result in an additional reduction in output current to maintain a safe level.

If the fault condition is corrected, the output stage will return to its normal saturated condition.

8-CHANNEL SATURATED SINK DRIVERS



Dwg. No. A-11,407

Developed for use with low-voltage LED and incandescent displays requiring low output saturation voltage, the UDQ2595A and UDQ2595LW meet many interface needs, including those exceeding the capabilities of standard logic buffers. The eight non-Darlington outputs of each driver can continuously and simultaneously sink load currents of 100 mA at ambient temperatures of up to +75°C.

The eight-channel driver's active-low inputs can be driven directly from TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified printed wiring board layouts.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2595A/LW are shown in Section 3. Complete, detailed technical information on the UDQ2595A/LW is available on request.

These drivers are packaged in plastic DIPs (suffix A) or surface-mountable wide-body SOICs (suffix LW), and are rated for operation over the temperature range of -40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one driver (unless otherwise noted)

Output Voltage, V_{CE} .... **20 V**
Supply Voltage, V_S .... **20 V**
Input Voltage, V_{IN} .... **20 V**
Output Current, I_C .... **200 mA**
Ground Terminal Current, I_{GND} **1.6A**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Note that the UDQ2595A (dual in-line package) and UDQ2595LW (small-outline IC package) are electrically identical and share a common pin number assignment.

FEATURES

- Non-Inverting Function (Input Low = Output ON)
- 200 mA Current Rating
- 100 mA Continuous and Simultaneous (All outputs) to +85°C
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- DIP or SOIC Packaging

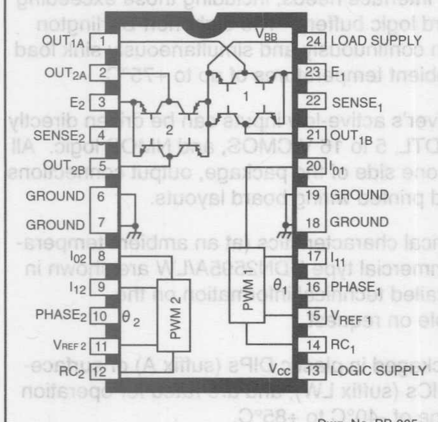
Always order by complete part number:

Part Number	Package
UDQ2595A	18-Pin DIP
UDQ2595LW	18-Lead Wide-Body SOIC

2916

DUAL FULL-BRIDGE PWM MOTOR DRIVER

UDQ2916B



Dwg. No. PP-005

The UDQ2916B, UDQ2916EB, and UDQ2916LB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors over a temperature range of -40°C to +85°C. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33, 67, or 100% of the maximum level. A PHASE input to each bridge determines load current direction. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2916B/EB/LB are shown in Section 3. Complete, detailed technical information on the UDQ2916B/EB/LB is available on request. These devices are also available on special order for operation to +105°C.

The UDQ2916B is supplied in a 24-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. The UDQ2916EB is supplied in a 44-lead power PLCC for surface mount applications. The UDQ2916LB is supplied in a 24-lead surface-mountable SOIC. Their batwing construction provides for maximum package power dissipation in the smallest possible construction.

ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Motor Supply Voltage, V_{BB} .... **45 V**
Output Current, I_{OUT}
(Peak) .... **+1.0 A**
(Continuous) .... **+750 mA**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E .... **1.5 V**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

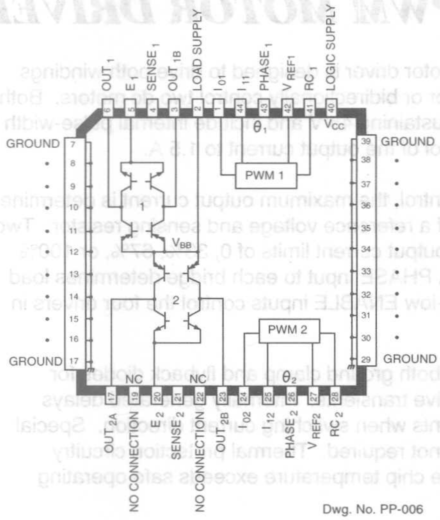
FEATURES

- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3717, UC3770

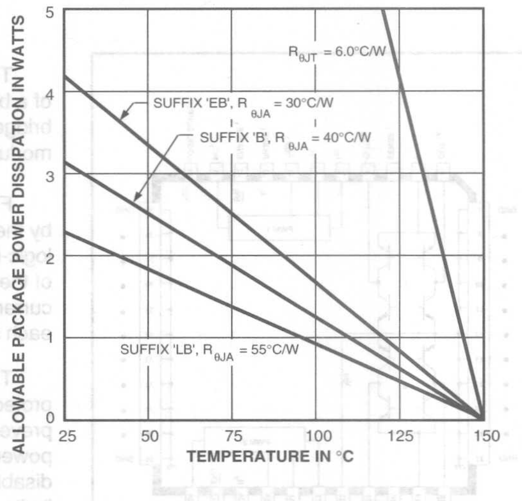
Always order by complete part number:

Part Number	Package
UDQ2916B	24-Pin DIP
UDQ2916EB	44-Lead PLCC
UDQ2916LB	24-Lead SOIC

UDQ2916EB

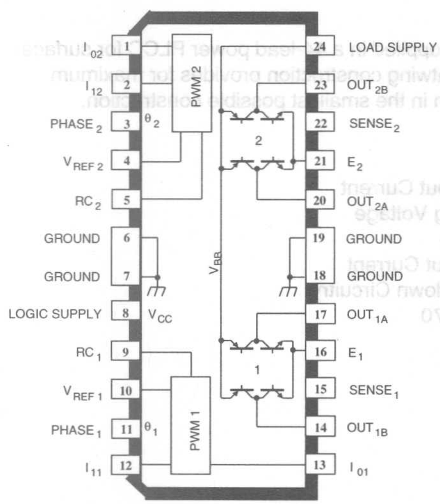


Dwg. No. PP-006



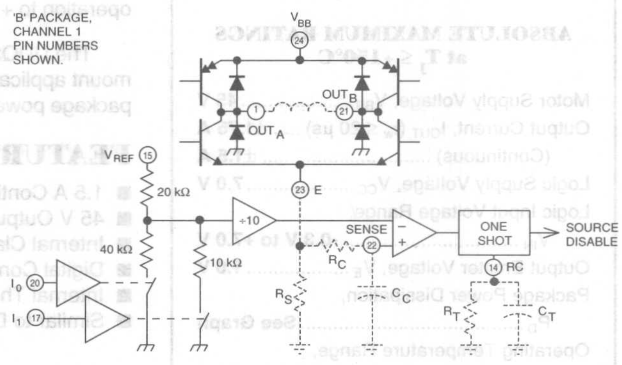
Dwg. GP-035A

UDQ2916LB



Dwg. PP-047

PWM CURRENT-CONTROL CIRCUITRY

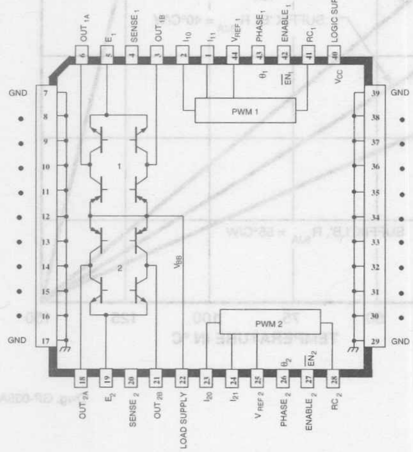


Dwg. No. EP-007B

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

DUAL FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PP-021

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} .... **45 V**
Output Current, I_{OUT} ($t_w \leq 20$ µs) ..... **±1.75 A**
(Continuous) .... **±1.5 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E .... **1.0 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The UDQ2917EB motor driver is designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 1.5 A.

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction. Active-low ENABLE inputs control the four drivers in each bridge.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2917EB are shown in Section 3. Complete, detailed technical information on the UDQ2917EB is available on request. These devices are also available on special order for operation to +125°C.

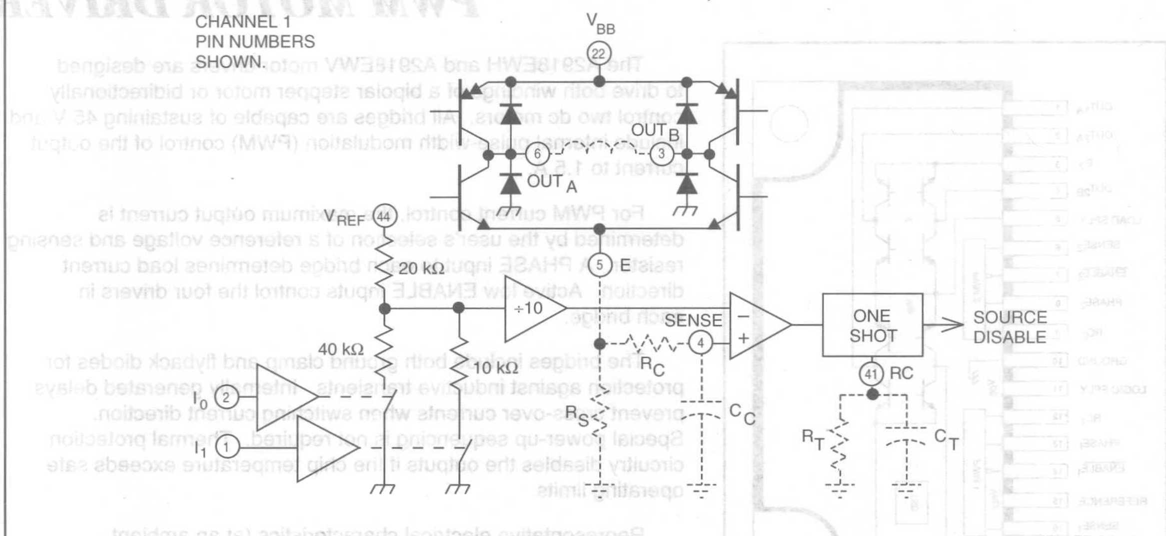
The UDQ2917EB is supplied in a 44-lead power PLCC for surface-mount applications. Its batwing construction provides for maximum package power dissipation in the smallest possible construction.

FEATURES

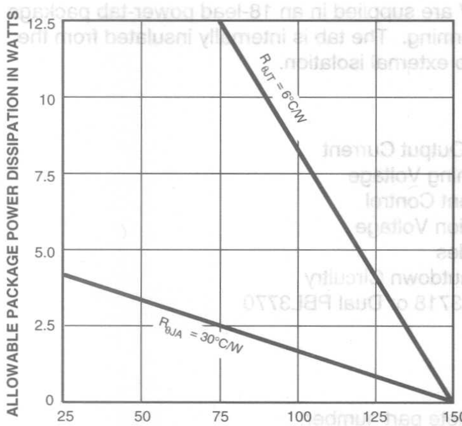
- 1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Digital Control of Output Current
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3770

Always order by complete part number: UDQ2917EB .

PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007-2A



Dwg. GP-020B

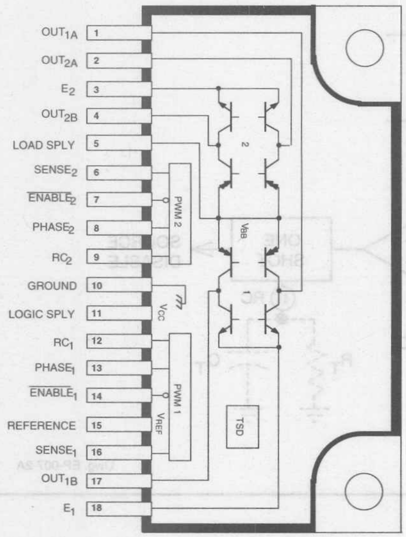
TRUTH TABLE

Enable	Phase	Out_A	Out_B
L	H	H	L
L	L	L	H
H	X	Z	Z

X = Don't care
Z = High impedance

2918

DUAL FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PP-051

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Motor Supply Voltage, V_{BB} . . . . **45 V**

Output Current, I_{OUT} ($t_w \leq 20$ µs) . . **±1.75 A**

(Continuous) . . . . **±1.5 A**

Logic Supply Voltage, V_{CC} . . . . **7.0 V**

Logic Input Voltage Range,

V_{IN} . . . . **-0.3 V to +7.0 V**

Output Emitter Voltage, V_E . . . . **1.5 V**

Package Power Dissipation,

P_D . . . . **See Graph**

Operating Temperature Range,

T_A . . . . **-40°C to +85°C**

Storage Temperature Range,

T_S . . . . **-40°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The A2918EWH and A2918EWV motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. All bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 1.5 A.

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. A PHASE input to each bridge determines load current direction. Active low ENABLE inputs control the four drivers in each bridge.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type A2918SWH/SWV are shown in Section 3. Complete, detailed technical information on the A2918EWH/EWV is available on request. These devices are also available on special order for operation to +125°C.

The A2918EWH/V are supplied in an 18-lead power-tab package with staggered lead forming. The tab is internally insulated from the device and requires no external isolation.

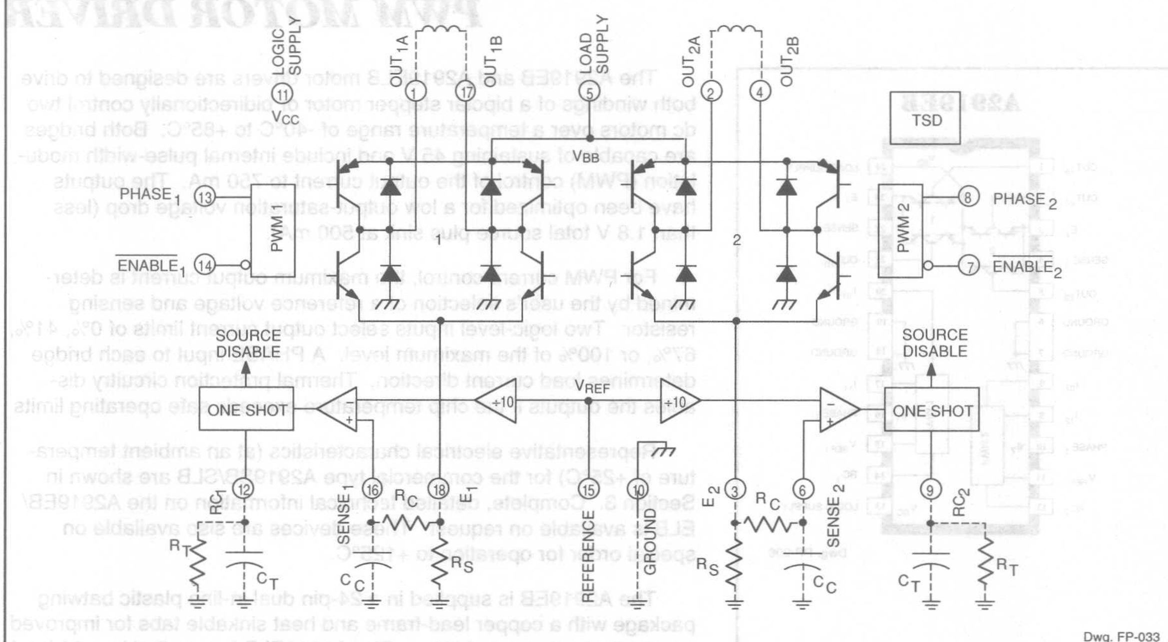
FEATURES

- ±1.5 A Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Clamp Diodes
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3718 or Dual PBL3770

Always order by complete part number:

Part Number	Application
A2918EWH	**For Horizontal Mount**
A2918EWV	**For Vertical Mount**

FUNCTIONAL BLOCK DIAGRAM

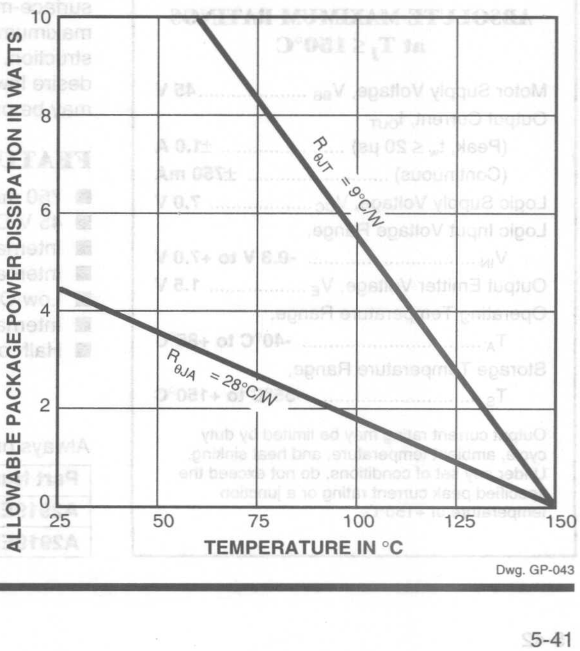


Dwg. FP-033

TRUTH TABLE

Enable	Phase	Out$_A$	Out$_B$
L	H	H	L
L	L	L	H
H	X	Z	Z

X = Don't care
Z = High impedance

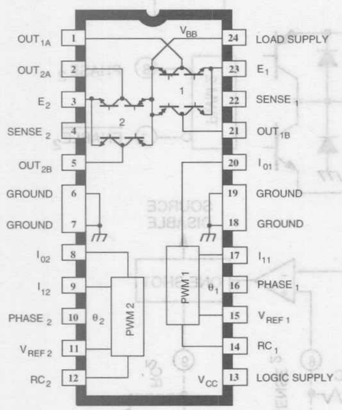


Dwg. GP-043

2919

DUAL FULL-BRIDGE PWM MOTOR DRIVER

A2919EB



Dwg. PP-006

ABSOLUTE MAXIMUM RATINGS at $T_J \le 150°C$

Motor Supply Voltage, V_{BB} .... **45 V**
Output Current, I_{OUT}
(Peak, $t_w \le 20\ \mu s$) .... **±1.0 A**
(Continuous) .... **±750 mA**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to +7.0 V**
Output Emitter Voltage, V_E .... **1.5 V**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The A2919EB and A2919ELB motor drivers are designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors over a temperature range of -40°C to +85°C. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output-saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0%, 41%, 67%, or 100% of the maximum level. A PHASE input to each bridge determines load current direction. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type A2919SB/SLB are shown in Section 3. Complete, detailed technical information on the A2919EB/ELB is available on request. These devices are slso available on special order for operation to +125°C.

The A2919EB is supplied in a 24-pin dual in-line plastic batwing package with a copper lead-frame and heat sinkable tabs for improved power dissipation capabilities. The A2919ELB is supplied in a 24-lead surface-mountable SOIC. Their batwing construction provides for maximum package power dissipation in the smallest possible construction. For applications not requiring quarter-step operation, but desire lower detent or running current, the similar UDQ2916B/EB/LB may be preferred.

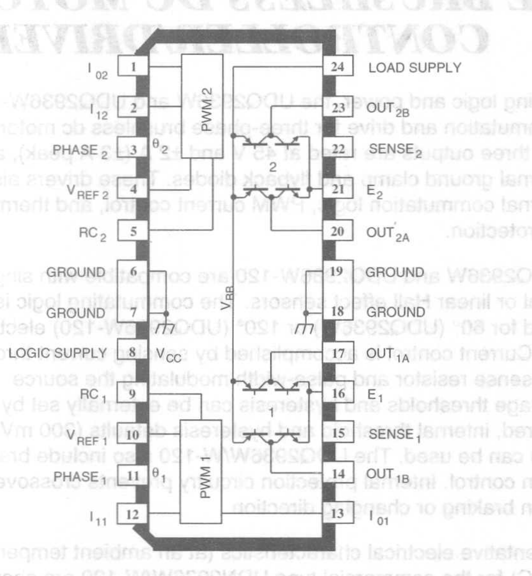
FEATURES

- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Half- or Quarter-Step Operation of Bipolar Stepper Motors

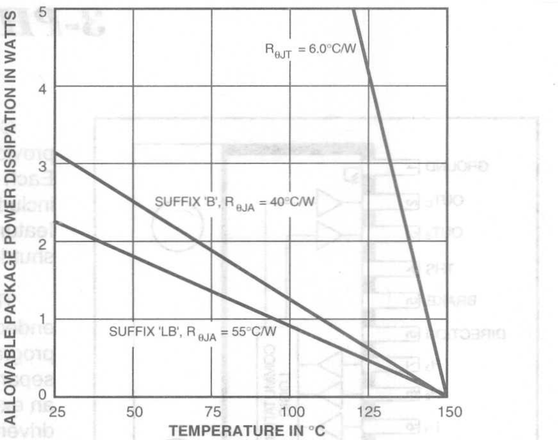
Always order by complete part number:

Part Number	Package	$R_{\theta JA}$	$R_{\theta JT}$
A2919EB	24-Pin DIP	40°C/W	6.0°C/W
A2919ELB	24-Lead SOIC	50°C/W	6.0°C/W

A2919ELB



Dwg. PP-047

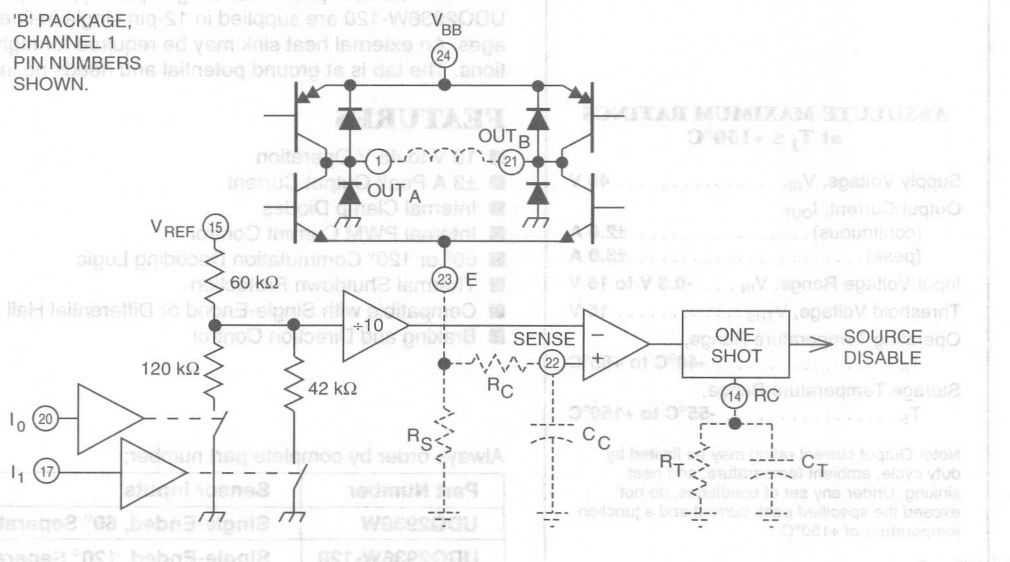


Dwg. GP-049A

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

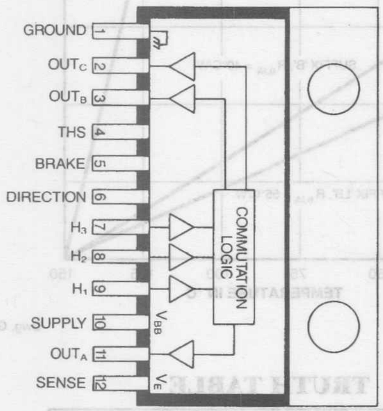
PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007-3

2936

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS



Dwg. No W-188

Combining logic and power, the UDQ2936W and UDQ2936W-120 provide commutation and drive for three-phase brushless dc motors. Each of the three outputs are rated at 45 V and ±2 A (±3 A peak), and include internal ground clamp and flyback diodes. These drivers also feature internal commutation logic, PWM current control, and thermal shutdown protection.

The UDQ2936W and UDQ2936W-120 are compatible with single-ended digital or linear Hall effect sensors. The commutating logic is programmed for 60° (UDQ2936W) or 120° (UDQ2936W-120) electrical separation. Current control is accomplished by sensing current through an external sense resistor and pulse-width modulating the source drivers. Voltage thresholds and hysteresis can be externally set by the user. If desired, internal threshold and hysteresis defaults (300 mV, 7.5 percent) can be used. The UDQ2936W/W-120 also include braking and direction control. Internal protection circuitry prevents crossover current when braking or changing direction.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2936W/W-120 are shown in Section 3. Complete, detailed technical information on the UDQ2936W/W-120 is available on request.

For maximum power-handling capability, the UDQ2936W and UDQ2936W-120 are supplied in 12-pin single in-line power tab packages. An external heat sink may be required for high-current applications. The tab is at ground potential and needs no insulation.

ABSOLUTE MAXIMUM RATINGS at $T_J \leq +150°C$

Supply Voltage, V_{BB} . . . . **45 V**

Output Current, I_{OUT}

(continuous) . . . . **±2.0 A**

(peak) . . . . **±3.0 A**

Input Voltage Range, V_{IN} . . . **-0.3 V to 15 V**

Threshold Voltage, V_{THS} . . . . **15 V**

Operating Temperature Range,

T_A . . . . **-40°C to +85°C**

Storage Temperature Range,

T_S . . . . **-55°C to +150°C**

Note: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

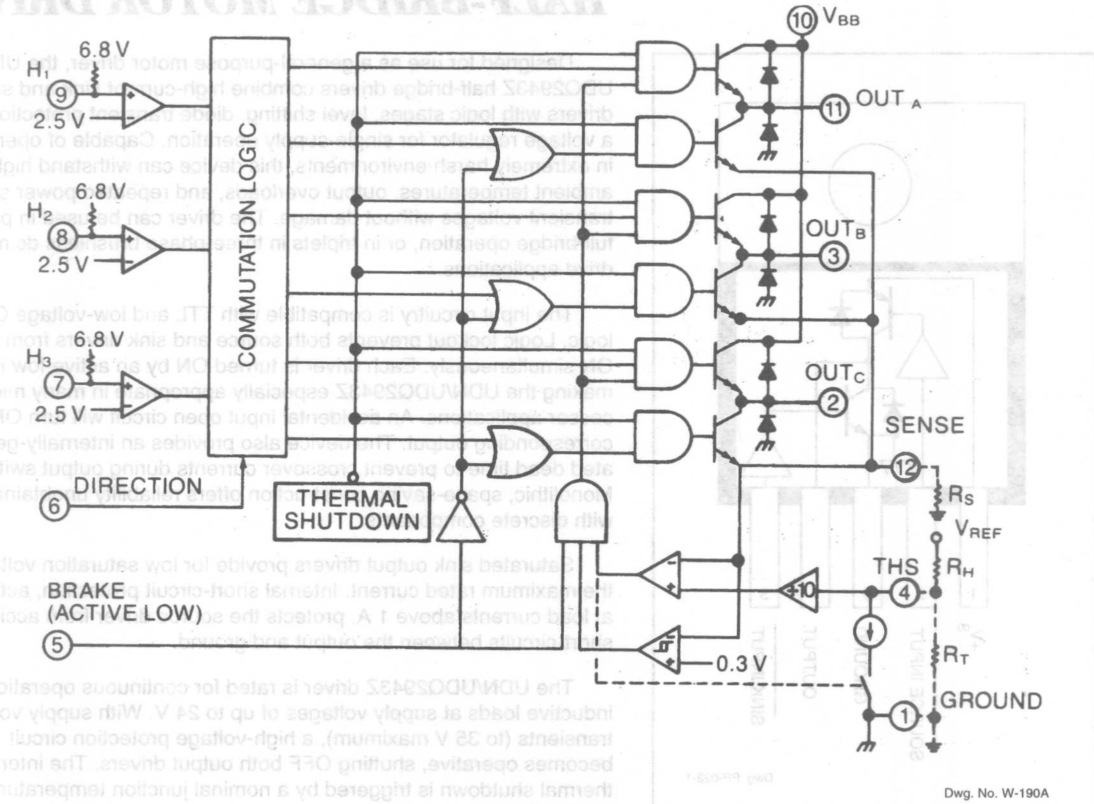
FEATURES

- 10 V to 45 V Operation
- ±3 A Peak Output Current
- Internal Clamp Diodes
- Internal PWM Current Control
- 60° or 120° Commutation Decoding Logic
- Thermal Shutdown Protection
- Compatible with Single-Ended or Differential Hall Effect Sensors
- Braking and Direction Control

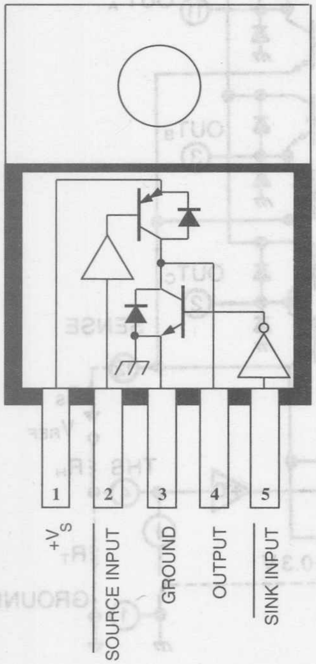
Always order by complete part number:

Part Number	Sensor Inputs
UDQ2936W	Single-Ended, 60° Separation
UDQ2936W-120	Single-Ended, 120° Separation

FUNCTIONAL BLOCK DIAGRAM



HIGH-CURRENT HALF-BRIDGE MOTOR DRIVER



Dwg. PP-022-1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Range V_S .... **8.5 V to 35 V***
Output Voltage, $V_{CE(sus)}$ .... **18 V**
Input Voltage Range, V_{IN} .... **-0.3 V to +18 V**
Continuous Output Current, I_{OUT} ...... **±1.0 A**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range, T_A
Prefix 'UDN' .... **-20°C to +85°C**
Prefix 'UDQ' .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Internal high-voltage shutdown above 24 V.

Designed for use as a general-purpose motor driver, the UDN and UDQ2943Z half-bridge drivers combine high-current sink and source drivers with logic stages, level shifting, diode transient protection, and a voltage regulator for single-supply operation. Capable of operating in extremely harsh environments, this device can withstand high ambient temperatures, output overloads, and repeated power supply transient voltages without damage. The driver can be used in pairs for full-bridge operation, or in triplets in three-phase brushless dc motor-drive applications.

The input circuitry is compatible with TTL and low-voltage CMOS logic. Logic lockout prevents both source and sink drivers from turning ON simultaneously. Each driver is turned ON by an active-low input, making the UDN/UDQ2943Z especially appropriate in many microprocessor applications. An accidental input open circuit will turn OFF the corresponding output. The device also provides an internally-generated dead time to prevent crossover currents during output switching. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Saturated sink output drivers provide for low saturation voltage at the maximum rated current. Internal short-circuit protection, activated at load currents above 1 A, protects the source driver from accidental short-circuits between the output and ground.

The UDN/UDQ2943Z driver is rated for continuous operation with inductive loads at supply voltages of up to 24 V. With supply voltage transients (to 35 V maximum), a high-voltage protection circuit becomes operative, shutting OFF both output drivers. The internal thermal shutdown is triggered by a nominal junction temperature of 160°C.

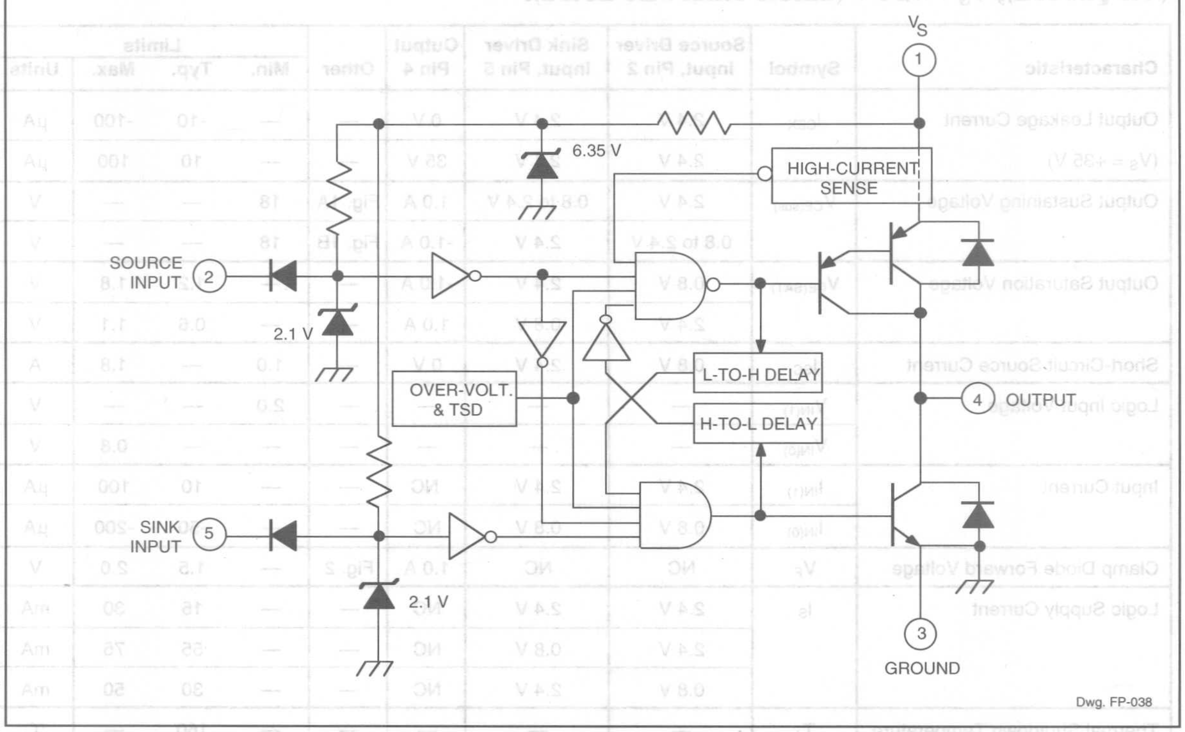
Single-chip construction and a 5-lead power-tab TS-001 plastic package provide cost-effective and reliable systems designs.
It also features excellent power dissipation ratings, minimum size, and ease of installation. The heat-sink tab is at ground potential and does not require insulation.

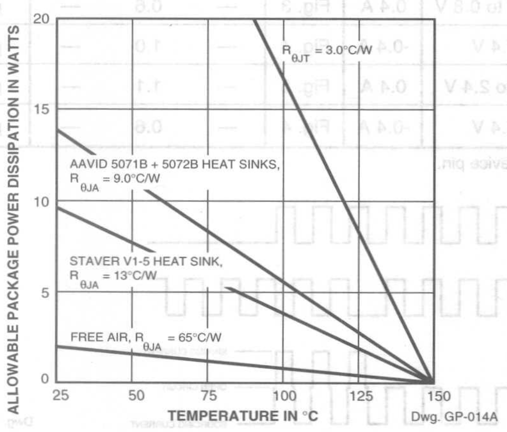
FEATURES

- ±1 A Output Current
- Saturated Output Drivers
- Logic-Compatible Inputs
- Output-Transient Protection
- Tri-State Output
- 8.5 V to 24 V Operating Range
- Crossover-Current Protected
- Withstands 35 V Supply Transients
- Internal Over-Voltage Protection
- Internal Short-Circuit Protection

Always order by complete part number, e.g., **UDN2943Z** .

FUNCTIONAL BLOCK DIAGRAM





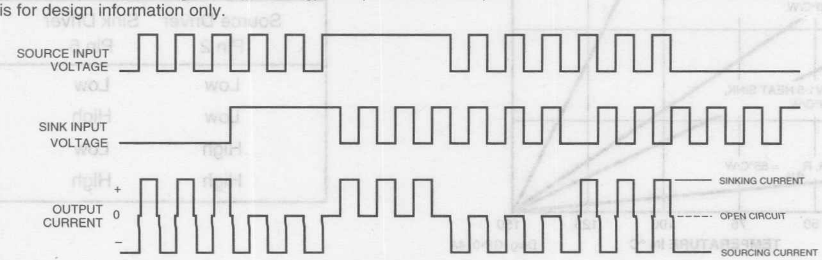
LOGIC TRUTH TABLE

Source Driver Pin 2	Sink Driver Pin 5	Output Pin 4
Low	Low	High
Low	High	High
High	Low	Low
High	High	High Z

ELECTRICAL CHARACTERISTICS at T_A = +25°C (UDN2943Z) or -40°C to +85°C (UDQ2943Z), V_S = +24 V (unless otherwise noted).

Characteristic	Symbol	Source Driver Input, Pin 2	Sink Driver Input, Pin 5	Output Pin 4	Other	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	2.4 V	2.4 V	0 V	—	—	-10	-100	µA
(V_S = +35 V)		2.4 V	2.4 V	35 V	—	—	10	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	2.4 V	0.8 to 2.4 V	1.0 A	Fig. 1A	18	—	—	V
		0.8 to 2.4 V	2.4 V	-1.0 A	Fig. 1B	18	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	0.8 V	2.4 V	-1.0 A	—	—	1.2	1.8	V
		2.4 V	0.8 V	1.0 A	—	—	0.6	1.1	V
Short-Circuit Source Current	I_{SC}	0.8 V	2.4 V	0 V	—	1.0	—	1.8	A
Logic Input Voltage	$V_{IN(1)}$	—	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	—	—	—	—	—	0.8	V
Input Current	$I_{IN(1)}$	2.4 V	2.4 V	NC	—	—	10	100	µA
	$I_{IN(0)}$	0.8 V	0.8 V	NC	—	—	-50	-200	µA
Clamp Diode Forward Voltage	V_F	NC	NC	1.0 A	Fig. 2	—	1.5	2.0	V
Logic Supply Current	I_S	2.4 V	2.4 V	NC	—	—	15	30	mA
		2.4 V	0.8 V	NC	—	—	55	75	mA
		0.8 V	2.4 V	NC	—	—	30	50	mA
Thermal Shutdown Temperature	T_J	—	—	—	—	—	160	—	°C
Over-Voltage Shutdown	V_S	—	—	—	—	24	—	35	V
Propagation Delay	t_{PD}	2.4 V	2.4 V to 0.8 V	0.4 A	Fig. 3	—	0.6	—	µs
		0.8 to 2.4 V	2.4 V	-0.4 A	Fig. 4	—	1.0	—	µs
		2.4 V	0.8 to 2.4 V	0.4 A	Fig. 3	—	1.1	—	µs
		2.4 to 0.8 V	2.4 V	-0.4 A	Fig. 4	—	0.6	—	µs

Notes: Negative current is defined as coming out of (sourcing) the specified device pin.
Typical Data is for design information only.



Dwg. WP-024

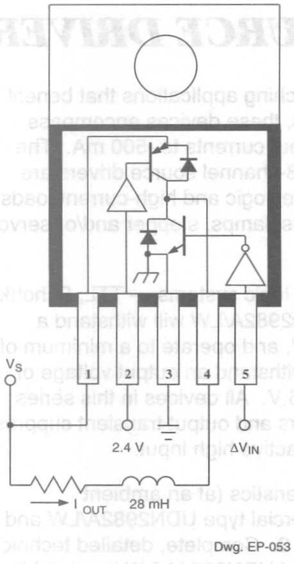


Figure 1A

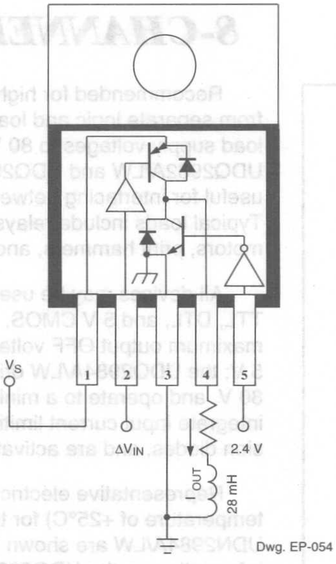


Figure 1B

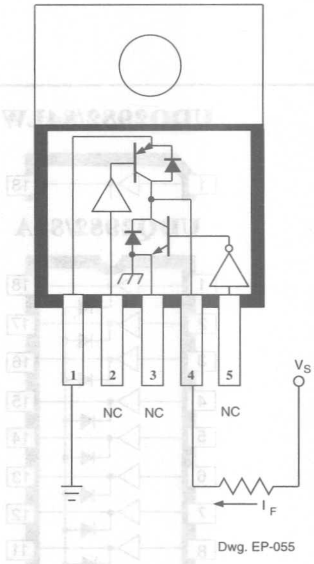


Figure 2

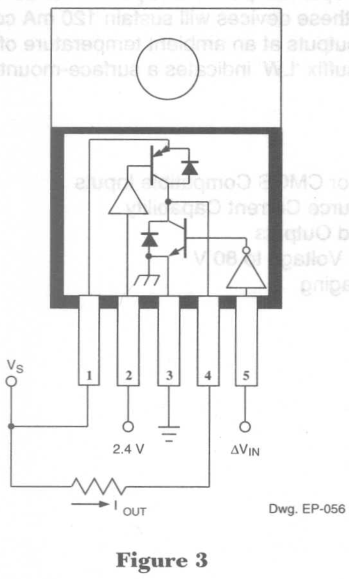


Figure 3

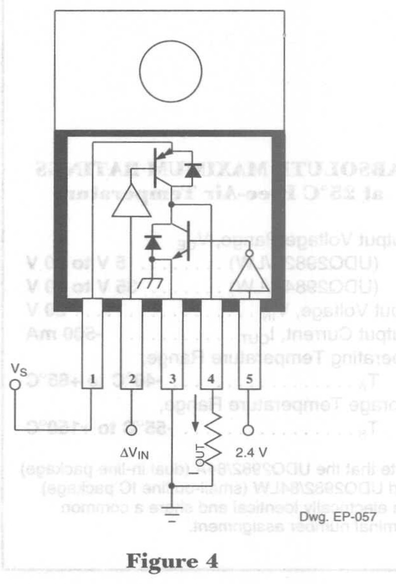


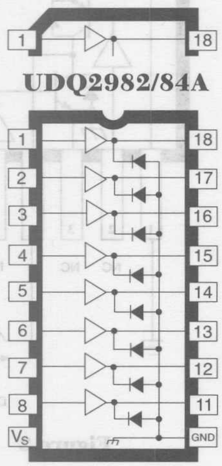
Figure 4

2982 AND 2984

8-CHANNEL SOURCE DRIVERS

UDQ2982/84LW

UDQ2982/84A



Dwg. No. A-10, 243

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage Range, V_{CE}
(UDQ2982A/LW) . . . . **5 V to 50 V**
(UDQ2984A/LW) . . . . **35 V to 80 V**
Input Voltage, V_{IN} . . . . **20 V**
Output Current, I_{OUT} . . . . **-500 mA**
Operating Temperature Range,
T_A . . . . **-40°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**

Note that the UDQ2982/84A (dual in-line package) and UDQ2982/84LW (small-outline IC package) are electrically identical and share a common terminal number assignment.

Recommended for high-side switching applications that benefit from separate logic and load grounds, these devices encompass load supply voltages to 80 V and output currents to -500 mA. The UDQ2982A/LW and UDQ2984A/LW 8-channel source drivers are useful for interfacing between low-level logic and high-current loads. Typical loads include relays, solenoids, lamps, stepper and/or servo motors, print hammers, and LEDs.

All devices may be used with 5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. The UDQ2982A/LW will withstand a maximum output OFF voltage of 50 V, and operate to a minimum of 5 V; the UDQ2984A/LW drivers will withstand an output voltage of 80 V, and operate to a minimum of 35 V. All devices in this series integrate input current limiting resistors and output transient suppression diodes, and are activated by an active high input.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UDN2982A/LW and UDN2984A/LW are shown in Section 3. Complete, detailed technical information on the UDQ2982A/LW and UDN2984A/LW is available on request.

The suffix 'A' indicates an 18-lead plastic dual in-line package with copper lead frame for optimum power dissipation. Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of 15 V. The suffix 'LW' indicates a surface-mountable wide-body SOIC package.

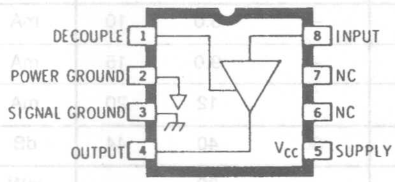
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V
- DIP or SOIC Packaging

3718

27117.25

LOW-VOLTAGE AUDIO POWER AMPLIFIER



Dwg. No. A-11,715

Providing a low-cost, compact alternative to discrete transistor amplifiers, the ULN3718M integrated circuit is ideal for application as a headphone driver in portable radios, tape players, and other battery-operated equipment. The low-power audio amplifier's wide frequency response and low noise ensure premium performance.

The amplifier will operate (at reduced volume) with supply voltages as low as 1.8 V without a significant increase in distortion. This feature allows operation with a 3 V battery supply and minimizes concern about weak batteries. The class-AB audio amplifier has low quiescent current drain for maximum battery life. This device is rated for operation with supply voltages up to 9 V.

The ULN3718M audio amplifier is supplied in an 8-pin mini-DIP plastic package. A copper alloy lead frame gives the amplifier enhanced power dissipation ratings.

FEATURES

- Wide Operating Voltage Range 1.8 - 9.0 V
- Low Quiescent Current
- AC Short-Circuit Protection
- Low External Parts Count
- Low Distortion
- 40 dB Voltage Gain
- Low Noise

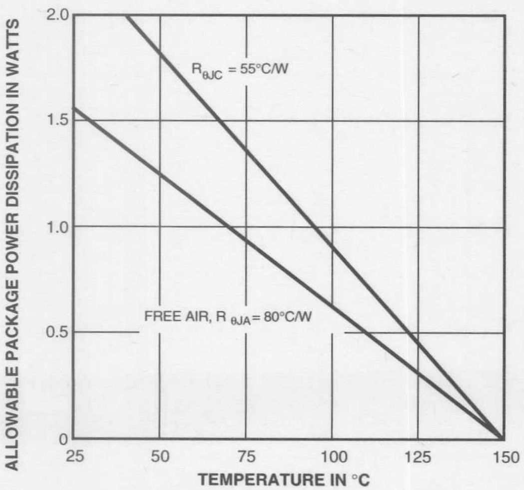
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . **10 V**
Package Power Dissipation,
P_D . . . . **See Graph**
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

Always order by complete part number: **ULN3718M** .

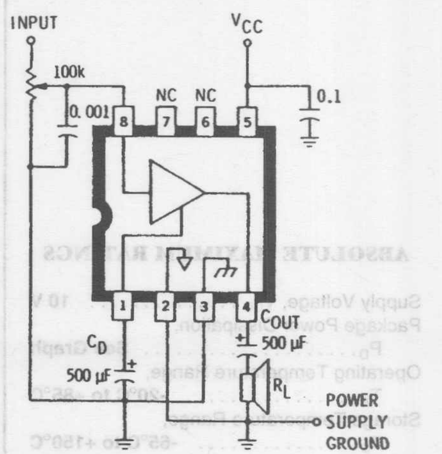
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 3 V, R_L = 32Ω, f_{in} = 400 Hz (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}		1.8	3.0	9.0	V
Quiescent Supply Current	I_{CC}	V_{CC} = 3.0 V	—	6.0	10	mA
		V_{CC} = 6.0 V	—	9.0	15	mA
		V_{CC} = 9.0 V	—	12	20	mA
Voltage Gain	A_V		36	40	44	dB
Audio Power Output	P_{OUT}	R_L = 8Ω, V_{CC} = 3.0 V, THD = 10%	—	80	—	mW
		R_L = 8Ω, V_{CC} = 6.0 V, THD = 10%	250	430	—	mW
		R_L = 32Ω, V_{CC} = 3.0 V, THD = 10%	15	25	—	mW
		R_L = 32Ω, V_{CC} = 6.0 V, THD = 10%	—	125	—	mW
Distortion	THD	P_{OUT} = 10 mW	—	0.3	1.0	%
		P_{OUT} = 1.0 mW, V_{CC} = 1.8 V	—	1.5	3.0	%
Output Noise	V_{out}	Input Shorted, BW = 80 kHz	—	200	500	µV
Input Resistance	R_{IN}	Pin 8	—	250	—	kΩ
Power Supply Rejection	PSRR	C_D (Pin 1) = 500 µF, f = 120 Hz	—	28	—	dB



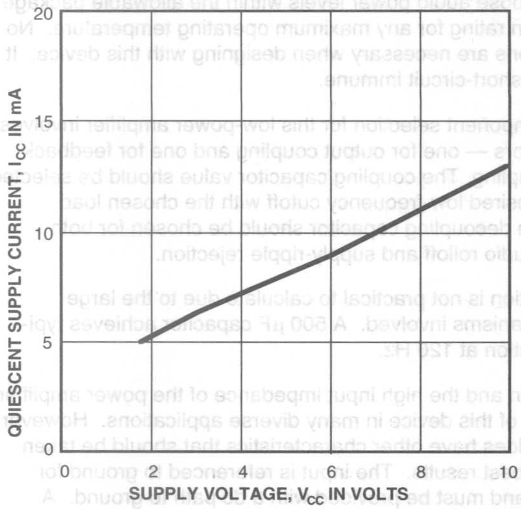
Dwg. No.GP-009-1B

TEST CIRCUIT AND TYPICAL APPLICATION



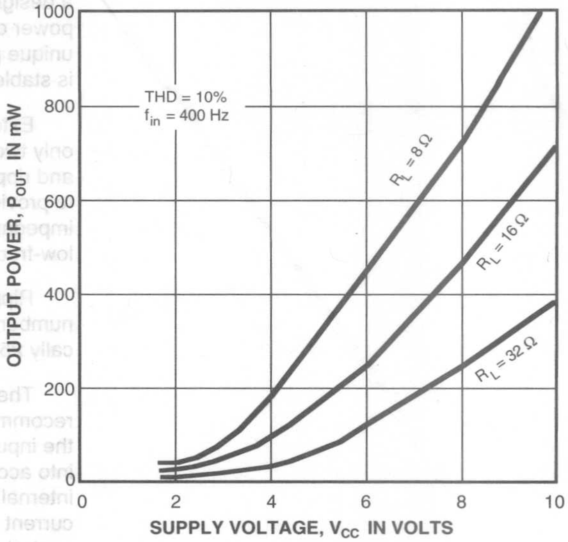
Dwg. No. A-11,716A

TYPICAL CHARACTERISTICS



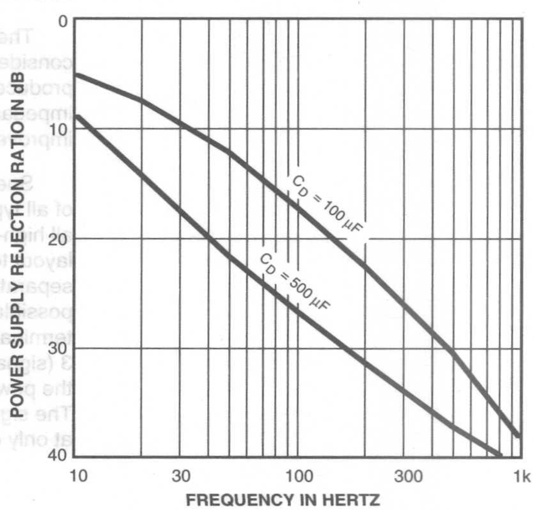
Dwg. No. GS-011

TYPICAL OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE



Dwg. No. GS-010

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREQUENCY



Dwg. No. GS-012

APPLICATIONS INFORMATION

Selection of power-supply voltage and speaker impedance allows a designer to choose audio power levels within the allowable package power dissipation rating for any maximum operating temperature. No unique precautions are necessary when designing with this device. It is stable and ac short-circuit immune.

External component selection for this low-power amplifier involves only two capacitors — one for output coupling and one for feedback and ripple decoupling. The coupling capacitor value should be selected to provide the desired low-frequency cutoff with the chosen load impedance. The decoupling capacitor should be chosen for both low-frequency audio rolloff and supply-ripple rejection.

Ripple rejection is not practical to calculate due to the large number of mechanisms involved. A 500 µF capacitor achieves typically 25 dB rejection at 120 Hz.

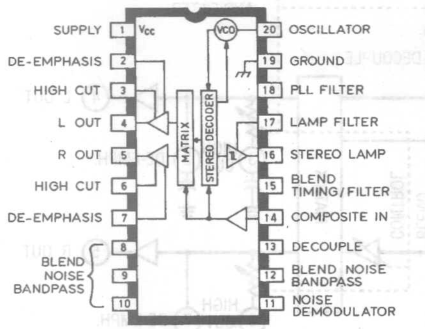
The high gain and the high input impedance of the power amplifier recommend use of this device in many diverse applications. However, the input stage does have other characteristics that should be taken into account for best results. The input is referenced to ground for internal biasing and must be provided with a dc path to ground. A current of typically 1 µA flows from the input through the volume control. This produces an IR drop that is multiplied by the closed loop dc gain of the amplifier and appears as an error in output centering. This recommends a value of 200 kΩ or less for the volume control; values of less than 100 kΩ are preferred.

The selection of amplifier load impedance involves more than just consideration of the desired power output. A low load impedance will produce the highest power output for any given supply voltage. Higher impedances will furnish significant reduction in harmonic distortion and improvement in overall repeatability in power output capacity.

Special steps toward minimizing tendencies towards instabilities of all types were taken in the design of this device. However, as with all high-gain circuits, care should be given to printed wiring board layout to avoid undesirable effects. Inputs and outputs should be well separated and should avoid common-mode impedances wherever possible. For best performance, connect low-level input-signal ground terminals and the decoupling capacitor ground terminal together at pin 3 (signal ground); connect the high-level speaker ground terminal and the power supply ground terminal together at pin 2 (power ground). The signal ground and the power ground should be interconnected at only one point.

3828

FM STEREO DECODER



Dwg. No. PS-011

The A3828EA FM stereo decoder utilizes advanced demodulation techniques for improved performance under adverse receiving conditions. This is particularly important in automotive receivers where the signal strength and multipath effects are continuously changing. It is designed to provide the best possible performance under the widest range of signal conditions while also reducing the cost and complexity of standard FM multiplex receivers. This is accomplished through the use of a dual-bandwidth phase-locked loop and a Walsh function for the regenerated carrier. These two improvements to the carrier recovery system produce the best possible immunity to noise and interference
of any modern PLL stereo decoder under poor signal conditions. The A3828EA is an improved, direct replacement for the ULN3827A.

The dual-bandwidth phase-locked loop switches to a very narrow bandwidth to assure optimal phase stability under noisy reception conditions. Noise-actuated blending adjusts the stereo separation as a function of signal-to-noise ratio to reduce the background noise for low-signal levels and eliminate transition problems at the stereo/mono switch point. The regenerated 19 kHz reference and 38 kHz carrier are free from 3rd and 5th harmonics to improve adjacent channel rejection and signal-to-noise ratio as well as providing good rejection of ARI (Auto Radio Information), RDS (Radio Data System), and other data tones.

The A3828EA is supplied in a 20-pin dual in-line plastic package with a copper lead frame that eliminates many decoupling problems.

FEATURES

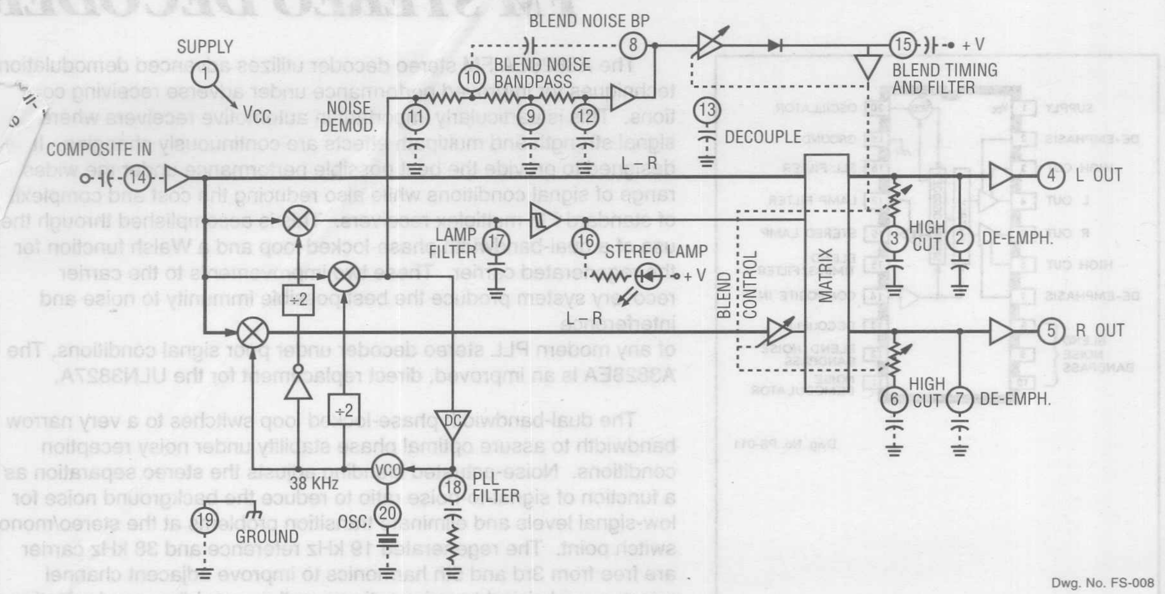
- Reduced Automotive Stereo Multi-Path Effects
- Dual Bandwidth Phase-Locked Loop
- No Adjustments Required
- Improved Adjacent-Channel Rejection
- Good ARI/RDS Rejection
- 19 kHz Pilot Canceling
- Noise-Actuated Blending and High Cut
- Ceramic Resonator Controlled Oscillator
- Automatic Stereo/Mono Switching

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} **13V**
Package Power Dissipation, P_D **1.0W**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

Always order by complete part number: **A3828EA**

FUNCTIONAL BLOCK DIAGRAM



THE ALLEGRO FM STEREO SYSTEM

This new stereo decoder utilizes advanced demodulation techniques for improved performance under adverse receiving conditions. This is particularly important in automotive receivers where the signal strength and multipath effects are continuously changing. The A3828EA FM stereo decoder also reduces the cost and complexity of FM multiplex receivers. It is designed to provide the best possible performance under the widest range of signal conditions. This is accomplished through the use of a variable-bandwidth phase-locked loop and the use of a Walsh function for the regenerated carrier.

Prior integrated stereo decoders utilized a loop bandwidth of typically 300 Hz, which was a compromise between acquisition performance and carrier recovery. Acquisition is generally satisfactory with this bandwidth, however, carrier recovery integrity often degrades under noisy conditions; in the worst case to complete loss of carrier. This is more apparent under multipath conditions. Although this is not the only noise observed under multipath events, it is a real source of disturbance. A secondary feature of the wider bandwidth is a peak in L – R distortion at the loop resonance frequency at 9.5 kHz. Clearly, to provide optimal performance, the loop bandwidth should be subaudible. To provide reasonable acquisition times, the A3828EA phase-locked loop is operated in a wide-band mode until carrier acquisition. Upon capture, the loop is then switched to a narrowband mode (typically 20 Hz) to provide superior noise immunity under adverse signal conditions.

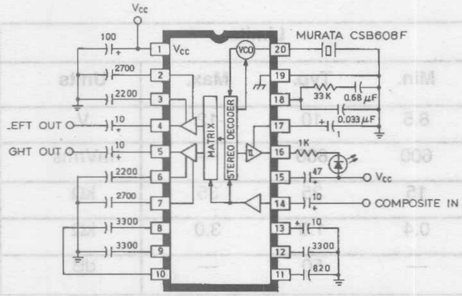
Currently available stereo decoders generate square waves for the regenerated 19 kHz pilot and 38 kHz carrier. Although this is convenient from the standpoint of circuit design, the spurious response of the receiver, as observed at RF, exhibits a sine n/n spurious response pattern centered about the received frequency and spaced at 38 kHz intervals. The most detrimental harmonic is the 5th, located at 190 kHz, since this spurious seriously degrades adjacent channel rejection. The preferred technique for eliminating these spurious responses would be the use of a pure sine-wave regenerated carrier.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 10.0V, Composite Input = 400 mVrms (L = R, pilot OFF), Pilot Level = 40 mVrms, f_m = 1 kHz, unless otherwise specified.

Characteristic	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	Functional	8.5	10	12	V
Max. Composite Input	THD = 1.0 %	600	800		mVrms
Input Impedance		15	25	35	kΩ
Output Impedance		0.4	1.0	3.0	kΩ
Stereo Channel Separation (100 Hz to 1 kHz)	f_m = 100 Hz	—	50	—	dB
	f_m = 1.0 kHz	30	50	—	dB
	f_m = 10 kHz	—	40	—	dB
Monaural Gain	19 kHz Pilot Level = 0	- 0.4	0.6	1.6	dB
Monaural Channel Balance	19 kHz Pilot Level = 0	—	0	±1.0	dB
Total Harmonic Distortion	19 kHz Pilot = 0	—	0.05	0.5	%
	L or R only	—	0.1	0.5	%
Ultrasonic Frequency Rejection	19 kHz	36	51	—	dB
	38 kHz	35	45	—	dB
SCA Rejection	67 kHz (Note 2)	55	65	—	dB
Spurious Response	114 kHz, 10% modulation	—	65	—	dB
	190 kHz, 10% modulation	—	65	—	dB
PLL Bandwidth	Loop Locked	—	20	—	Hz
Stereo Switch Level	19 kHz Pilot Only, Lamp ON	10	15	22	mVrms
	19 kHz Pilot Only, Lamp OFF	6.0	11	16	mVrms
Stereo Lamp Hysteresis	Lamp OFF to Lamp ON	—	3.0	—	dB
Capture Range	Pilot = 6.0 mV	—	300	—	Hz
Lock Range	Pilot = 20 mV	—	300	—	Hz
Blend Threshold	S+N/N	—	36	—	dB
Stereo Lamp Output Current	Short Circuit, Lamp ON	5.0	20	40	mA
	Lamp OFF, V_{CC} = 12 V	—	< 0.1	3.0	µA
Quiescent Supply Current	Lamp OFF	—	22	35	mA

NOTES: 1) Typical values are given for circuit design information only.
2) Measured with a stereo composite signal of 80% stereo, 10% pilot, and 10% SCA.

TEST CIRCUIT AND TYPICAL APPLICATION



POLARIZED CAPACITANCE VALUES ARE IN µF, NON-POLARIZED CAPACITANCE VALUES ARE IN pF, UNLESS OTHERWISE INDICATED.

Dwg. No. ES-010

The typical application and circuit constants herein are included only as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by Allegro MicroSystems for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

However, this is impractical using digital carrier regeneration techniques. A more conveniently implemented method is the Walsh function which is a digital technique for generating the odd-ordered harmonics in a waveform that can be subtracted from the square wave to produce a sine-wave approximation. This avoids much of the previously described spurious responses. The implementation of this function is relatively easy in a modern stereo decoder employing a high-frequency ceramic resonator for the oscillator since the required divider can readily produce the Walsh function as a side product.

This stereo decoder also incorporates a noise-operated blending system that is completely contained within the chip. Other devices with signal-strength operated blending are frequently fooled into full stereo operation by strong but poor quality signals during multipath events. The noise-operated blending system is also actuated by environmentally generated and multipath-induced noise since the system is based exclusively on signal-to-noise ratio as observed at the FM detector output . Since the technique of blending on noise is inherently more repeatable than signal-strength based blending, production blend adjustments are not required.

In addition to the advanced features previously described, the A3828EA decoder uses a ceramic oscillator to eliminate the last remaining adjustment. Forced mono can be accomplished externally which also stops the oscillator.

Implementation is in DABiC, which is a bipolar plus CMOS process. It has the advantages of low-noise linear circuitry and CMOS logic that is dense (for reduced cost) and fully characterized for operation over a very-wide temperature range.

PIN FUNCTIONS

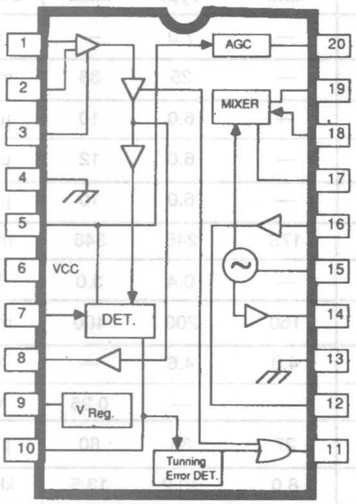
Pin	DC Voltage	Function	Notes
1	10.0	Supply	–
2	4.0	Left De-Emphasis	R_S = 27.8 kΩ
3	4.3	Left High Cut	R_S = 20 kΩ
4	3.4	Left Output	R_S = 1 kΩ
5	3.4	Right Output	R_S = 1 kΩ
6	4.3	Right High Cut	R_S = 20 kΩ
7	4.0	Right De-Emphasis	R_S = 27.8 kΩ
8	3.0	Blend Capacitor	–
9	3.7	Blend Capacitor	–
10	4.4	Blend Capacitor	–
11	5.1	Blend Capacitor	–
12	5.4	Blend Capacitor	–
13	5.4	Blend Decouple	–
14	3.6	Composite Input	R_{IN} = 25 kΩ [1]
15	8.3	Blend Timing & Filter	[2]
16	9.0	Stereo Indicator	Locked = 0.1 V
17	5.0	Lock Detector Filter	Locked = 4.7 V
18	5.6	Loop Filter	Locked = 4.7 [3]
19	0.0	Ground	–
20	9.0	608 kHz Resonator	–

NOTES 1) The decoder matrix does not account for FM detector frequency roll-off. An input RC network can be used to correct for this if separation is not sufficient.
2) Blend threshold can be increased to about 42 dB (but separation will be reduced at lower levels) by adding 470 kΩ to V_{CC}. Smaller values will cause blending when it is not desired.
3) The loop filter capacitor should be low-leakage current because the phase detector output current is very low.

3841

27121.11A

AM SIGNAL PROCESSOR



Providing the AM signal processing functions for an electronically-tuned AM receiver (ETR), the ULN3841A includes a balanced mixer, buffered local oscillator, IF amplifier, AM detector, scan control detectors, and a switchable voltage regulator. The addition of a JFET matched to a whip antenna, RF tuning components, IF selectivity, and audio stages gives a complete AM radio which can be used in automotive receivers. Additional applications are in high-quality home entertainment receivers (especially with the addition of an AM stereo decoder) and scanning-type shortwave receivers. The frequency-detecting stop circuit is also capable of recovering narrow-band FM, making it useful for scanners or weatherband radio applications.

The ULN3841A has a greatly improved stop detection system over other existing devices. It uses the dual criteria of frequency and amplitude for establishing a valid stop. Tuning accuracy (frequency criteria) is established by evaluating phase shift across the detector coil. The circuitry is similar to that used in FM discriminators. Since this detection system is phase operated, it remains effective even in the presence of strong signals, which can cause false stops in systems using narrow-band filters. The amplitude criterion for stop is determined by evaluating the IF level. It includes a unique circuit that removes the effect of the AGC action. This allows the AGC tuning components to be selected for low-frequency audio performance without compromising scanning speed.

These AM signal processors are packaged in 20-pin plastic DIPs and are rated for operation over the temperature range of -40°C to +85°C.

FEATURES

- Low Noise Figure
- Balanced Mixer
- Buffered Local Oscillator
- Improved 'Stop' Detector
- Wide-Band AGC
- Delayed AGC
- Narrow-Band FM Output
- Low Supply Current
- 7 to 16 Volt Operation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... **18 V**
Package Power Dissipation, P_D . . . **1.18 W**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

Always order by complete part number: **ULN3841A** .

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 14.4 V, f_o = 1 MHz, f_{if} = 450 kHz, f_m = 1 kHz at 30% AM (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Minimum Operating Voltage	V_6		—	7.0	—	V
Quiescent Supply Current	I_{CC}	No Signal	—	25	33	mA
Sensitivity	V_{in}	V_{OUT} = 50 mV	—	6.0	10	µV
		V_{CC} = 11 V	—	6.0	12	µV
Usable Sensitivity	V_{in}	S + N/N = 20 dB	—	6.0	10	µV
Recovered Audio	V_{OUT}	V_{in} = 1 mV	173	245	346	mV
Total Harmonic Distortion	THD	V_{in} = 1 mV, 80% AM	—	0.4	3.0	%
Oscillator Output Voltage	V_{out}		150	200	400	mV
Stop Output Voltage	V_{11}	V_{in} = 0	4.3	4.6	—	V
		V_{in} = 1 mV	—	—	0.25	V
Stop Sensitivity	V_{in}	V_{11} = 1.5 V, 0% AM	27	35	80	µV
Stop Bandwidth		V_{in} = 10 mV, V_{11} = 1.5 V, 0% AM	8.0	10.2	13.5	kHz
Wide-Band AGC	V_{agc}	V_{in} = 0	—	—	0.20	V
		V_{in} = 60 mV	2.0	—	—	V
Overload	V_{in}	THD = 10%, 80% AM	25	70	—	mV
Input Limiting Threshold	V_{TH}	Pin 10, Δf = ±3 kHz, -3 dB	—	12	—	µV
FM Recovered Audio	V_{10}	Δf = ±3 kHz, f_m = 50 Hz	—	380	—	mV
Signal-to-Noise Ratio	S + N/N	V_{in} = 250 µV	45	50	—	dB
		V_{in} = 10 mV	—	60	—	dB
AGC Figure of Merit	V_{in}	ΔV_{OUT} = -10 dB ref. V_{in} = 5 mV	4.2	6.0	8.4	µV
Delayed AGC Voltage	V_{17}	V_{in} = 0	1.5	1.65	1.8	V
		V_{in} = 1 mV	0.6	0.85	1.2	V
Regulator Voltage	V_9		—	5.1	—	V
		Pin 20 Grounded (Muted)	—	—	0.6	V

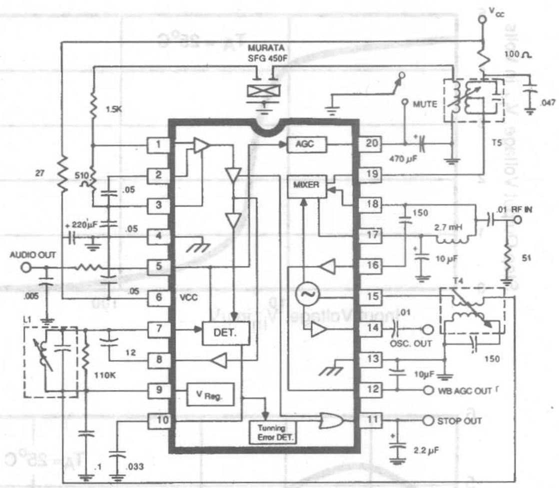
3841
AM SIGNAL PROCESSOR

Small-Signal AC Parameters at T_A = +25°C, V_{CC} = 14.4 V, f_o = 1 MHz, f_{if} = 450 kHz

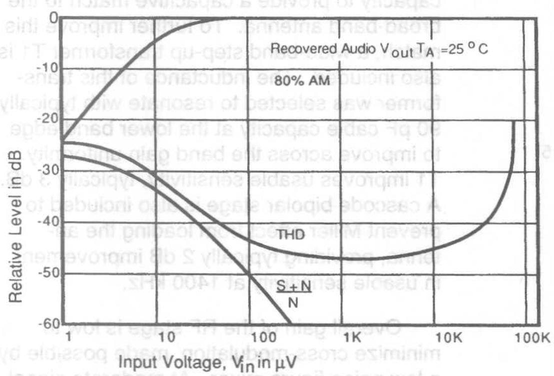
Characteristic	Pins	Typical Value
MIXER		
Input Resistance	18	5 kΩ
Input Capacitance	18	20 pF
Transconductance	18 to 19	4 mmho
Output Resistance	19	75 kΩ
Output Capacitance	19	4 pF
IF		
Input Resistance	1	8 kΩ
Input Capacitance	1	7 pF
Voltage Gain	1 to 8	54 dB
Output Resistance	8	45 Ω

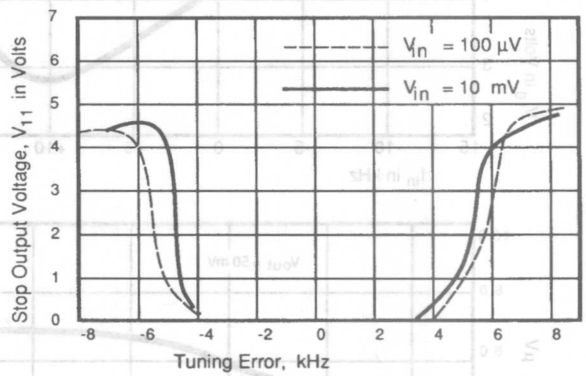
Typical values are given for circuit design information only.

TEST CIRCUIT

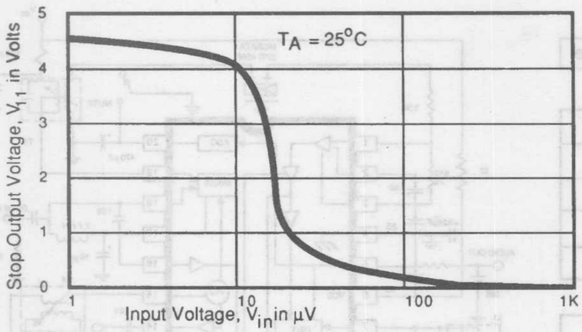


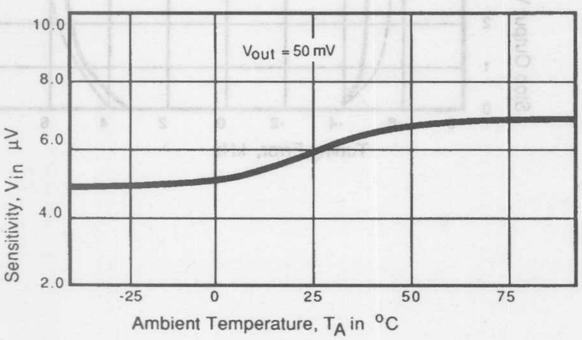
TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS





A HIGH-PERFORMANCE ELECTRONICALLY-TUNED AM STEREO RECEIVER FOR AUTOMOTIVE APPLICATION USING THE ULN3841A

The advent of AM stereo has changed the perception of AM as a low-fidelity medium. This has caused a revaluation of AM receiver performance objectives, particularly minimum audio bandwidth. To achieve satisfactory stereo imaging, a minimum high-frequency response of 4 kHz has been shown to be necessary. Additionally, AM stereo has imposed the totally new requirements of phase linearity and freedom from incidental phase noise and modulation.

RF SECTION

RF gain is provided by a large-area JFET, selected for high gate-to-channel capacity to provide a capacitive match to the broad-band antenna. To further improve this match, a wide-band step-up transformer T1 is also included. The inductance of this transformer was selected to resonate with typically 90 pF cable capacity at the lower band edge to improve across the band gain uniformity. T1 improves usable sensitivity, typically 3 dB. A cascode bipolar stage is also included to prevent Miller effect from loading the antenna, providing typically 2 dB improvement in usable sensitivity at 1400 kHz.

Overall gain of the RF stage is low to minimize cross-modulation, made possible by a low noise figure mixer. At moderate signal levels, cross-modulation is primarily limited by the performance of the JFET. At higher levels, wide-band AGC is applied to a clamp transistor at the antenna. This signal is derived from the secondary of T2 and is rectified and amplified by the ULN3841A.

A wider RF bandwidth is used to reduce the effects of mistracking and misalignment on stereo separation and distortion. The

overall bandwidth (audio response) and band shape of the receiver should be determined by the IF selectivity.

To achieve widest bandwidth with minimum sacrifice in out-band selectivity, a double-tuned section was selected, T2 and T3. To further enhance bandwidth vs. selectivity performance across the band, a combination of frequency-dependent loading and coupling is used. The 330 μH choke is used as top coupling and is constant across the band; the .047 μF capacitor is a bottom-coupling element which decreases coupling with increasing frequency. The varactor diode series-loading resistors (6.8Ω) are also employed to reduce Q at the lower end of the band. This produces typical 6 dB bandwidths of 18.6 kHz at 600 kHz and 24 kHz at 1400 kHz. Variable coupling also reduces gain variation across the band (ref. 1).

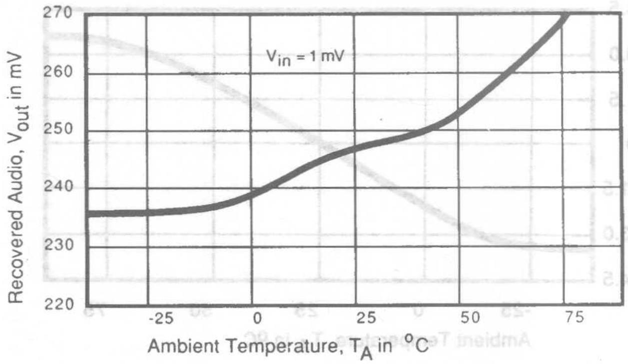
MIXER AND IF

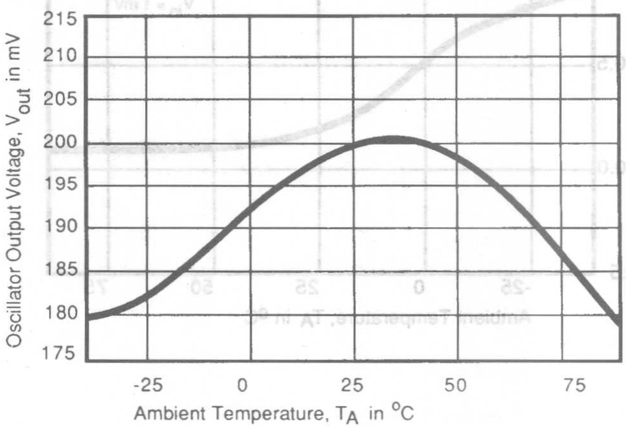
The output from the double-tuned RF is applied to the balanced mixer, pin 18, which is biased from pin 17. Output from the mixer is taken via T5. The primary impedance is 15 kΩ. Secondary and Q are selected for the ceramic filter which was chosen for stereo performance and bandwidth. This filter has a quasi-parabolic band pass and reasonably constant group delay. Termination resistors at pin 1 are configured as a pad to permit adjustment of overall gain.

The detector coil (L1) serves as the AM detector and also establishes the stop bandwidth. Tuning accuracy is established by evaluating phase shift across the detector coil employing circuitry similar to that used in FM discriminators. Stop phase criteria is internally set to one-half the 3 dB bandwidth (f_{if}/2x loaded Q) of L1. The value in the application is 20. This circuit also recovers narrow-band FM at pin 10.

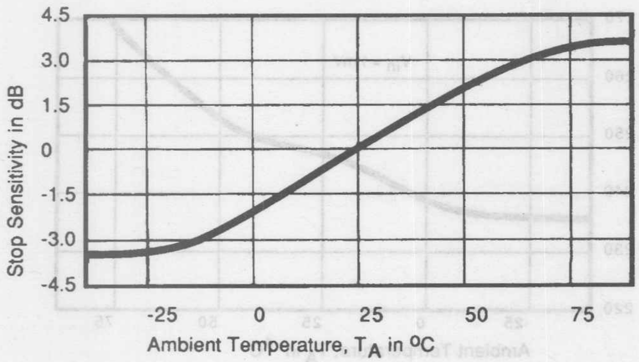
AGC rate is selected for audio performance. AGC action is removed from the stop circuit, which effectively eliminates the trade-off between AGC performance and permitted scanning rate. Monaural output is provided in this application for alignment and evaluation. If the monaural output is not required the 10 kΩ and .005 μF components can be deleted without affecting stereo performance. In this application the ULN3841A stop detector output (pin 11) is applied through a time delay to the AM stereo decoder force monaural input to reset the decoder counters during the tuning. The IF signal for the decoder is taken out at the detector coil.

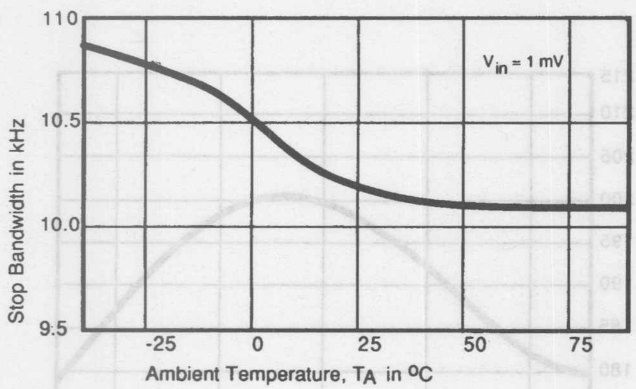
TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS





STEREO DECODER

The component values used with the AM stereo decoder are based on the applications information as given elsewhere. Note that the pilot-tone and co-channel components should be precision as shown (ref. 2, 3).

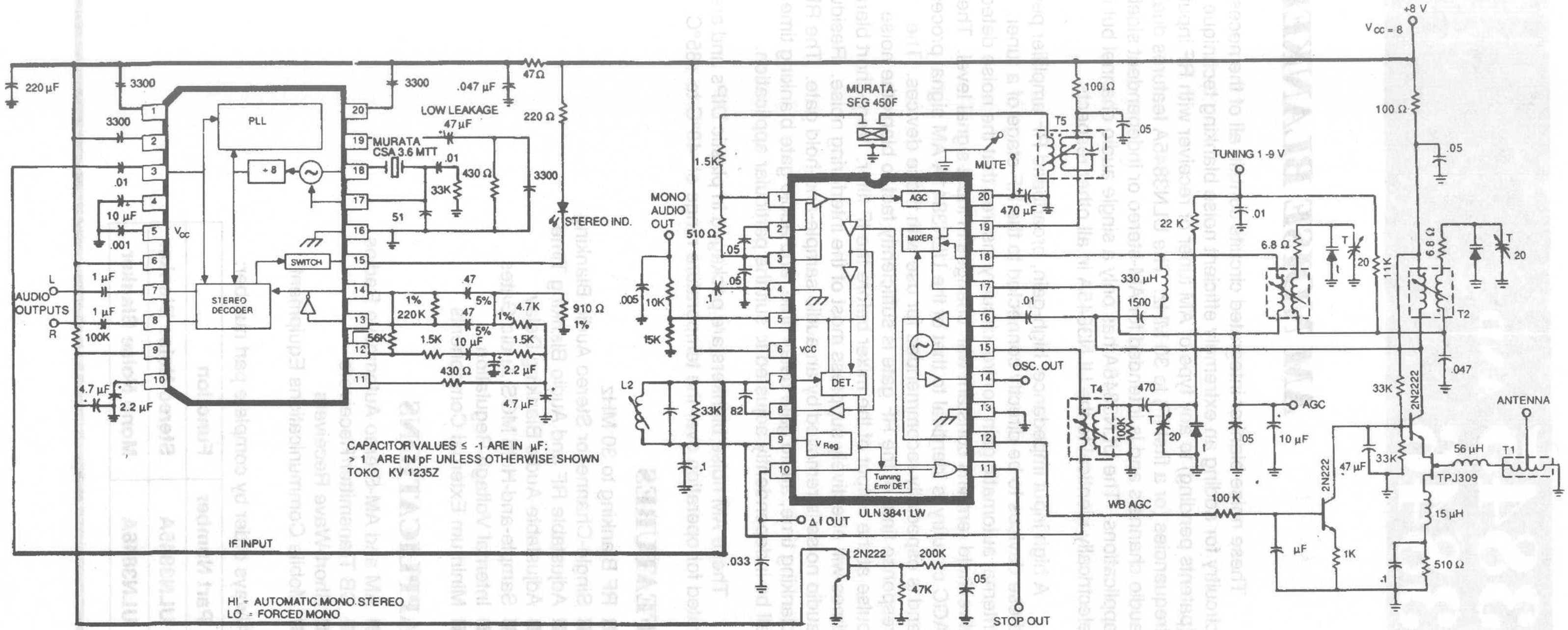
REFERENCES

1. "Development of High Quality Receiver for AM Stereo" by Jon P. Grosjean and Oliver Richards, publication TP80-5.

2. "Pilot-Tone Band-Pass Filter Circuit Component Tolerance Considerations," Motorola, publication M68465.

3. "VCO and Phase-Lock Loop Performance," Motorola publication M684131.

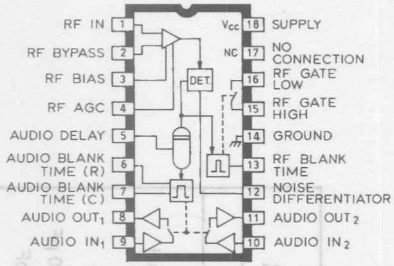
AM STEREO RECEIVER FOR AUTOMOTIVE APPLICATION



	Symbol	Q	N1/N2	N1/N3	Toko Part Number
COIL INFORMATION FOR TEST CIRCUIT AND HIGH-PERFORMANCE ETR AM STEREO RECEIVER					
Antenna	T1		1:1.6		7HN-60064CY
RF	T2, T3	120		10:1	RWOS-6A7894A0, L = 178 µH
Local Osc.	T4	120		5:1	7TRS-A5609A0
Mixer	T5		2:1	8.9:1	7LC-502112N4, C_T = 180 pF
Detector (test)	L1	100			7NRES-A5622AAG, C_T = 100 pF
(application)	L2	100			A7BRS-T1041Z, C_T = 1000 pF

AM NOISE BLANKERS

ULN3845A



Dwg. No. PS-003

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 12 V
Package Power Dissipation,
P_D . . . . 880 mW
Operating Temperature Range,
T_A . . . . -40°C to +125°C
Storage Temperature Range,
T_S . . . . -55°C to +125°C

These noise blanker integrated circuits contain all of the necessary circuitry for adding an extremely efficient noise blanking technique (patents pending) to any type of AM tuner or receiver with RF input frequencies (or a first IF) to 30 MHz. The ULN3845A features dual audio channels and is intended for AM-stereo or independent sideband applications. The ULN3846A has only a single audio channel but is electrically identical to the ULN3845A in all other respects.

A high input impedance, high-gain, broadband RF amplifier permits these devices to be directly connected to the RF stage of a tuner. The internal automatic gain control circuitry insures that the noise detection threshold remains constant with changes in input signal level. The AGC circuitry is identical to that of the ULN3841A AM signal processor and is especially recommended for use with those devices. The response time of the RF gate is sufficiently fast to blank the noise pulse at the output of the mixer before the IF filter. Very-short blanking times will effectively suppress most of the interfering noise. Residual audio noise is removed by an audio sample-and-hold gate. The RF blanking time, audio gate delay time, and audio gate blanking time can all be independently adjusted to suit the particular application.

These AM noise blankers are packaged in plastic DIPs and are rated for operation over the temperature range of -40°C to +85°C.

FEATURES

- RF Blanking to 30 MHz
- Single-Channel or Stereo Audio Blanking
- Adjustable RF and Audio Blanking Time
- Adjustable Audio Blanking Delay
- Sample-and-Hold MOS Audio Gates
- Internal Voltage Regulation
- Minimum External Components

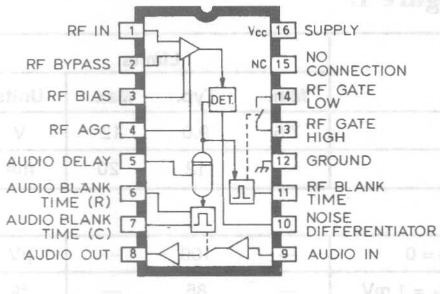
APPLICATIONS

- AM and AM-Stereo Automotive Radios
- CB Transmitter/Receivers
- Short-Wave Receivers
- Mobile Communications Equipment

Always order by complete part number:

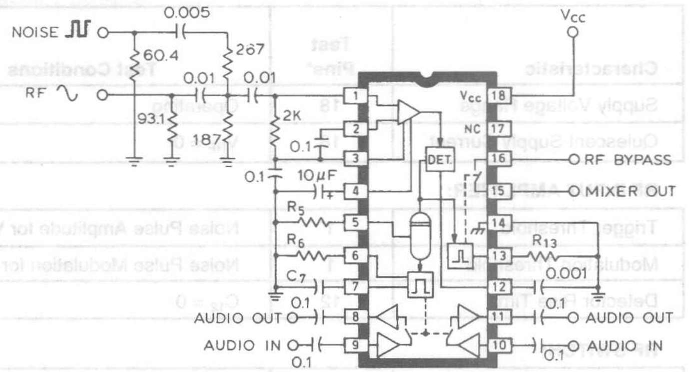
Part Number	Function
ULN3845A	Stereo Noise Blanker
ULN3846A	Mono Noise Blanker

ULN3646A



Dwg. No. PS-004

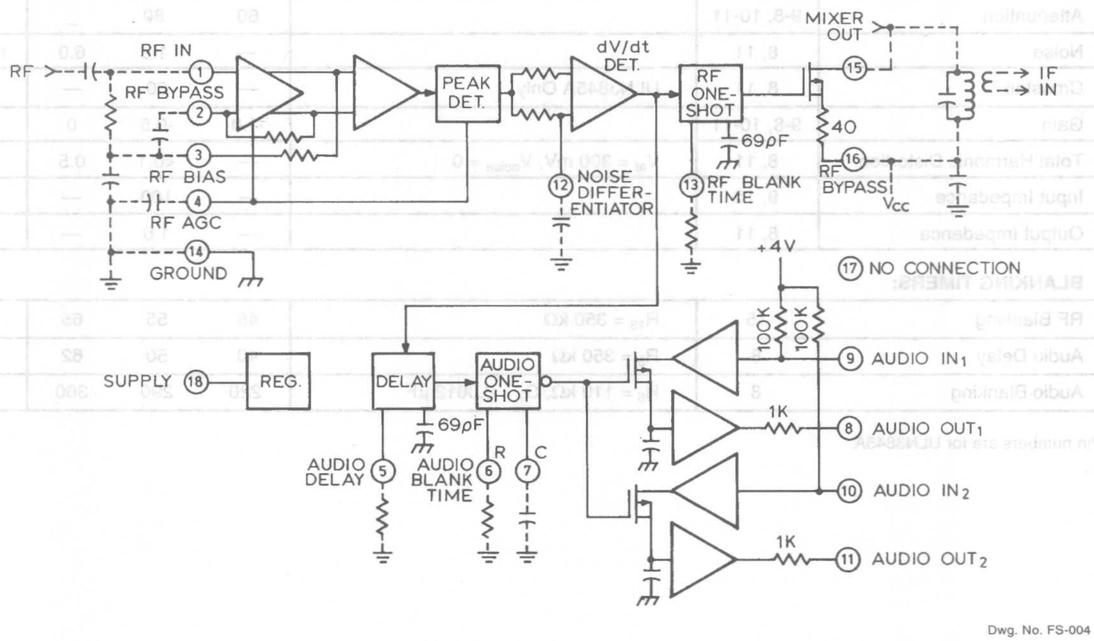
TEST CIRCUIT
FIGURE 1



Dwg. No. ES-007

Note that the noise-pulse input is attenuated 20 dB by the test circuit.

FUNCTIONAL BLOCK DIAGRAM
(ULN3845A)



Dwg. No. FS-004

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 9 V, f_{rf} = 1 MHz, Noise (f_{noise}) = 500 Hz Square Wave, f_{af} = 1 kHz, Test Figure 1.

Characteristic	Test Pins*	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	18	Operating	7.5	9.0	12	V
Quiescent Supply Current	18	V_{RF} = 0	—	12	20	mA
RF INPUT AMPLIFIER:						
Trigger Threshold	1	Noise Pulse Amplitude for V_{RF} = 0	—	100	—	µV
Modulation Threshold	1	Noise Pulse Modulation for V_{RF} = 1 mV	—	85	—	%
Detector Rise Time	12	C_{12} = 0	—	500	—	ns
RF SWITCH:						
ON Resistance	15-16		—	50	70	Ω
OFF Resistance	15-16		—	100	—	kΩ
Time Delay	1-15	From Beginning of RF Pulse to Beginning of RF Blanking	—	1.5	3.0	µs
AUDIO SWITCHES:						
Attenuation	9-8, 10-11		60	80	_	dB
Noise	8, 11		—	1.5	6.0	mVpp
Crosstalk	8, 11	ULN3845A Only	—	60	—	dB
Gain	9-8, 10-11		-1.0	-0.5	0	dB
Total Harmonic Distortion	8, 11	V_{af} = 300 mV, V_{noise} = 0	—	<0.1	0.5	%
Input Impedance	9, 10		—	100	—	kΩ
Output Impedance	8, 11		—	1.0	—	kΩ
BLANKING TIMERS:						
RF Blanking	15	R_{13} = 350 kΩ	45	55	65	µs
Audio Delay	8	R_5 = 350 kΩ	40	50	62	µs
Audio Blanking	8	R_6 = 110 kΩ, C_7 = 0.0012 µF	220	290	360	µs

*Pin numbers are for ULN3845A.

CIRCUIT DESCRIPTION

Previous attempts at suppression of impulse noise in AM receivers have used a variety of approaches ranging from gating the signal OFF at the antenna to simply clipping (limiting) any signal that was larger than the average modulation. Unfortunately, the former can generate as much noise as it removes while the latter only reduces the level of noise impulses and does not remove them.

A major problem in attempting to suppress impulse noise in an AM receiver can best be described by looking at the shape of a noise pulse as it passes through a typical tuner as shown in Figure 2. Here, a typical 0.5 μs pulse is applied to the antenna input. The resulting waveforms are essentially the impulse response of the different selectivity sections as limited only by the dynamic range of the individual sections. Note that the signal remains quite narrow until the IF filter is reached. Because of the relatively narrow bandwidth of the IF filter, the limiting of the IF amplifier, and the filtering effect of the detector, the audio output resulting from the impulse is much wider than the original input pulse and is therefore much more objectionable.

One blanking scheme currently in use senses the noise pulse in the IF amplifier and blanks the audio output. This results in a long blanking time and poor performance at the higher frequencies where a short blanking time is needed most.

The ULN3845A and ULN3846A take a different approach to the noise suppression problem by sensing the noise pulse in the receiver's RF section and blanking the pulse before it reaches the IF. This requires a noise amplifier with a minimum propagation delay and high-speed gating.

Blanking the noise pulse in this way is very effective, but some of the interference can still reach the audio output due to the loss of carrier during the blanking interval.

QUIESCENT DC VOLTAGES
(FOR CIRCUIT DESIGN INFORMATION ONLY)

Pin Number			Typical
ULN3845A	ULN3846A	Pin Function	DC Voltage
1	1	RF In	3.1
2	2	RF Bypass	3.1
3	3	RFBias	3.1
4	4	RF AGC	0.9
5	5	Audio Delay	4.8
6	6	Audio Blank Time (R)	4.8
7	7	Audio BlankTime (C)	4.8
8	8	Audio Out_x	4.75
9	9	Audio In_x	4.0
10	—	Audio In_2	4.75
11	—	Audio Out_2	4.0
12	10	Noise Differentiator	4.9
13	11	RF Blank Time	4.8
14	12	Ground	Reference
15	13	RF Gate High	—
16	14	RF Gate Low	—
17	15	No Connection	0
18	16	Supply	V_{CC}

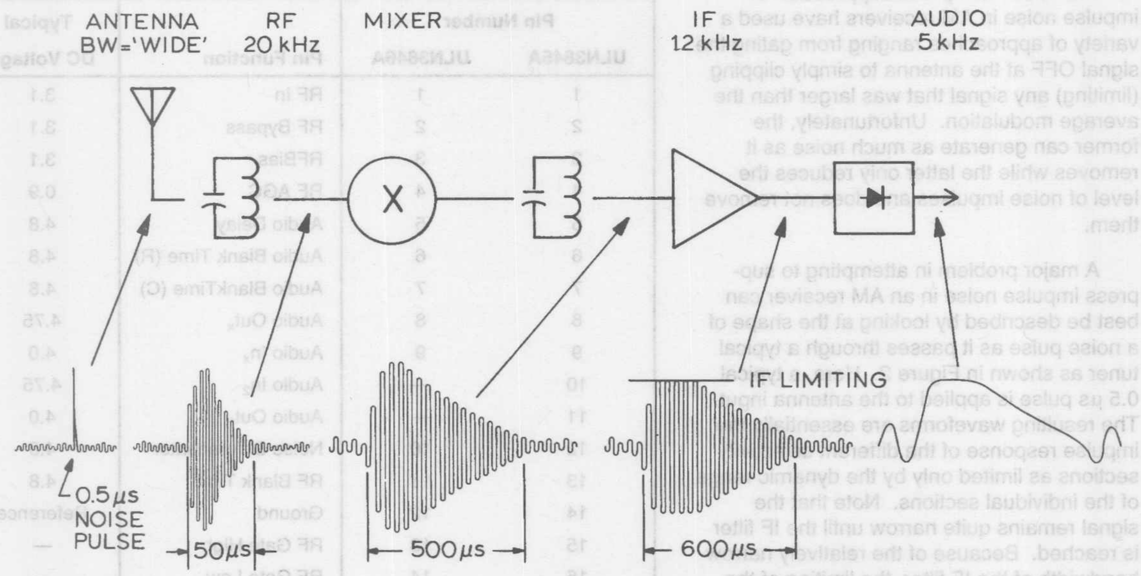
For this purpose, an additional delay, blanking interval, and audio gate (or gates in the case of the ULN3845A) are included to further suppress any residual signal. The result is almost 100% suppression of impulse noise including that from ignition systems and from sources producing interference at a power line rate such as light dimmers and fluorescent lamps.

Referring to the Functional Block Diagram, the RF input stage is a differential amplifier, so that the input impedance is high. The triggering threshold at the RF amplifier input is about 15 μV at 1 MHz. This means that a pulsed RF input signal of 15 μV will exceed the threshold and trigger the blanker. The external capacitor at the dV/dt detector circuit (C_{12}) is selected so that audio signals do not cause triggering. At high input levels, the threshold is internally set so that an RF burst of 50% modulation triggers the blanker. A resistor in parallel with C_{13} will increase the detection threshold level.

The RF-switching MOSFET (pins 15-16) is controlled by the RF one-shot whose gate time is determined by the value of R_{13}.

RF Gate Time (μs) = $157 \times 10^{-12} \times R_{13}$

TYPICAL PULSE RESPONSE
FIGURE 2



Dwg. No. OS-001

where R_{13} should be greater than 33 kΩ. Smaller values for C_{12} will reduce the sensitivity to RF input pulses. The MOSFET turns ON within approximately 1.5 µs (shunting the RF signal to ground) after a noise pulse is detected and then turns OFF over a 15 µs period after the end of the RF gate time. The ON resistance of the MOSFET is about 40 Ω. The slow turn-OFF prevents any additional transients from being introduced into the receiver by the RF gate. The internal gate circuit also includes charge-balancing circuits so that switching transients are canceled and do not appear at the output. These features ensure transient-free switching even when the RF gate is connected to the low-level input stages of a receiver. Note that the RF gate must be connected to a supply to obtain the minimum ON-resistance of the MOSFET gate. This makes it convenient to connect the RF gate in parallel with the receiver mixer output transformer primary.

Blanking in the RF or mixer sections of the receiver removes most of the noise pulse but a small amount still remains due to the hole punched in the carrier. This residual noise is theoretically somewhere between the peak audio and 100% negative modulation but is significantly smaller and narrower than that which the impulse would normally produce without blanking. An audio delay, one-shot, and audio gate(s) are included to eliminate this residual signal.

The audio delay is determined by the value of R_5:

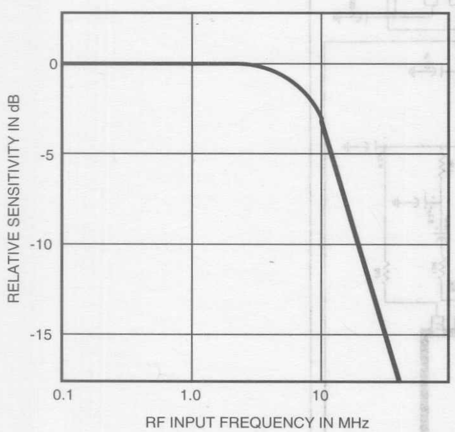
Audio Gate Delay (µs) = $143 \times 10^{-12} \times R_5$

where R_5 should be greater than 33 k. The amount of delay required will depend on the IF filtering characteristics of the particular receiver design. After the audio delay time, the audio one-shot is triggered. The audio switching MOSFETs (pins 8-9 and pins 10-11) are controlled by the audio one-shot whose gate time is determined by the values of R_5 and C_7:

Audio Gate Time (µs) = $2.2 \times R_6 \times C_7$

The MOSFET audio gates also include charge-balancing circuits to eliminate switching transients.

TYPICAL RF FREQUENCY RESPONSE



Dwg. No. GS-006

TYPICAL APPLICATION

A typical application using the ULN3845A in a C-QUAM® AM stereo car radio tuner is shown in Figure 3. Although there is a 1.5 µs delay from the beginning of the noise pulse to the start of blanking, this is small compared with the impulse response time of the receiver. It takes almost 10 µs for the RF noise burst to reach 70% amplitude at the mixer input. The blanker RF input could have been connected to the collector of the discrete RF amplifier, but the bandwidth is much wider there and false triggering from strong adjacent channel signals could occur.

The ULN3845A and ULN3846A noise blankers can also be used in dual-conversion AM tuners. The blanker RF input would then be connected at the first IF amplifier input and the blanker RF gate connected at the second mixer output. Since the first IF band-width is usually relatively wide, the noise pulses are narrower, and the RF blanking time will be correspondingly less. In this case, it may be necessary to reduce the value of capacitor C_{12} so that the noise separator does not extend the RF blanking time.

COIL INFORMATION FOR HIGH-PERFORMANCE ETR AM STEREO RECEIVER WITH NOISE BLANKING

	Symbol	Q	N1:N2	N1:N3	Toko Part Number
Antenna	T_1		1:1.6		7HN-60064CY
RF	T_2, T_3	120		10:1	RWOS-6A7894AO, L = 178 µH
Local Osc.	T_4	120		5:1	7TRS-A5609AO
Mixer	T_5		2:1	8.9:1	7LC-502112N4, C_T = 180 pF
Detector	L_2	100			A7BRS-T1041Z, C_T = 1000 pF

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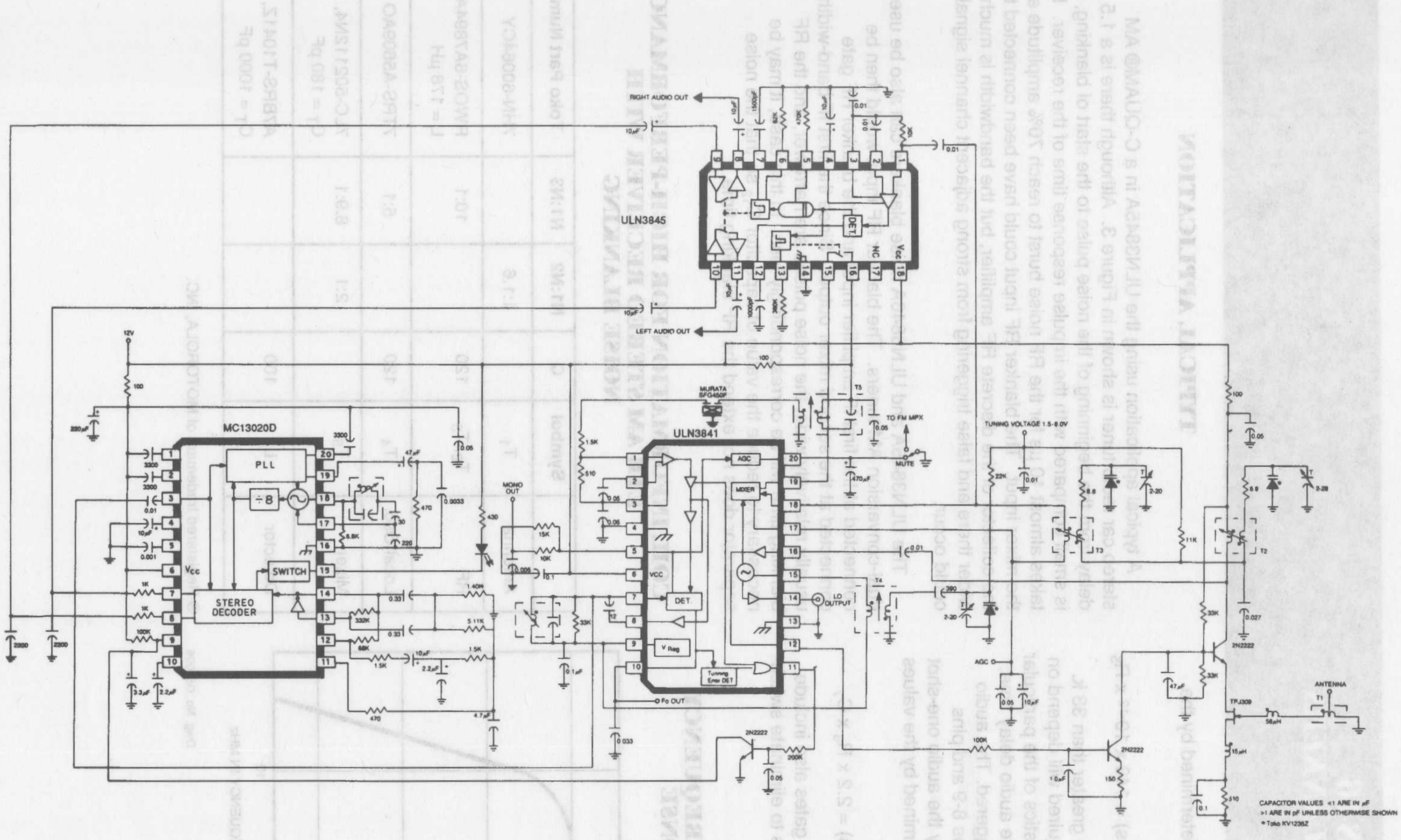
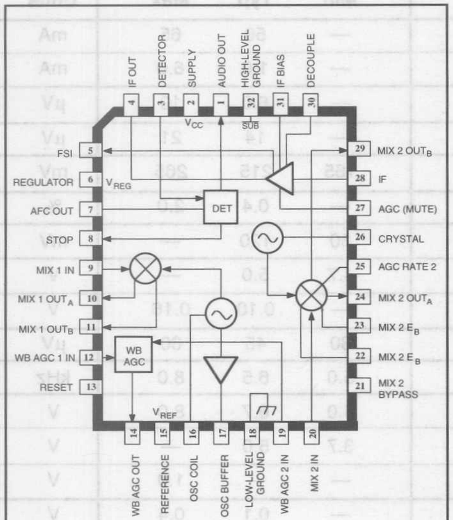
ETR AM STEREO RECEIVER WITH NOISE BLANKING



3848

27121.15

DUAL-CONVERSION AM RECEIVER



Dwg. No. PS-012-1

Providing the AM signal processing functions for an electronically tuned AM receiver (ETR), the A3848EEQ includes two balanced mixers, a crystal local oscillator, an L/C-tuned local oscillator, oscillator buffer, IF amplifier, AM detector, scan control detectors, and a switchable voltage regulator. This dual-conversion device typically mixes the incoming RF up to a first IF of 10.7 MHz, then down to 450 kHz, and then detects the audio. The addition of a JFET matched to a whip antenna, RF low-pass filter, IF selectivity, and audio stages gives a complete AM radio which can be used in automotive receivers. The frequency-detecting stop circuit is also capable of recovering narrow-band FM, making it useful for scanners or weather band radio applications. Two AGC and field-strength indicator modes provide special features for scanning.

The A3848EEQ uses the dual criteria of frequency and amplitude for establishing a valid stop. Tuning accuracy (frequency criterion) is established by evaluating phase shift across the detector coil. The circuitry is similar to that used in FM discriminators. Because this detection system is phase operated, it remains effective even in the presence of strong signals, which can cause false stops in systems using narrow-band filters. The amplitude criterion for stop is determined by evaluating the IF level. It includes a unique circuit that removes the effect of the AGC action. This allows the AGC tuning components to be selected for low-frequency audio performance without compromising scanning speed.

In the normal AGC mode (AGC RESET low), a slow, narrow-band field-strength indicator (FSI) is provided for controlling signal-dependent functions such as stereo blending. A fast AGC mode (AGC RESET high) resets the AGC holding capacitors to maximum gain. This mode allows cataloging station strengths quickly during a band sweep.

This AM signal processor is packaged in a rectangular, 32-lead, plastic, leaded chip carrier (PLCC) for surface-mount applications and is rated for operation over the temperature range of -40°C to +105°C are available on special order.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . **12 V**
Package Power Dissipation, P_D . . . . **1.2 W**
Operating Temperature Range,
T_A . . . . **-40°C to +105°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**

FEATURES

- Low Noise Figure
- Balanced Mixers
- High Dynamic Range First Mixe
- Field-Strength Indicator
- Buffered Oscillator
- Fast Scan Mode

Always order by complete part number: **A3848EEQ**

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 10 V, f_o = 1 MHz, f_{if1} = 10.7 MHz, f_{if2} = 450 kHz, V_{in} = 10 mV; f_m = 1 kHz , Mod = 30% (except as noted).

Characteristic	Symbol	Test Conditions	Limits Min	Limits Typ	Limits Max	Units
Supply Current	I_{CC}	I_2, V_{in} = 0	—	50	65	mA
		I_2, V_{in} = 0, V_{27} = 0 (Muted)	—	1.0	6.0	mA
Sensitivity	V_{in}	V_{out} = 50 mV	—	6.0	10	µV
Usable Sensitivity	V_{in}	S + N/N = 20 dB	—	14	21	µV
Recovered Audio	V_{out}		165	215	265	mV
Total Harmonic Dist.	THD	Mod = 90%	—	0.4	2.0	%
Oscillator Output	V_o	V_{17}	80	120	—	mV
Stop Output Voltage	V_{STP}	V_8, V_{in} = 0	4.7	5.0	—	V
		V_8, Mod = 0%	—	0.10	0.16	V
Stop Sensitivity	V_{stp}	V_{12} = 2.5 V, Mod = 0%	30	45	60	µV
Stop Bandwidth	BW_{STP}	V_8 = 2.5 V, = 0%	5.0	6.5	8.0	kHz
Wide-Band AGC	V_{AGC}	V_{in} = 0	5.0	6.7	8.0	V
		V_{in} = 11 mV, Mod = 0%	3.7	5.0	—	V
		V_{in} = 26 mV, Mod = 0%	—	—	1.0	V
Field-Strength Indicator Output Voltage (unmodulated, AGC Reset Low)	V_{FSI}	V_{in} = 0	—	0.1	0.4	V
		V_{in} = 30 µV, Mod = 0%	0.25	0.60	1.05	V
		V_{in} = 100 µV, Mod = 0%	1.1	1.6	2.2	V
		V_{in} = 1 mV, Mod = 0%	1.8	2.5	3.2	V
		V_{in} = 10 mV, Mod = 0%	3.1	3.7	4.4	V
Field-Strength Indicator Output Voltage (unmodulated, AGC Reset High)	V_{FSI}	V_{in} = 0	—	—	0.5	V
		V_{in} = 30 µV, Mod = 0%	0.9	1.1	1.5	V
		V_{in} = 100 µV, Mod 0%	1.3	1.6	2.0	V
		V_{in} = 1 mV, Mod = 0%	2.3	2.9	3.5	V
		V_{in} = 10 mV, Mod = 0%	2.5	3.7	4.0	V
Overload	V_{in}	V_{out} = 3% THD, Mod = 90%	60	100	—	mV
		First Mixer (Note 2)	350	450	—	mV
-3dB Limiting	V_{in}	Mod = 3 kHz peak deviation	—	12	—	µV
IF Output Voltage	V_{out}	V_{in} = 1 mV	200	250	320	mV
FM Recovered Audio	V_{out}	V_7, Mod = 3 kHz peak deviation	—	380	—	mV
Signal to Noise Ratio	S+N/N	V_{in} = 1 mV	50	53	—	dB
		V_{in} = 10 mV	53	56	—	dB
AGC Figure of Merit	FOM	Ref. at V_{in} = 10 mV, V_{in} for V_{out} = -10 dB	7.0	10	14	µV

Continued next page...

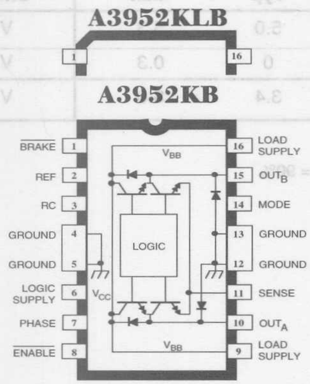
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 10 V, f_o = 1 MHz, f_{if1} = 10.7 MHz, f_{if2} = 450 kHz, V_{in} = 10mV; f_m = 1 kHz, Mod = 30% (except as noted) (continued)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min	Typ	Max	
Regulator Voltage	V_{REG}	V_6	4.7	5.0	5.3	V
		V_6, V_{27} = 0 (Muted)	—	0	0.3	V
Reference Voltage	V_{REF}	V_{15}	3.2	3.4	3.6	V

NOTES: 1. Typical data is for design information only.
2. Attenuate MIXER 1 output with 50 Ω load on mixer coil secondary, V_{out} =3% THD, Mod = 90%

3952

FULL-BRIDGE PWM MOTOR DRIVER



Dwg. PP-056

Note that the A3952KB (DIP) and the A3952KLB (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} .... **50 V**
Output Current, I_{OUT}
($t_w \leq 20$ µs) .... **±3.5 A**
(Continuous) .... **±2.0 A**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range,
V_{IN} .... **-0.3 V to V_{CC} + 0.3 V**
Sense Voltage, V_{SENSE} .... **1.5 V**
Reference Voltage, V_{REF} .... **15 V**
Operating Temperature Range,
T_A .... **–40°C to +125°C**
Junction Temperature, T_J .... **+150°C***
Storage Temperature Range,
T_S .... **–55°C to + 150°C**

Output current rating may be limited by duty cycle, ambient temperature, heat sinking and/or forced cooling. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed for bidirectional pulse-modulated current control of inductive loads in extended temperature automotive/industrial applications, the A3952K— is capable of continuous output currents to ±2 A and operating voltages to 50 V over a temperature range of -40°C to +125°C. Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed OFF-time pulse duration is set by a user-selected external RC timing network. Internal circuit protection includes thermal shutdown with hysteresis, transient suppression diodes, and crossover-current protection. Special power-up sequencing is not required.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type A3952S— are shown in Section 3. Complete, detailed technical information on the A3952K— is available on request. The devices are also available for operation between -40°C and +85°C. To order, change the part number suffix from K— to E—.

The A3952K— is supplied in a choice of four power packages. In all package styles, the batwing/power tab is at ground potential and needs no isolation.

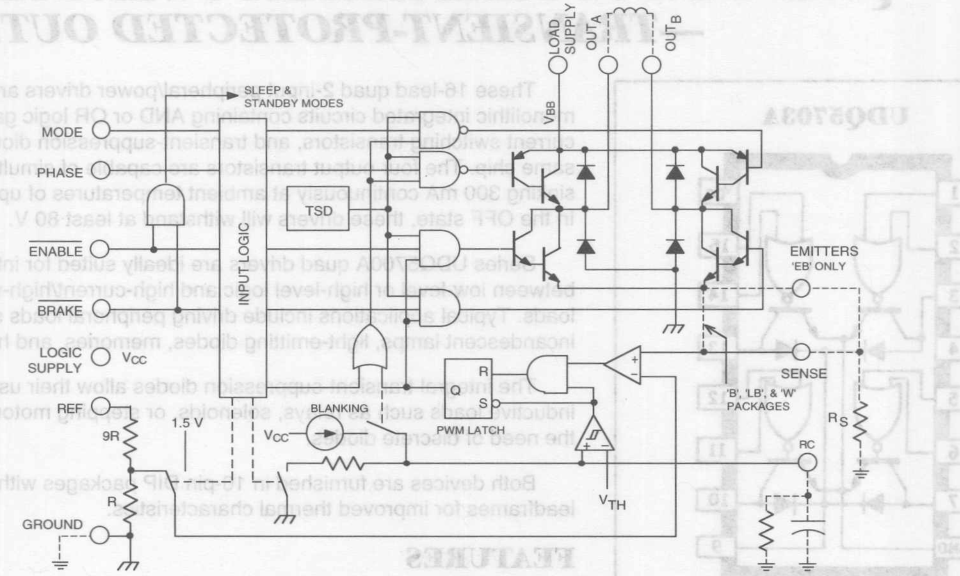
FEATURES

- ±2 A Continuous Output Current Rating
- 50 V Output Voltage Rating
- Internal PWM Current Control
- Fast and Slow Current-Decay Modes
- Sleep (Low Current Consumption) Mode
- Internal Transient Suppression Diodes
- Under-Voltage Lockout
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protection

Always order by complete part number:

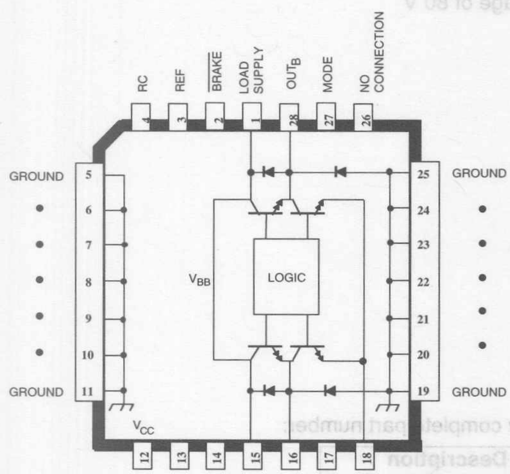
Part Number	Package	$R_{\theta JA}$	$R_{\theta JT}$
A3952KB	16-Pin DIP	43°C/W	6.0°C/W
A3952KEB	28-Lead PLCC	42°C/W	6.0°C/W
A3952KLB	16-Lead SOIC	67°C/W	6.0°C/W
A3952KW	12-Pin Power-Tab SIP	36°C/W	2.0°C/W

FUNCTIONAL BLOCK DIAGRAM



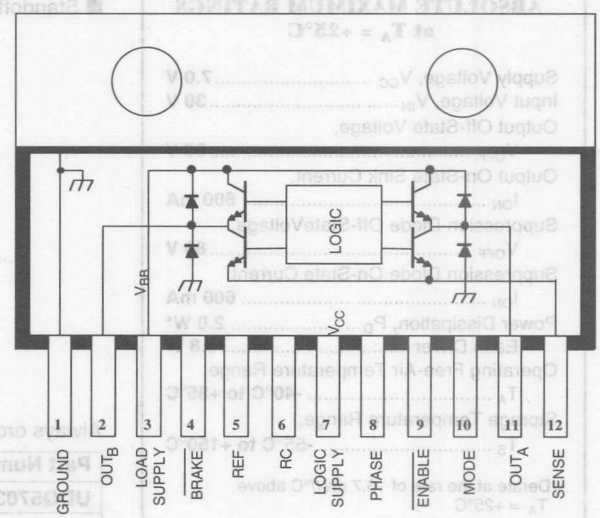
Dwg. FP-036

A3952KEB



Dwg. PP-057

A3952KW



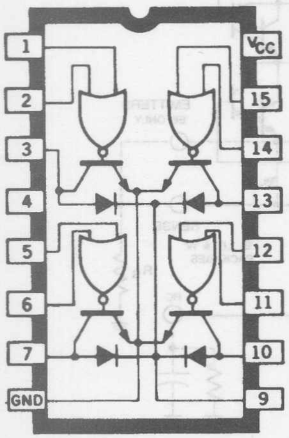
Dwg. PP-058

5703 AND 5706

29306.1B

QUAD 2-INPUT PERIPHERAL/POWER DRIVERS —TRANSIENT-PROTECTED OUTPUTS

UDQ5703A



Dwg. No. A-9869

These 16-lead quad 2-input peripheral/power drivers are bipolar monolithic integrated circuits containing AND or OR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Series UDQ5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need of discrete diodes.

Both devices are furnished in 16-pin DIP packages with copper leadframes for improved thermal characteristics.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} .... **7.0 V**
Input Voltage, V_{IN} .... **30 V**
Output Off-State Voltage,
V_{OFF} .... **80 V**
Output On-State Sink Current,
I_{ON} .... **600 mA**
Suppression Diode Off-StateVoltage,
V_{OFF} .... **80 V**
Suppression Diode On-State Current,
I_{ON} .... **600 mA**
Power Dissipation, P_D .... **2.0 W***
Each Driver .... **0.8 W**
Operating Free-Air Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

FEATURES

- Two Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Always order by complete part number:

Part Number	Description
UDQ5703A	Quad OR Driver
UDQ5706A	Quad AND Driver

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4. 75	5.0	5.25	V
Operating Temperature Range	-40	+25	+85	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	—	MIN	—	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	—	MIN	—	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	—	MAX	0.4 V	30 V	—	—	-50	-100	µA	2
"1" Input Current	$I_{IN(1)}$	—	MAX	30 V	0 V	—	—	—	10	µA	2
Input Clamp Voltage	V_{LK}	—	MIN	-12 mA	—	—	—	—	-1.5	V	—

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	200	—	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts), C_L = 15 pF	—	300	—	ns	3

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

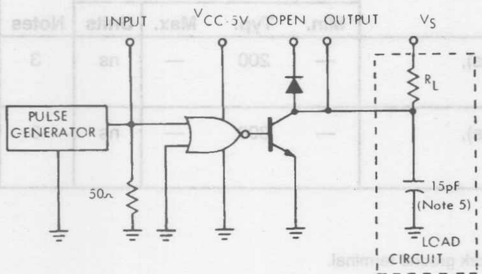
INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	t_f = 7 ns	t_p = 1µs
$V_{IN(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

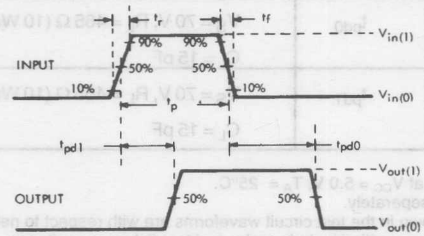
UDQ5703A QUAD OR DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{OFF}		MIN	2.0 V	0 V	80 V			100	µA	
		—	OPEN	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	0.8V	150 mA	—	0.35	0.5	V	—
		—	MIN	0.8 V	0.8V	300 mA	—	0.5	0.7	V	—
Diode Leakage Current	I_R	NOM	NOM	0 V	0 V	OPEN	—	—	200	µA	3
Diode Forward Voltage Drop	V_F	NOM	NOM	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	72	100	mA	1, 2

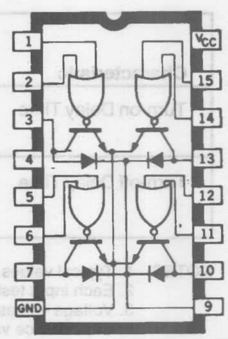
NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package
3. Diode leakage current measured at $V_R = V_{off\,(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-9123A



Dwg. No. A-7628C

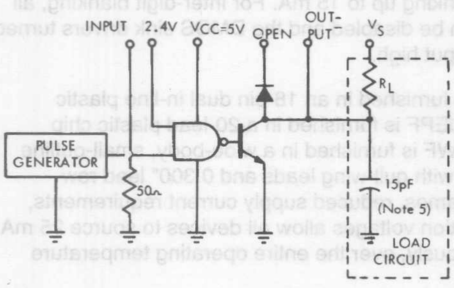


Dwg. No. A-9869

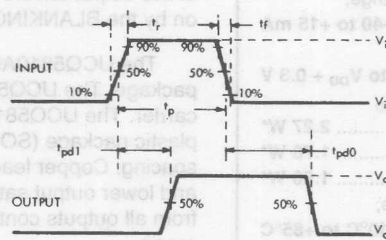
UDQ5706A QUAD AND DRIVER
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted).

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{OFF}	—	MIN	2.0 V	2.0 V	80 V	—	—	100	µA	—
			OPEN	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	MIN	0.8 V	V_{CC}	150 mA	—	0.35	0.5	V	—
		—	MIN	0.8 V	V_{CC}	300 mA	—	0.5	0.7	V	—
Diode Leakage Current	I_R	NOM	NOM	0 V	0 V	OPEN	—	—	200	µA	3
Diode Forward Voltage Drop	V_F	NOM	NOM	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V	—	—	16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V	—	—	70	98	mA	1, 2

NOTES: 1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package
3. Diode leakage current measured at $V_R = V_{off\ (min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.



Dwg. No. A-7878A



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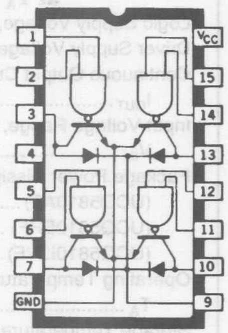


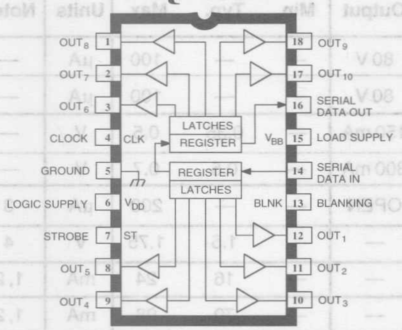
Dwg. No. A-9866

5810-F

26182.25

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCQ5810AF



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current Range,
I_{OUT} .... **-40 to +15 mA**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCQ5810AF) .... **2.27 W***
(UCQ5810EPF) .... **1.78 W***
(UCQ5810LWF) .... **1.56 W***
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

*Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCQ5810AF (dual in-line package) and UCQ5810LWF (small-outline IC package) are electrically identical and share a common pin number assignment.

The UCQ5810AF, UCQ5810EPF, and UCQ5810LWF combine a 10-bit CMOS shift register and accompanying data latches, control circuitry, bipolar sourcing outputs with DMOS active pull-downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and -40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The UCQ5810AF/EPF/LWF feature reduced supply requirements (active DMOS pull-downs) and lower saturation voltages when compared with the original UCQ5810A.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, serial-data input rates are typically over 5 MHz, with significantly higher speeds obtainable at 12 V. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCQ5811A (12 bits), UCQ5812AF/EPF (20 bits) and UCQ5818AF/EPF (32 bits).

The UCQ5810AF/EPF/LWF output source drivers are NPN Darlingtons capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA. For inter-digit blanking, all of the output drivers can be disabled and the DMOS sink drivers turned on by the BLANKING input high.

The UCQ5810AF is furnished in an 18-pin dual in-line plastic package. The UCQ5810EPF is furnished in a 20-lead plastic chip carrier. The UCQ5810LWF is furnished in a wide-body, small-outline plastic package (SOIC) with gull-wing leads and 0.300" lead row spacing. Copper lead frames, reduced supply current requirements, and lower output saturation voltages allow all devices to source 25 mA from all outputs continuously, over the entire operating temperature range.

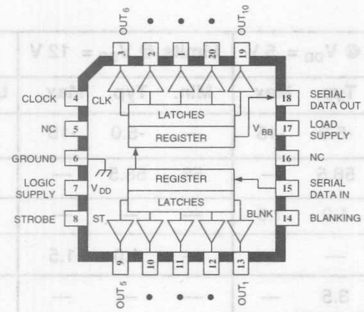
FEATURES

- High-Speed Source Drivers
- 60 V Minimum Output Breakdown
- Improved Replacements for TL4810B
- Low Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- To 3.3 MHz Data Input Rate
- Active DMOS Pull-Downs

Always order by complete part number, e.g., **UCQ5810AF**.

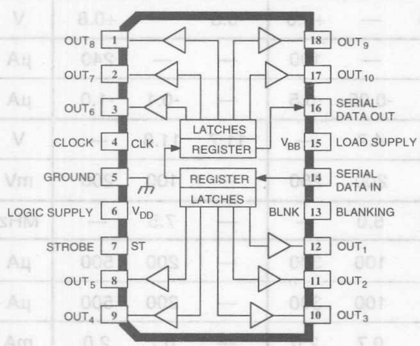
5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCQ5810EP

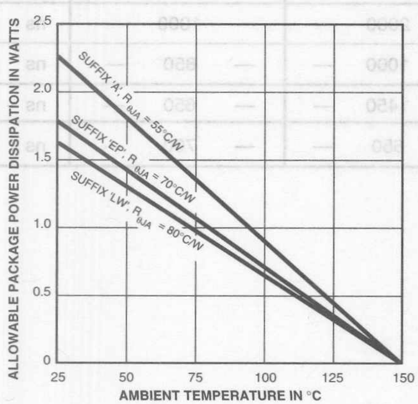


Dwg. No. PP-059

UCQ5810LWF

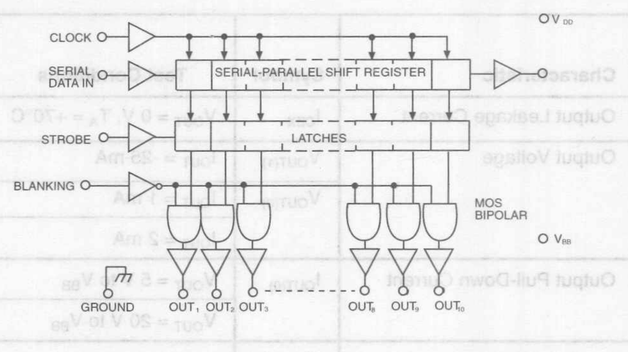


Dwg. PP-029-1

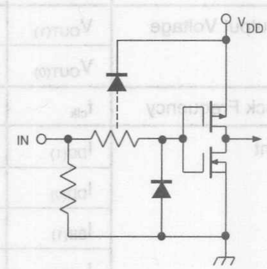


Dwg. GP-024A

FUNCTIONAL BLOCK DIAGRAM

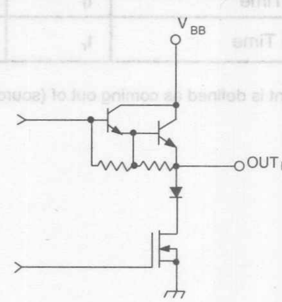


TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A

TYPICAL OUTPUT DRIVER



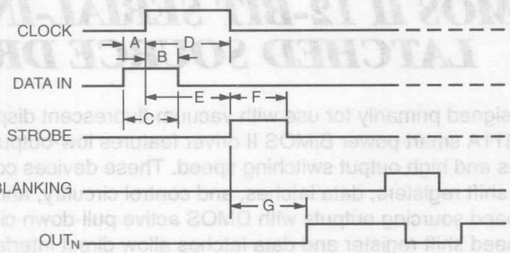
Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS over operating temperature range, V_{BB} = 60 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	—	100	—	—	240	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	0.7	2.0	—	0.7	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.

5810-F
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



Dwg. A-12,649A

TIMING CONDITIONS
(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) **75ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) **75ns**
C. Minimum Data Pulse Width **150ns**
D. Minimum Clock Pulse Width **150ns**
E. Minimum Time Between Clock Activation and Strobe **300ns**
F. Minimum Strobe Pulse Width **100ns**
G. Typical Time Between Strobe Activation and Output Transition **500ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5811

BiMOS II 12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

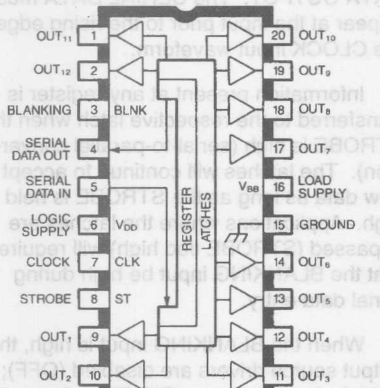
Designed primarily for use with vacuum-fluorescent displays, the UCQ5811A smart power BiMOS II driver features low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCQ5811A features 60 V and -40 mA output ratings, allowing it to be used in many other peripheral power driver applications. It can be used as an improved replacement tor the SN75512B. The Allegro devices do not require special power-up sequencing.

The UCQ5811A has been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, it will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of this device with TTL may require the use of appropriate pull-up resistors to ensure a proper input logic high.

Representative electrical characteristics (at an ambient temperature of +25°C) for the commercial type UCN5811A are shown in Section 3. Complete, detailed technical information on the UCQ5811A is available on request.

This device is supplied in a 20-pin plastic dual in-line package. It can be operated over the ambient temperature range of -40°C to + 85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 76°C .



Dwg. W-180

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current,
I_{OUT} .... **-40 to +25 mA**
Input Voltage Range,
V_{IN} .... **0.3 V to V_{DD} +0.3 V**
Package Power Dissipation,
P_D .... **See Graph**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

FEATURES

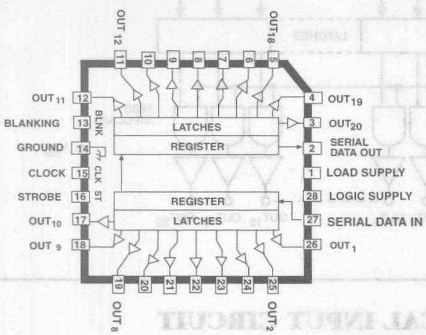
- To 3.3 MHz Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

Always order by complete part number: **UCQ5811A** .

5812-F

BiMOS II 20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCQ5812EPF



Dwg. No. A-14,356

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current Range,
I_{OUT} .... **-40 to +15 mA**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCQ5812AF) .... **3.12 W***
(UCQ5812EPF) .... **1.92 W=**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Derate at rate of 25 mW/°C above T_A = +25°C

= Derate at rate of 15 mW/°C above T_A = +25°C

Caution: Allegro CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCQ5812AF (dual in-line package) and UCQ5812EPF (PLCC package) are electrically identical and share a common pin number assignment.

The UCQ5812AF/EPF combine a 20-bit CMOS shift register, data latches, and control circuitry with high-voltage bipolar source drivers and active DMOS pull-downs for reduced supply current requirements. Although designed primarily for vacuum-fluorescent displays, the high-voltage, high-current outputs also allow them to be used in other peripheral power driver applications.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Data input rates are typically over 5 MHz with a 5 V logic supply, and over 7.5 MHz at 12 V. Especially useful for inter-digit blanking, the BLANKING input disables the output source drives and turns on the DMOS sink drivers. Use with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Similar devices are available as the UCQ5810AF/LWF (10 bits), UCQ5811A (12 bits), and UCQ5818AF/EPF (32 bits).

The output source drivers are high-voltage PNP-NPN Darlingtons with a minimum breakdown of 60 V and are capable of sourcing up to 40 mA. The DMOS active pull-downs are capable of sinking up to 15 mA.

The UCQ5812AF is supplied in a 28-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. For surface-mounting, the UCQ5812EPF is furnished in 28-lead plastic chip carrier (quad pack) with 0.050"(1.22 mm) centers. Copper lead-frames, reduced supply current requirements and lower output saturation voltages, allow continuous operation, with all outputs sourcing 25 mA, of the UCQ5812AF over the operating temperature range, and the UCQ5812EPF up to +75°C.

FEATURES

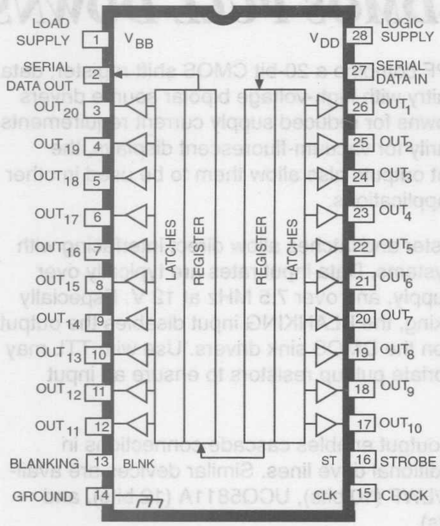
- High-Speed Source Drivers
- 60 V Source Outputs
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- Active DMOS Pull-Downs
- Reduced Supply Current Requirements
- Improved Replacement for TL5812

Always order by complete part number, e.g., UCQ5812AF.

5812-F

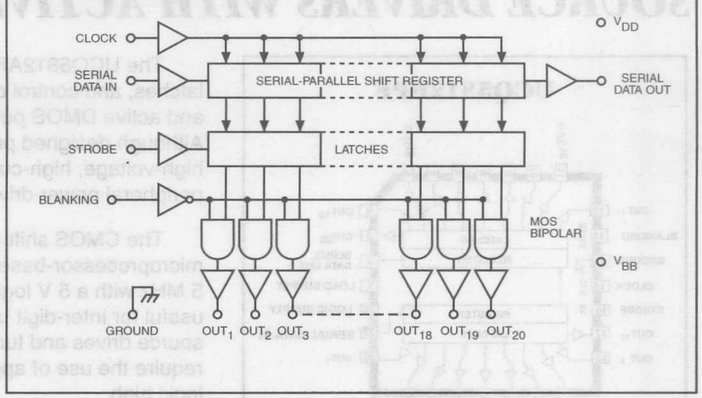
20-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCQ5812AF

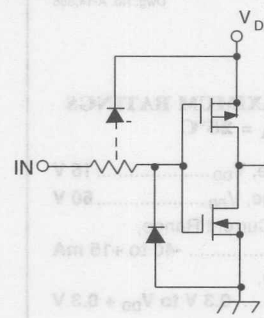


Dwg. No. A-12,270

FUNCTIONAL BLOCK DIAGRAM

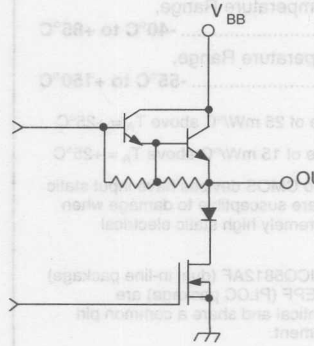


TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER

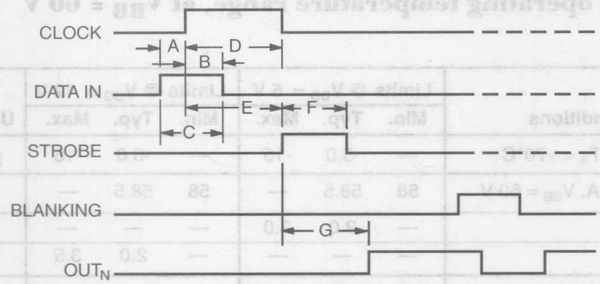


Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS over operating temperature range, at V_{BB} = 60 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA, V_{BB} = 60 V	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	4.0	—	1.5	4.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.



Dwg. No. 12,649A

Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**

C. Minimum Data Pulse Width .... **150 ns**

D. Minimum Clock Pulse Width .... **150 ns**

E. Minimum Time Between Clock Activation and Strobe .... **300 ns**

F. Minimum Strobe Pulse Width .... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Blanking	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	↑	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	↑	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	↓	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N1}	P_N
										X	X	X	...	X	X	H	L	L	L	...	L	L

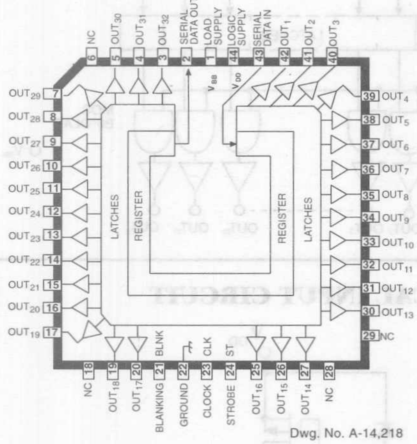
L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

5818-F

26182.29

BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS

UCQ5818EPF



Dwg. No. A-14,218

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **15 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current,
I_{OUT} .... **-40 to +15 mA**
Input Voltage Range,
V_{IN} .... **-30 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D
(UCQ5818AF) .... **3.5 W***
(UCQ5818EPF) .... **2.5 W†**
Operating Temperature Range,
T_A .... **-40°C to +85°C**
Storage Temperature Range,
T_S .... **-55°C to +150°C**

* Derate at rate of 28 mW/°C above T_A = +25°C
† Derate at rate of 20 mW/°C above T_A = +25°C

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with vacuum-fluorescent displays, the UCQ5818AF and UCQ5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interfacing with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and -40 mA output ratings, allowing them to be used in many other peripheral power driver applications.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of -40°C to +85°C. The UCQ5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirement, and low output saturation voltage permits operation with minimum junction temperature rise. The 'A' package allows all 32 outputs to be operated at -25 mA continuously over the operating temperature range.

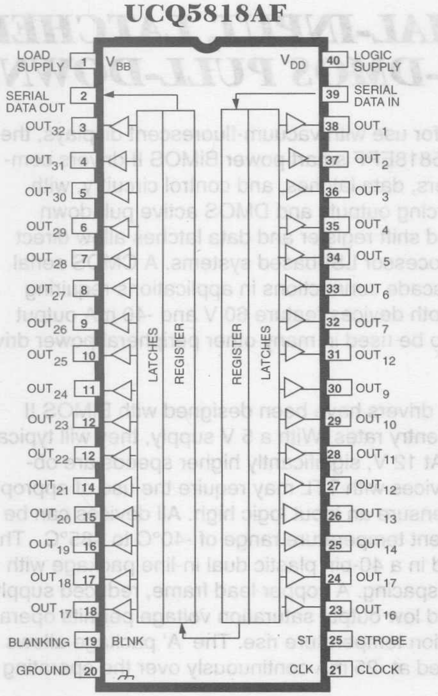
For high-density packaging applications, the UCQ5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface mounting on solder lands with 0.050" (1.27 mm) centers. The PLCC allows -25 mA continuous operation of all outputs simultaneously at ambient temperatures to 60°C. Similar devices are available as the UCQ5810AF/LWF (10 bits), UCQ5811A (12 bits), and UCQ5812AF/EPF (20 bits).

FEATURES

- 60 V Source Outputs
- High-Speed Source Drivers
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Active DMOS Pull-Downs
- Low-Power CMOS Logic and Latches
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

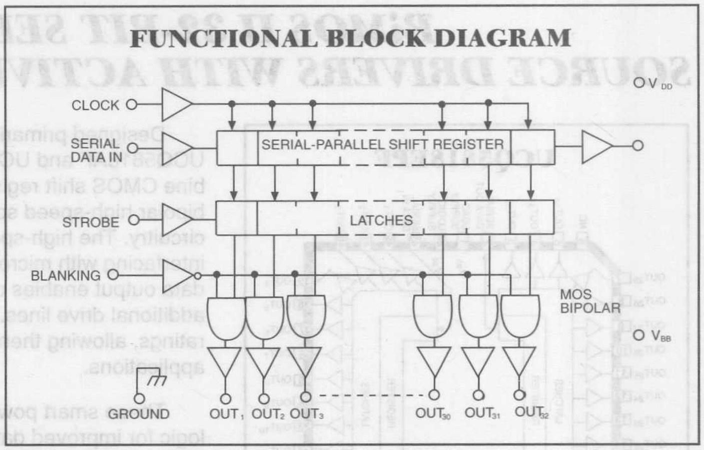
Always order by complete part number, e.g., **UCQ5818EPF**

UCQ5818AF

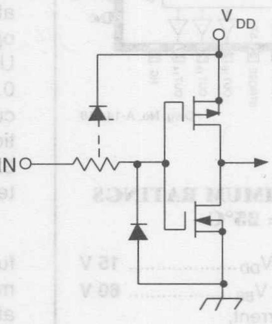


Dwg. No. A-12,269A

FUNCTIONAL BLOCK DIAGRAM

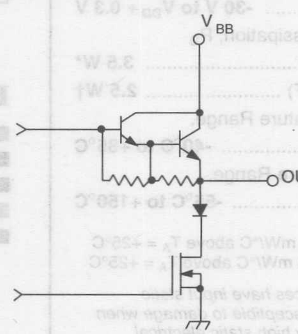


TYPICAL INPUT CIRCUIT

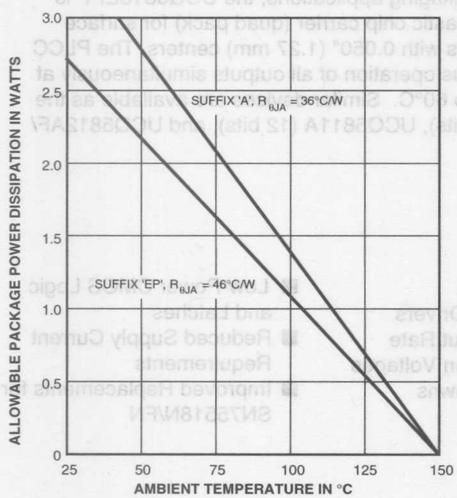


Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

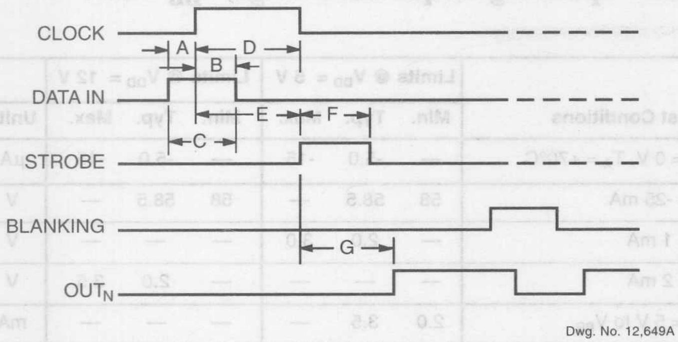


Dwg. GP-025A

ELECTRICAL CHARACTERISTICS over operating temperature range, V_{BB} = 60 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V Min.	Typ.	Max.	Limits @ V_{DD} = 12 V Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	-5.0	-15	—	-5.0	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	58	58.5	—	58	58.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2 mA	—	—	—	—	2.0	3.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.0	3.5	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		-0.3	—	+0.8	-0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-0.05	-0.5	—	-0.1	-1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	300	—	200	500	µA
	$I_{DD(0)}$	All Outputs Low	—	100	300	—	200	500	µA
	$I_{BB(1)}$	Outputs High, No Load	—	3.0	6.0	—	3.0	6.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF, 50% to 50%	—	2000	—	—	1000	—	ns
	t_{PLH}	C_L = 30 pF, 50% to 50%	—	1000	—	—	850	—	ns
Output Fall Time	t_f	C_L = 30 pF, 90% to 10%	—	1450	—	—	650	—	ns
Output Rise Time	t_r	C_L = 30 pF, 10% to 90%	—	650	—	—	700	—	ns

Negative current is defined as coming out of (sourcing) the specified device pin.



Serial Data present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

V_{DD} = 5.0 V

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) .... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) .... **75 ns**
C. Minimum Data Pulse Width .... **150 ns**
D. Minimum Clock Pulse Width .... **150 ns**
E. Minimum Time Between Clock Activation and Strobe .... **300 ns**
F. Minimum Strobe Pulse Width .... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition .... **500 ns**

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	↑	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	↑	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	↓	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

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TECHNICAL DATA & APPLICATION NOTES FOR PERIPHERAL POWER DRIVER ICs 3

TECHNICAL DATA & APPLICATION NOTES FOR HALL-EFFECT SENSOR ICs 4

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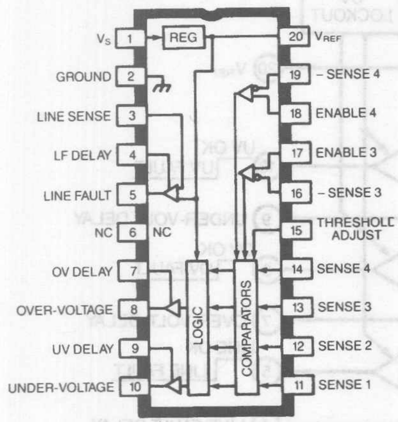
SECTION 6. TECHNICAL DATA FOR POWER CONVERSION / POWER MANAGEMENT ICs

8131

27467.2*

PRECISION SUPERVISORY SYSTEMS MONITOR

ULN8131A



Dwg. No. W-185

Capable of monitoring four dc power lines, the ULN8131A and ULN8131LW are power-fault monitors for both under-voltage and over-voltage conditions. Two of the four inputs are designed to monitor positive voltages, while the other two inputs can be used to monitor positive or negative voltages. Typical examples might be a +5 V logic supply, +15 V and -15 V analog supplies, and a positive peripheral power load supply. The primary power line is monitored by an additional comparator and will provide early warning of line voltage drop-out.

During low-supply voltage operations, an under-voltage lockout, which monitors the ULN8131A/LW internal supply, prevents false outputs from occurring. The logic outputs can be used to operate LEDs or other low-voltage indicators.

The circuit configuration of the ULN8131A/LW allows easy programming of over-voltage thresholds which are referenced to a 1% trimmed 2.5 V bandgap reference. The UV FAULT (pin 10) is initiated by one or more of the four sense inputs falling below the UV trip point (the internal reference voltage). The OV FAULT (pin 8) is activated by one or more of the sense inputs rising above the externally set (pin 15) OV trip point. The LINE OK output (pin 5) will remain high as long as the LINE SENSE input (pin 3) is above the internal voltage. The LINE SENSE will accept a positive dc voltage proportional to either the high-voltage master bus or the ac line.

continued next page...

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . **35 V**
Power Dissipation, P_D . . . . **1.1 W**
Operating Temperature Range,
T_A . . . . **0°C to +70°C**
Storage Temperature Range,
T_S . . . . **-65°C to +150°C**
Junction Temperature, T_J . . . . **+150°C**

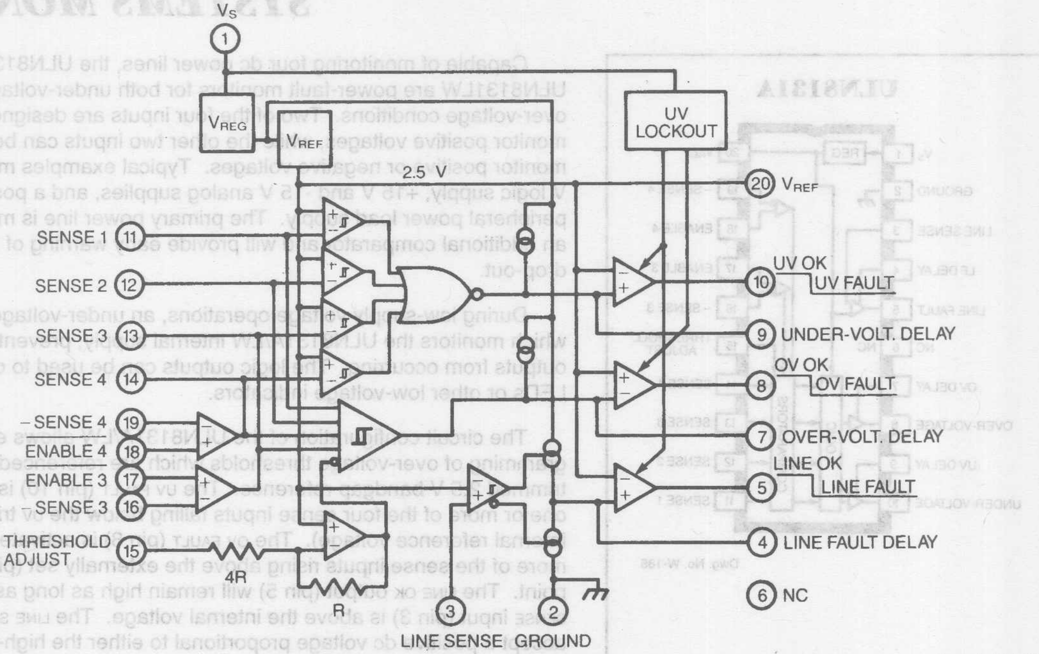
FEATURES

- Monitors Four DC Supplies
- V_S Under-Voltage Lockout
- Fixed Under-Voltage Threshold
- Low Standby Current
- Line Sense Input
- Programmable Over-Voltage Threshold
- Pull-Up Clamped Outputs
- Programmable Output Delays
- 10 to 35 Volts Operation
- Reference Trimmed to 1%
- Separate Under-Voltage Comparators

Always order by complete part number:

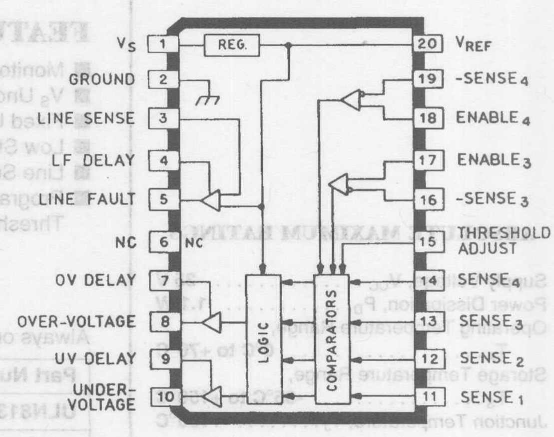
Part Number	Package
ULN8131A	**20-Pin DIP**
ULN8131LW	**20-Lead SOIC**

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. W-186

ULN8131LW



Dwg. No. A-14,372

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 15$ V

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Max.	Units
Functional V_S Range	1		10	35	V
Quiescent Current	1	$V_S = 35$ V, $V_{17} = V_{18} = V_{20}$ No Fault	—	15	mA
REFERENCE VOLTAGE SECTION					
Reference Voltage	20	No Load, $T_A = +25°C$	2.47	2.53	V
		No Load, Change Over Temp.	—	25	mV
Load Regulation	20	$I_{REF} = 0$ to 10 mA	—	20	mV
Line Regulation	20	$V_S = 10$ to 35 V	—	10	mV
Ripple Rejection	20	f = 120 Hz	60		dB
Short-Circuit Current Protection	20		—	40	mA
COMPARATOR SECTION					
Under-Voltage Trip Points	11-14*	$T_A = +25°C$	2.47	2.53	V
		Over Temperature	2.46	2.54	V
Under-Voltage Trip Hysteresis	11-14*	Over Temperature	10	25	mV
Over-Voltage Trip Points	11-14*	$V_{15} = 0$	3.08	3.17	V
Over-Voltage Trip Hysteresis	15	$V_{15} = 0$ to 2.5 V, Over Temp.	10	25	mV
Line Monitor Trip Threshold	3		2.40	2.54	V
Under-Voltage Lockout Enable	1	V_S Decreasing	8.5		V
Under-Voltage Lockout Disable	1	V_S Increasing	—	10.5	V
Input Bias Current	3, 11, 12	$V_{IN} = 2.0$ V	—	-6.0	µA
		$V_{IN} = 3.0$ V	—	6.0	µA
	15	$V_{IN} = 0$	—	-50	µA
	16, 19	$V_{IN} = -2.0$ V, $V_{17} = V_{18} = 0$ V	—	-2.0	µA
OUTPUT DRIVERS					
Output Saturation Voltage	5, 10	$I_{SINK} = 5.0$ mA	—	0.5	V
	8	$I_{SINK} = 10$ mA	—	0.5	V
	5, 8, 10	$I_{SOURCE} = 500$ µA	4.0	5.25	V
Output Leakage current	5, 8, 10	$V_{OUT} = 35$ V	—	50	µA
Line Fault Delay Current Source	4	$V_4 = 2.0$ V	160	350	µA
Line Fault Delay Current Sink	4	$V_4 = 2.0$ V	3.2	7.0	mA
Over-Voltage Delay Current Source	7	$V_7 = 2.0$ V	160	300	µA
Under-Voltage Delay Current Source	9	$V_9 = 2.0$ V	35	75	µA

*All inputs connected to 2.75 V except input being tested.

APPLICATIONS

The basic voltage monitors are based on a 2.5 V precision bandgap reference. External resistive dividers are used to present a nominal 2.5 V level to each under-voltage comparator at the minimum allowable under-voltage condition. The over-voltage reference is set up by another resistive divider at pin 15 determined by the tightest over-voltage tolerance requirement.

BASIC FORMULAS:

1. An under-voltage fault is detected, (pin 10 goes low), when the positive input voltage being monitored is less than:

$$V_{MON(LO)} = 2.5\ (R_1 + R_2)/R_2$$

2. The internal over-voltage threshold is defined as:

$$V_{OVT} = 2.5 \left[1 + \frac{R_A}{4(R_A + R_B)} \right]$$

where $R_A // R_B << 100\ k\Omega$.

3. An over-voltage fault is detected when the positive input voltage being monitored exceeds:

$$V_{MON(HI)} = V_{OVT}\ (R_1 + R_2)/R_2$$

4. Individual over-voltage thresholds can be increased by the addition of R_X with

$$R_X = R_1 \left[\frac{V_{OVT} - 2.5}{V_{MON(HI)} - V_{OVT} \left(\frac{R_1 + R_2}{R_2} \right)} \right]$$

5. To monitor negative supplies at SENSE 3 or SENSE 4, pin 17 or 18, respectively, is connected to ground. In this condition, an under-voltage fault indication will occur when the negative supply being monitored falls below:

$$V_{MON(LO)} = 2.5\ R_3/R_4$$

Note that for monitor purposes, under-voltage means the negative supply is actually going net positive, or toward ground.

6. For negative supplies, an over-voltage fault indication will occur when:

$$V_{MON(HI)} = V_{OVT}\ R_3/R_4$$

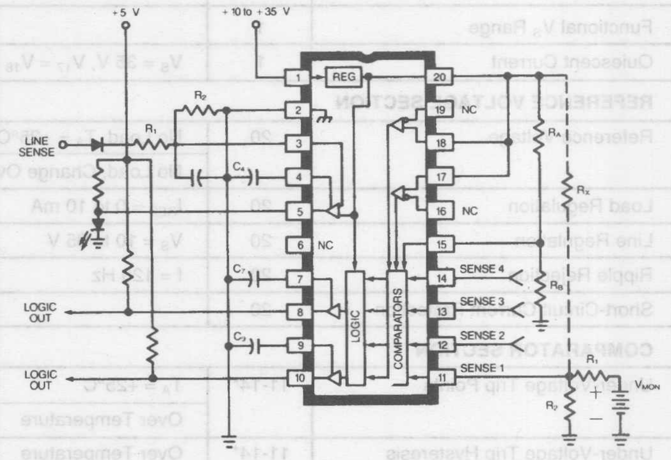
7. Fault delay capacitor values are determined by:

$$C_4 \text{ or } C_7 = \frac{200 \times 10^{-6} \times t}{2.5}$$

$$C_9 = \frac{55 \times 10^{-6} \times t}{2.5}$$

where t is the output delay in seconds.

LINE SENSE AND POSITIVE SUPPLY MONITORING (SENSE 1, 2, 3, and 4)



Dwg. No. W-157

UNUSED INPUTS

Unused positive sense channel inputs (pins 3, 11-14) must not be left unconnected. They cannot be tied high (over-voltage fault indication), tied low (under-voltage fault indication), or tied to the internal reference (susceptible to noise and voltage offsets). Unused sense channel inputs should be connected to any operating sense channel input. For example, if channels 1, 2, and 4 are being used, the unused channel 3 sense input (pin 13) should be connected to the SENSE 2 or SENSE 4 input.

Unused negative sense channel inputs (pins 16 and 19) can be left open-circuited *provided* the associated ENABLE inputs (pins 17 and 18) are tied high and the associated positive sense channel inputs (pins 13 and 14) are utilized to monitor positive supplies or are connected as described above.

DESIGN EXAMPLE

As an example, consider the following set of monitoring conditions:

V_1 = +5 V (+10%, -5%)

V_2 = +12 V (±10%)

V_3 = +15 V (±5%)

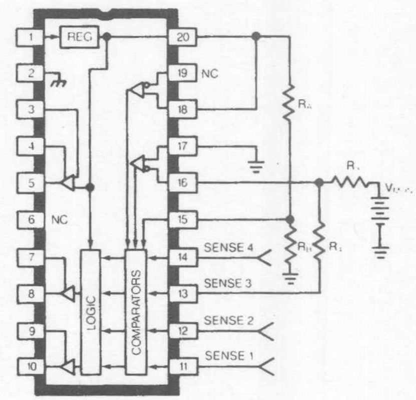
V_4 = +24 V (±10%)

The required input dividers are calculated per (1) to yield the resistor divider ratios, $R_2(R_1 + R_2)$, of: 0.5263, 0.2315, 0.1754 (Note 1), and 0.1157 respectively. The over-voltage threshold, V_{OVT}, would be dictated by the tightest tolerance supply which gives the lowest V_{OVT} from (3). Therefore, $V_{MON(HI)}$ = 15 x 1.05 = 15.75 V and V_{OVT} = 15.75 x 0.1754 = 2.763 V[1]. This is the voltage appearing at the SENSE terminal and is equal to the over-voltage threshold to be set via the resistor ratio at pin 15. From (2) $R_A/(R_A + R_B)$ is calculated to be 0.4096. It is good practice to keep the equivalent external impedances as low as possible, in order to minimize bias current and offset errors. For the purpose of this example, all resistor dividers will be taken to have an equivalent impedance of 1000 ohms. This being the case, the final values are:

R_A = 1.7 kΩ and R_B = 2.44 kΩ.

In order to provide accurate over-voltage sensing for the V_1, V_2, and V_4 supplies, resistors are connected from the respective input sense nodes and returned to the 2.5 V reference. Calculation is made by first picking values for the input dividers and then calculating the required value of R_X from (4). Again, assuming 1 kΩ equivalent divider

NEGATIVE SENSE MONITORING
SENSE 3 and 4 Only



Dwg. No. W-187

impedances and making the calculations, a summary of results is given below.

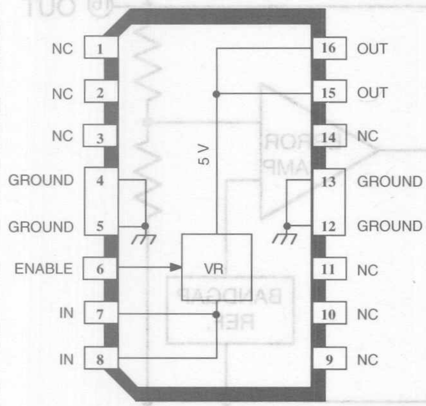
MONITORED SUPPLY	$V_{MON(HI)}$	$V_{MON(LO)}$	R_1	R_2	R_X
+5 V (+10%, -5%)	5.5 V	4.75 V	1.90 kΩ	2.11 kΩ	2.0 kΩ
+12 V (±10%)	13.2 V	10.8 V	4.32 kΩ	1.30 kΩ	900 Ω
+15 V (±5%)	15.75 V	14.25 V	5.70 kΩ	1.21 kΩ	∞
+24 V (±10%)	26.4 V	21.6 V	8.64 kΩ	1.13 kΩ	900 Ω

1. Note that the number 0.1754 is rounded off. Due to required accuracies in the external dividers, round off numbers only after final resistor values are calculated. For the same reason, use stable high-accuracy metal film resistors. Many applications may benefit from combining the ULN8131A and functionally trimmed resistor-capacitor networks.

8181

27468*

LOW-DROPOUT, 5 V REGULATOR — HIGH EFFICIENCY



Dwg. PS-018

Especially suited for hand-held, portable, battery-operated equipment such as cellular telephones, the A8181SLB low dropout voltage regulator provides high efficiency for maximum battery life in a minimum package size. Equally applicable to camcorders and portable computers, the device provides a fixed 5 V regulated continuous output at almost 200 mA of load current under worst-case conditions. Under normal operating conditions, output currents over 500 mA are permitted.

A MOSFET pass element delivers high output current with an input-output differential of less than 300 mV. For high efficiency, the low dropout voltage allows a longer battery discharge before output voltage regulation is lost. A low quiescent current, even during high load conditions, makes the device ideal for standby power systems. High regulator accuracy and excellent temperature characteristics are provided by a bandgap reference. An enable input gives the designer complete control over sequential power-up or emergency shutdown.

This device is supplied in a 16-lead wide-body, small-outline plastic power package (SOIC) for surface-mount applications. The copper batwing provides for maximum package power dissipation in the smallest possible construction. The A8181SLB is rated for operation over a temperature range of -20°C to +85°C.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Input Voltage, V_I .... **10 V**

Output Current, I_O

(40% duty cycle) .... **1 A***

(75% duty cycle) .... **500 mA***

(continuous) .... **370 mA***

Enable Input Voltage, V_E .... **V_I**

Operating Temperature Range,

T_A .... **-20°C to +85°C**

Junction Temperature, T_J .... **+150°C†**

Storage Temperature Range,

T_S .... **-40°C to +150°C**

* Output current rating is limited by input voltage, duty cycle, and ambient temperature. Under any set of conditions, do not exceed a junction temperature of +150°C. See next page.

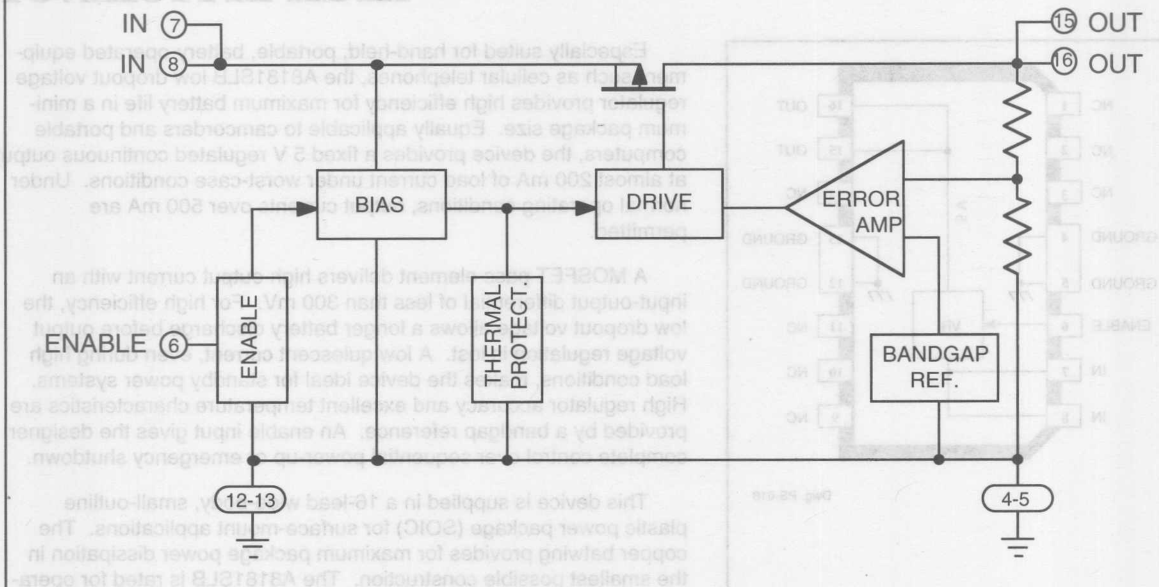
† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

FEATURES AND BENEFITS

- High Efficiency Provides Extended Battery Life
- Less Than 300 mV Dropout Voltage
- Low Quiescent Current
- >200 mA Output Current
- LSTTL-Compatible ON/OFF Control For Sequential Power-up or Emergency Shutdown
- Internal Thermal Protection
- SOIC Surface-Mount Package

Always order by complete part number: **A8181SLB** .

FUNCTIONAL BLOCK DIAGRAM



Dwg. FS-012

MAXIMUM ALLOWABLE OUTPUT CURRENT with device mounted on 2.24" x 2.24" (56.9 mm x 56.9 mm) solder-coated copper-clad board in still air.

	Maximum Allowable Output Current in Milliamperes with V_I = 10 V, T_J = 150°C* dc (Duty Cycle)								
T_A	100%	90%	80%	70%	60%	50%	40%	30%	20%
25°C	370	415	465	530	620	745	930	1000	1000
50°C	295	330	370	425	495	595	745	995	1000
70°C	235	265	295	340	395	475	595	795	1000
85°C	190	215	240	275	320	385	485	645	970

* $I_O = (T_J - T_A)/([V_I - V_O]\ R_{\theta JA} \bullet dc) = (150 - T_A)/(5 \bullet 67 \bullet dc)$

Output current rating can be increased (to 1 A maximum) by heat sinking or reducing the input voltage. With an infinite heat sink, $R_{\theta JA} = R_{\theta JT}$ = 6°C/W. Conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

ELECTRICAL CHARACTERISTICS at T_A +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Output Voltage	V_O	T_A = 25°C, 5.5 V ≤ V_I ≤ 10 V, 0 mA ≤ I_O ≤ 500 mA†	4.90	5.00	5.10	V
		T_A = 85°C, 5.5 V ≤ V_I ≤ 10 V, 0 mA ≤ I_O ≤ 500 mA*†	4.85	—	5.15	V
Output Volt. Temp. Coeff.	α_{VO}	I_O = 0	—	±100	—	µV/°C
Line Regulation	$\Delta V_{O(\Delta VI)}$	5.5 V ≤ V_I ≤ 10 V, Output open	—	10	30	mV
Load Regulation	$\Delta V_{O(\Delta IO)}$	0 mA ≤ I_O ≤ 500 mA†, V_I = 6 V	—	40	100	mV
Dropout Voltage	$V_I$min - V_O	I_O = 500 mA†	—	—	300	mV
Quiescent Current (GND terminal current)	I_Q	V_I = 10 V, I_O = 500 mA†	—	87	120	µA
		V_I = 10 V, Output open	—	86	120	µA
	$I_{Q(off)}$	V_I = 10 V, Output open, V_E = 0.4 V	—	—	20	µA
ENABLE Input Voltage	V_{EH}	Output ON, V_I = 10 V	2.4	—	—	V
	V_{EL}	Output OFF, V_I = 10 V	—	—	0.4	V
ENABLE Input Current	I_E	V_E = V_I = 10 V	—	—	±0.1	µA
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Resistance	$R_{\theta JA}$	Mounted on 2.24" x 2.24" solder-coated copper-clad board in still air	—	67	—	°C/W
	$R_{\theta JT}$		—	6.0	—	°C/W

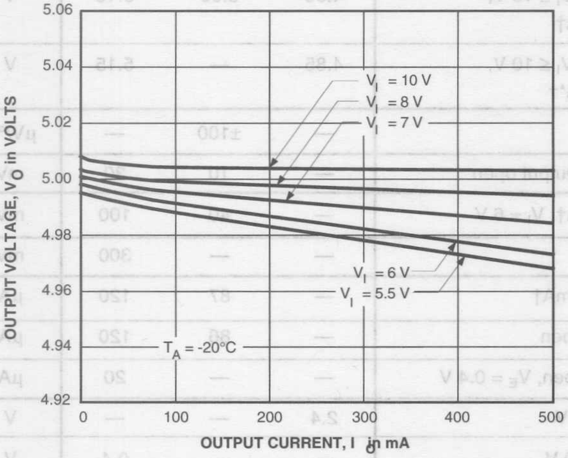
Typical values are given for circuit design information only.

* This parameter is tested to a lot sample plan only.

† Pulse test (<20 ms).

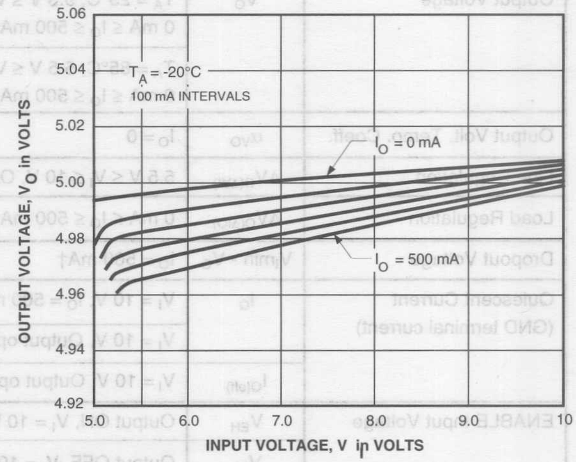
TYPICAL CHARACTERISTICS

LOAD REGULATION

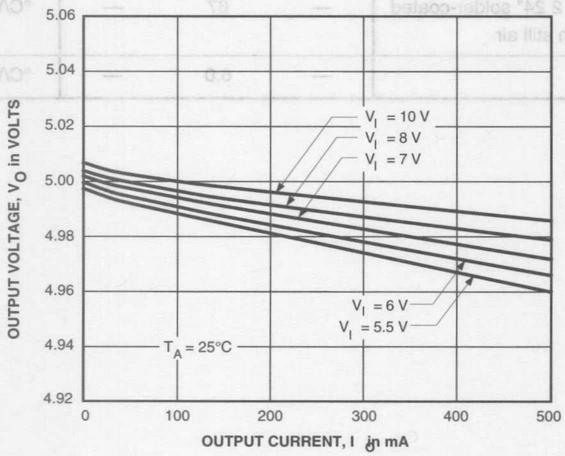


Dwg. GP-039

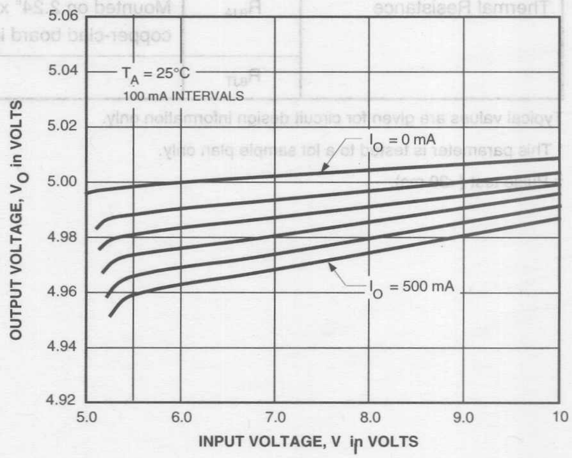
LINE REGULATION



Dwg. GP-040



Dwg. GP-039-1

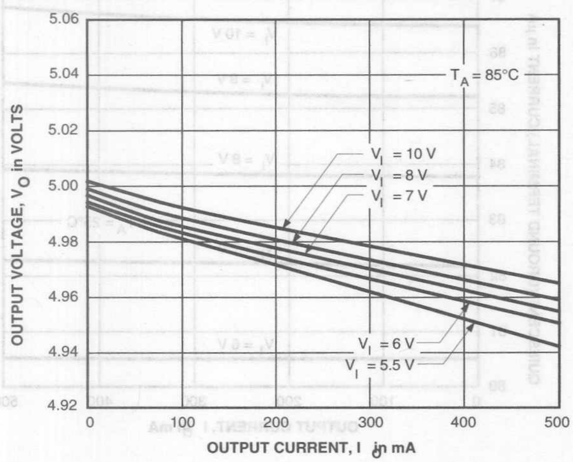


Dwg. GP-040-1

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

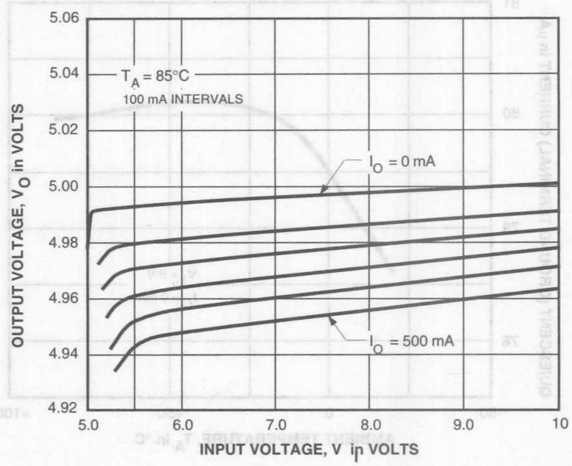
TYPICAL CHARACTERISTICS (cont'd)

LOAD REGULATION



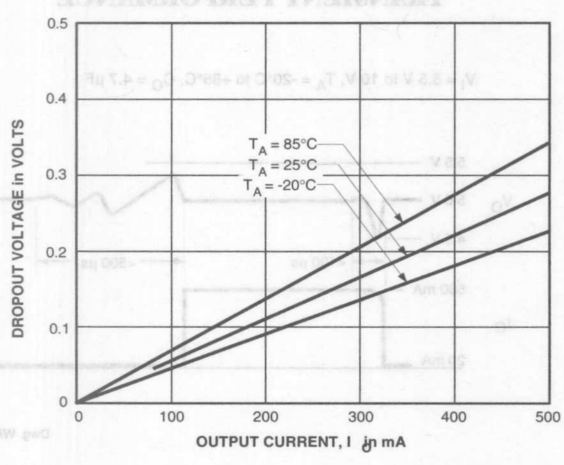
Dwg. GP-039-2

LINE REGULATION



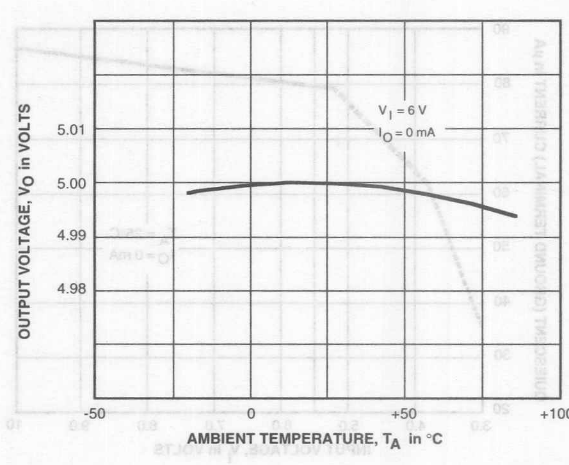
Dwg. GP-040-2

DROPOUT VOLTAGE



Dwg. GP-041

OUTPUT VOLTAGE vs TEMP.

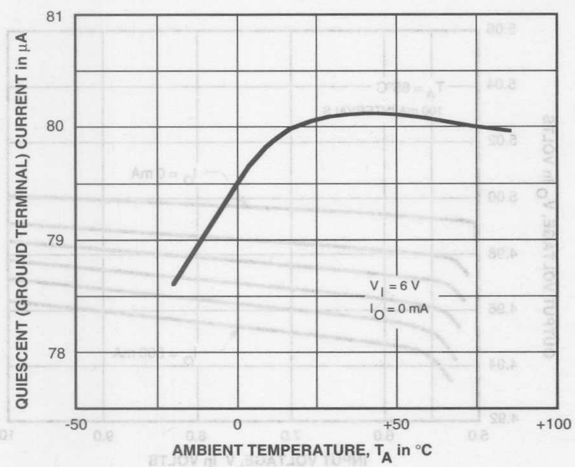


Dwg. GP-036

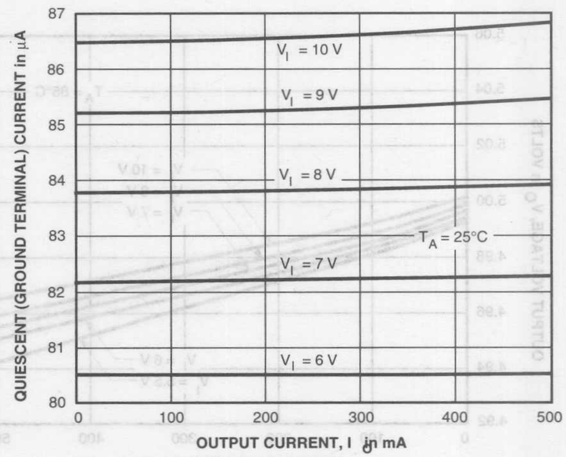
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (cont'd)

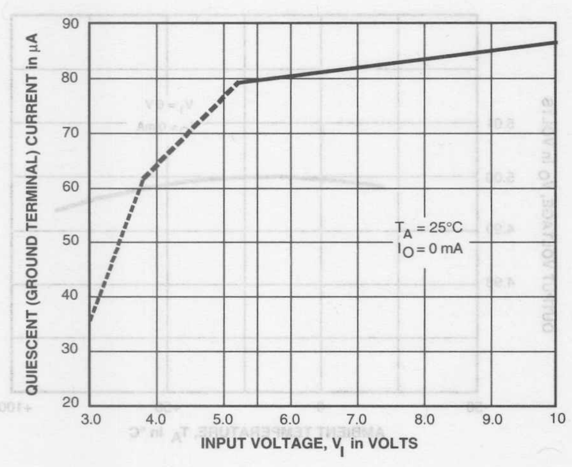
QUIESCENT (GROUND TERMINAL) CURRENT



Dwg. GP-037

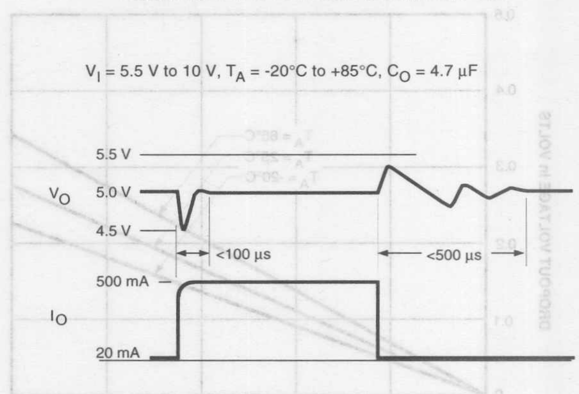


Dwg. GP-038



Dwg. GP-042

TRANSIENT PERFORMANCE



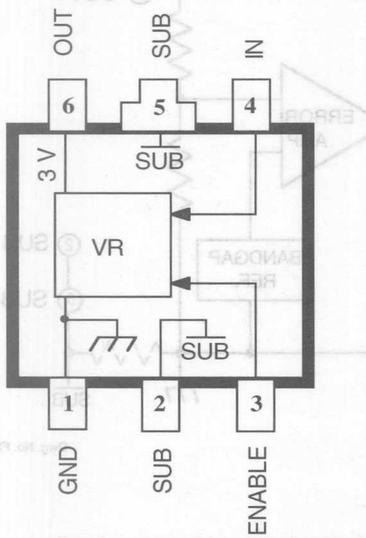
Dwg. WP-018

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

8183

27468.4A

LOW-DROPOUT, 3 V REGULATOR — HIGH EFFICIENCY



Dwg. No. PS-021

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_I	**10 V**
Output Current, I_O	**250 mA***
Enable Input Voltage, V_E	V_I
Operating Temperature Range, T_A	**-20°C to +85°C**
Junction Temperature, T_J	**+150°C†**
Storage Temperature Range, T_S	**-40°C to +150°C**

* Output current rating is limited by input voltage, duty cycle, and ambient temperature. Under any set of conditions, do not exceed a junction temperature of +150°C. See next page.

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed specifically to meet the requirement for extended operation of battery-powered equipment such as cordless and cellular telephones, the A8183SLU voltage regulator offers the reduced dropout voltage and quiescent current essential for maximum battery life. Applicable also to palmtop computers and personal data assistants, the device delivers a regulated, continuous 3 V output at up to 75 mA under normal operating conditions, or to 250 mA (transient) under worst-case conditions.

A PMOS pass element provides a typical dropout voltage of only 90 mV at 60 mA of load current. The low dropout voltage permits deeper battery discharge before output regulation is lost. Furthermore, quiescent current does not increase as the dropout voltage is approached, an ideal feature in standby/resume power systems where data integrity is crucial. Regulator accuracy and excellent temperature characteristics are provided by a bandgap reference. An ENABLE input gives the designer complete control over power up, standby, or power down.

This device is supplied in a 6-lead small-outline plastic package (similar to the SOT-89/TO-243AA) for surface-mount applications. The A8183SLU is rated for operation over a temperature range of -20°C to +85°C.

FEATURES AND BENEFITS

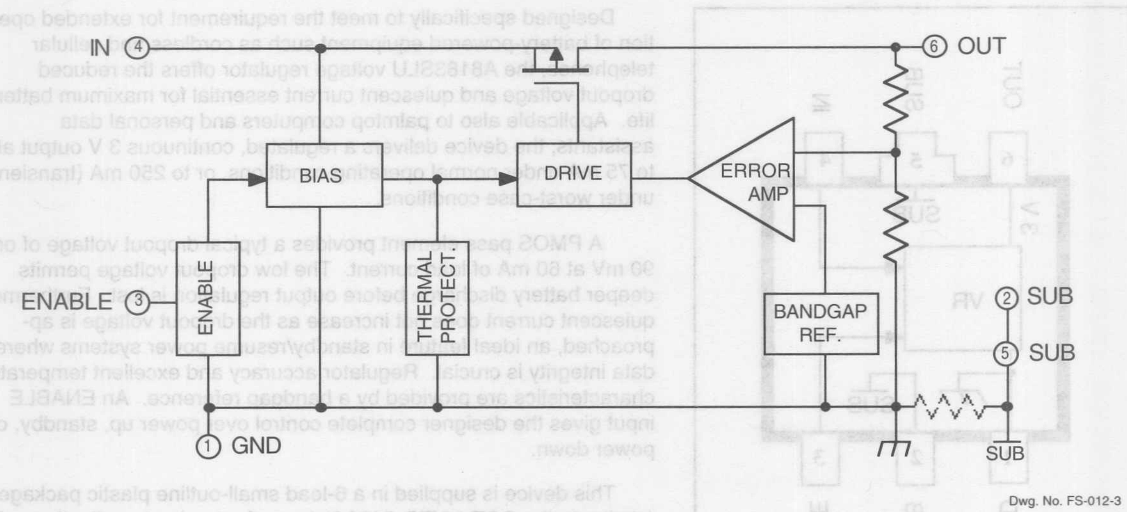
- High Efficiency Provides Extended Battery Life
- 90 mV Typical Dropout Voltage at I_O = 60 mA
- 45 μA Typical Quiescent Current at V_I = 6 V Less Than 1 μA "Sleep" Current
- Up to 250 mA Output Current
- CMOS-Compatible ON/OFF Control For Power-Up, Standby, or Shutdown
- Internal Thermal Protection
- Surface-Mount Package

APPLICATIONS

- Cordless and Cellular Telephones
- Personal Data Assistants
- Personal Communicators
- Palmtop Computers

Always order by complete part number: **A8183SLU** .

FUNCTIONAL BLOCK DIAGRAM



Terminal numbering is in accordance with EIA/JEDEC convention. Where EIAJ conventions apply, the tab is not numbered, resulting in terminal 6 being designated terminal 5.

For proper operation, terminals 1 and 2 must be externally connected together.

MAXIMUM ALLOWABLE OUTPUT CURRENT with device mounted on 2.24" x 2.24" (56.9 mm x 56.9 mm) solder-coated copper-clad board in still air.

	Maximum Allowable Output Current in Milliamperes with V_I = 8 V, T_J = 150°C, Period ≤10 s*								
	dc (Duty Cycle)								
T_A	100%	90%	80%	70%	60%	50%	40%	30%	20%
25°C	95	105	120	135	160	190	240	250	250
50°C	75	85	95	110	125	155	190	250	250
70°C	60	65	75	85	100	120	155	205	250
85°C	50	55	60	70	80	100	125	165	250

* $I_O = (T_J - T_A)/([V_I - V_O]\, R_{\theta JA} \bullet dc) = (150 - T_A)/(5 \bullet 258 \bullet dc)$

Output current rating can be increased (to 250 mA maximum) by heat sinking or reducing the input voltage. Conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

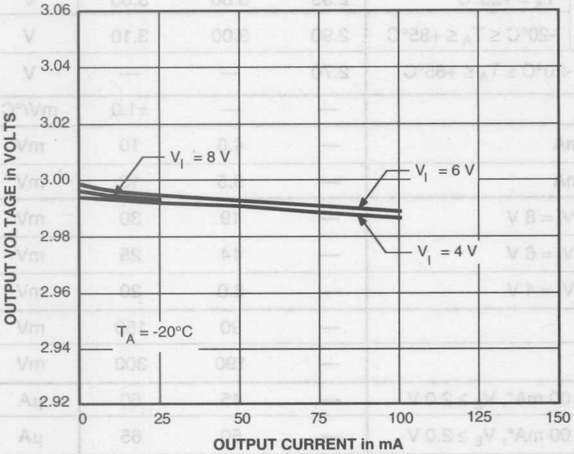
Characteristic	Symbol	Test Conditions		Limits Min.	Limits Typ.	Limits Max.	Units
Output Voltage	V_O	$4\ V \le V_I \le 8\ V$,	T_A = +25°C	2.95	3.00	3.05	V
		$10\ \mu A \le I_O \le 100\ mA$*	$-20°C \le T_A \le +85°C$	2.90	3.00	3.10	V
		$V_I = 3\ V$, $I_O = 60\ mA$*, $-20°C \le T_A \le +85°C$		2.70	—	—	V
Output Volt. Temp. Coeff.	α_{VO}	$V_I = 6\ V$, $I_O = 10\ mA$		—	—	±1.0	mV/°C
Line Regulation	$\Delta V_{O(\Delta VI)}$	$6\ V \le V_I \le 8\ V$, $I_O = 1\ mA$		—	4.0	10	mV
		$4\ V \le V_I \le 6\ V$, $I_O = 1\ mA$		—	9.5	18	mV
Load Regulation	$\Delta V_{O(\Delta IO)}$	$1\ mA \le I_O \le 100\ mA$*, $V_I = 8\ V$		—	19	30	mV
		$1\ mA \le I_O \le 100\ mA$*, $V_I = 6\ V$		—	14	25	mV
		$1\ mA \le I_O \le 100\ mA$*, $V_I = 4\ V$		—	8.0	20	mV
Dropout Voltage	$V_I min - V_O$	$I_O = 60\ mA$*		—	90	150	mV
		$I_O = 125\ mA$*		—	190	300	mV
Quiescent Current	I_Q	$V_I = 6\ V$, $1\ mA \le I_O \le 100\ mA$*, $V_E \ge 2.0\ V$		—	45	60	µA
(GND terminal current)		$V_I = 8\ V$, $1\ mA \le I_O \le 100\ mA$*, $V_E \ge 2.0\ V$		—	50	65	µA
	$I_{Q(off)}$	$4\ V \le V_I \le 8\ V$, $V_E \le 0.8\ V$		—	—	1.0	µA
ENABLE Input Voltage	V_{EH}	$4\ V \le V_I \le 8\ V$,	Output ON	2.0	—	—	V
	V_{EL}	$-20°C \le T_A \le +85°C$	Output OFF	—	—	0.8	V
ENABLE Input Current	I_E	$T_A \le +85°C$, $V_E = V_I = 8\ V$		—	—	±0.1	µA
Power Supply Rejection Ratio	PSRR	$V_I = 4.5\ V$, $V_i = 100\ mV$ @ 400 Hz, $I_O = 10\ mA$		—	-45	—	dB
Output Noise Voltage	V_n	f = 10 Hz to 100 kHz, $I_O = 10\ mA$: $C_O = 0$		—	1.0	—	µV/Hz
		$C_O = 10\ \mu F$		—	2.0	—	µV/Hz
Thermal Shutdown Temp.	T_J			150	—	—	°C
Thermal Resistance	$R_{\theta JA}$	Mounted on 2.24" x 2.24" solder-coated copper-clad board in still air		—	258	—	°C/W

Typical values are at T_A = +25°C and are given for circuit design information only.

* Pulse test (≤20 ms). See previous page for duty cycle limitations.

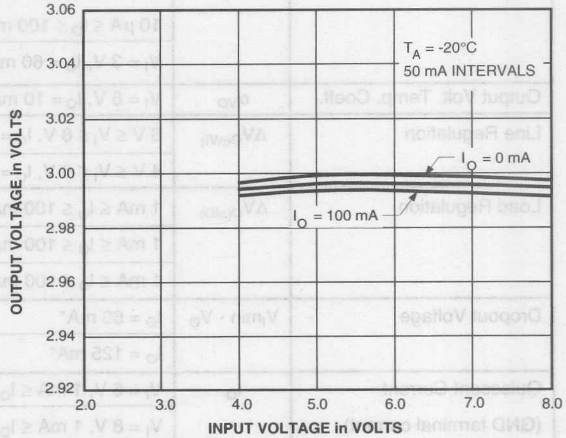
TYPICAL CHARACTERISTICS

LOAD REGULATION

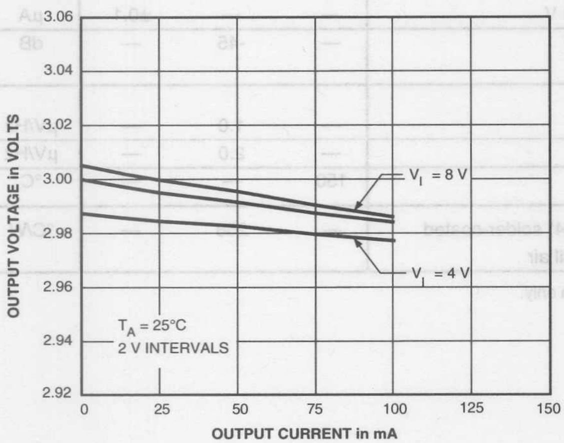


Dwg. No. GP-052-3

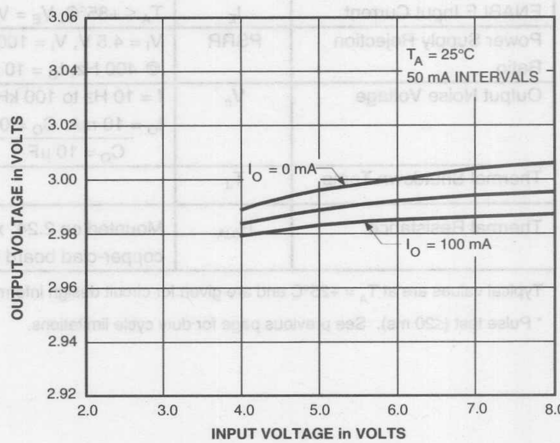
LINE REGULATION



Dwg. No. GP-053-3



Dwg. No. GP-052-4



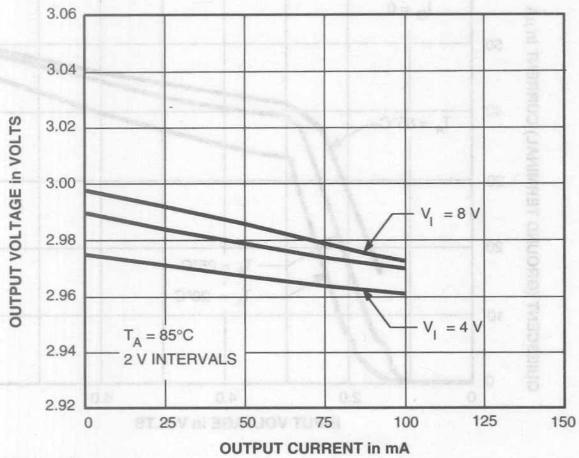
Dwg. No. GP-053-4

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

8183
LOW-DROPOUT, 3 V REGULATOR

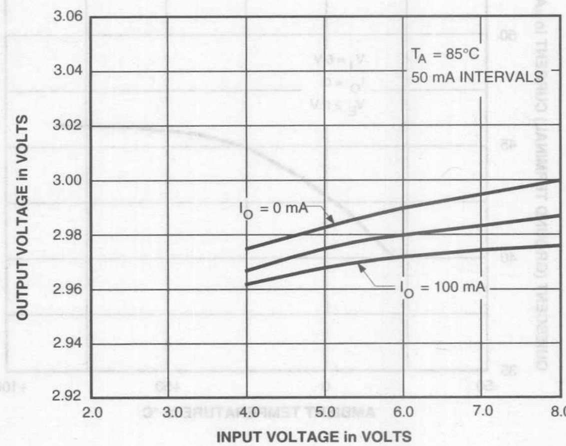
TYPICAL CHARACTERISTICS (cont'd)

LOAD REGULATION



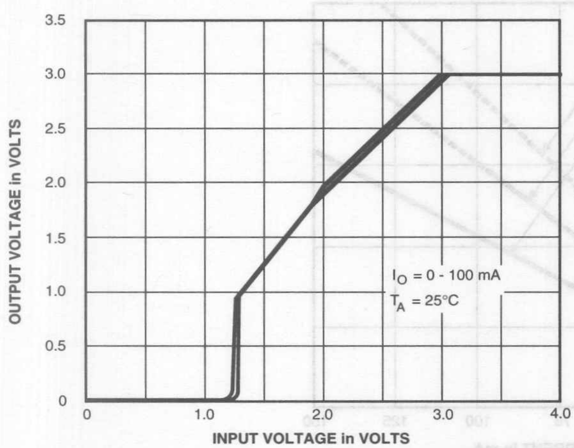
Dwg. No. GP-052-5

LINE REGULATION

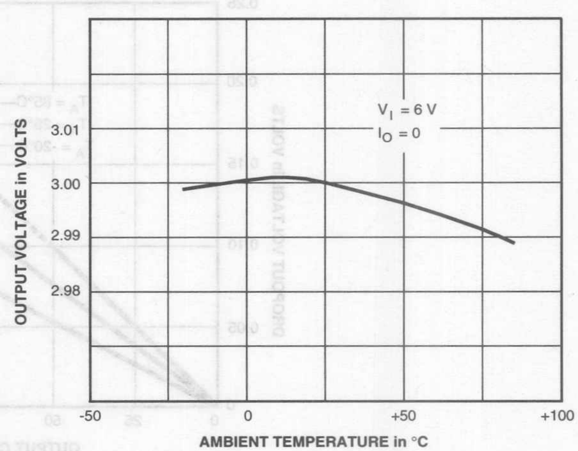


Dwg. No. GP-053-5

OUTPUT VOLTAGE



Dwg. No. GP-059

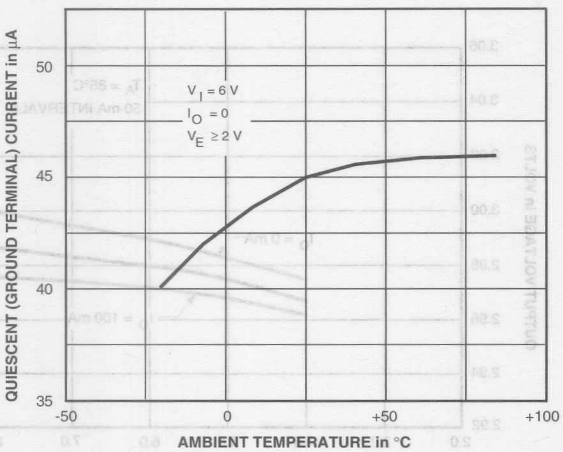


Dwg. No. GP-050-1

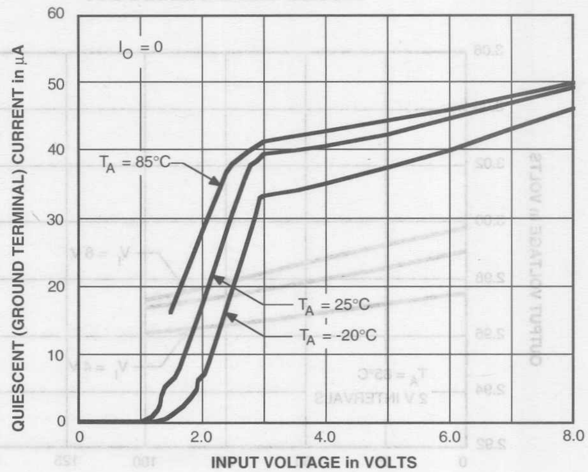
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (cont'd)

QUIESCENT (GROUND TERMINAL) CURRENT

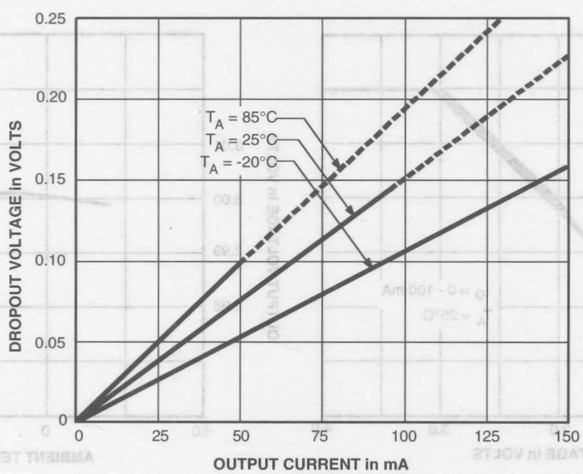


Dwg. No. GP-051-1



Dwg. No. GP-058

DROPOUT VOLTAGE



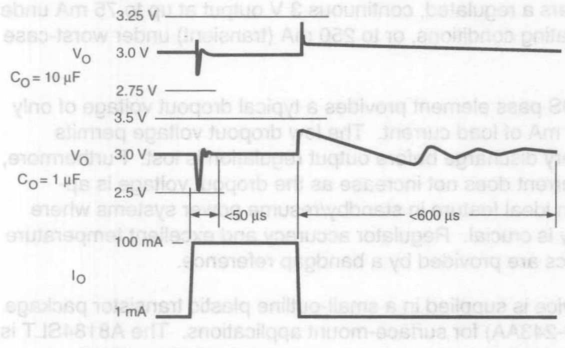
Dwg. No. GP-054-1

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (concluded)

LOAD TRANSIENT PERFORMANCE

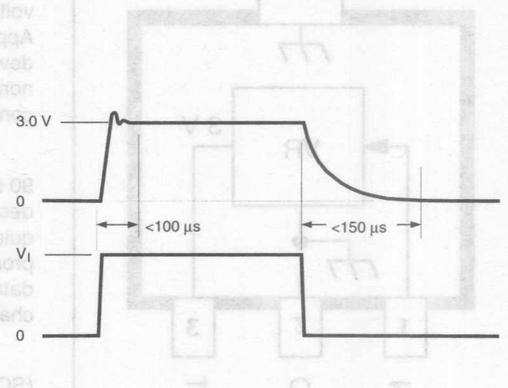
V_I = 3.2 V to 6.2 V, C_O as specified, T_A = 25°C



Dwg. No. WP-026

ENABLE TRANSIENT PERFORMANCE

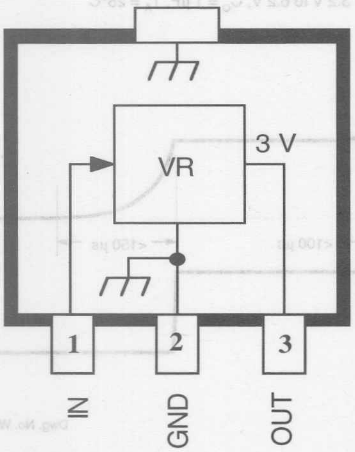
V_I = 3.2 V to 6.2 V, C_O = 1 µF, T_A = 25°C



Dwg. No. WP-027-1

8184

LOW-DROPOUT, 3 V REGULATOR — HIGH EFFICIENCY



Dwg. PS-022

Designed specifically to meet the requirement for extended operation of battery-powered equipment such as cordless and cellular telephones, the A8184SLT voltage regulator offers the reduced dropout voltage and quiescent current essential for maximum battery life. Applicable also to palmtop computers and personal data assistants, the device delivers a regulated, continuous 3 V output at up to 75 mA under normal operating conditions, or to 250 mA (transient) under worst-case conditions.

A PMOS pass element provides a typical dropout voltage of only 90 mV at 60 mA of load current. The low dropout voltage permits deeper battery discharge before output regulation is lost. Furthermore, quiescent current does not increase as the dropout voltage is approached, an ideal feature in standby/resume power systems where data integrity is crucial. Regulator accuracy and excellent temperature characteristics are provided by a bandgap reference.

This device is supplied in a small-outline plastic transistor package (SOT-89/TO-243AA) for surface-mount applications. The A8184SLT is rated for operation over a temperature range of -20°C to +85°C. A similar device with an ENABLE input for control over sequential power up, standby, or power down is the A8183SLU.

FEATURES AND BENEFITS

- High Efficiency Provides Extended Battery Life
- 90 mV Typical Dropout Voltage at I_O = 60 mA
- 45 µA Typical Quiescent Current at V_I = 6 V
- Up to 250 mA Output Current
- Internal Thermal Protection
- Surface-Mount Package

APPLICATIONS

- Cordless and Cellular Telephones
- Personal Data Assistants
- Personal Communicators
- Palmtop Computers

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_I . . . . **10 V**

Output Current, I_O . . . . **250 mA***

Operating Temperature Range,
T_A . . . . **-20°C to +85°C**

Junction Temperature, T_J . . . . **+150°C†**

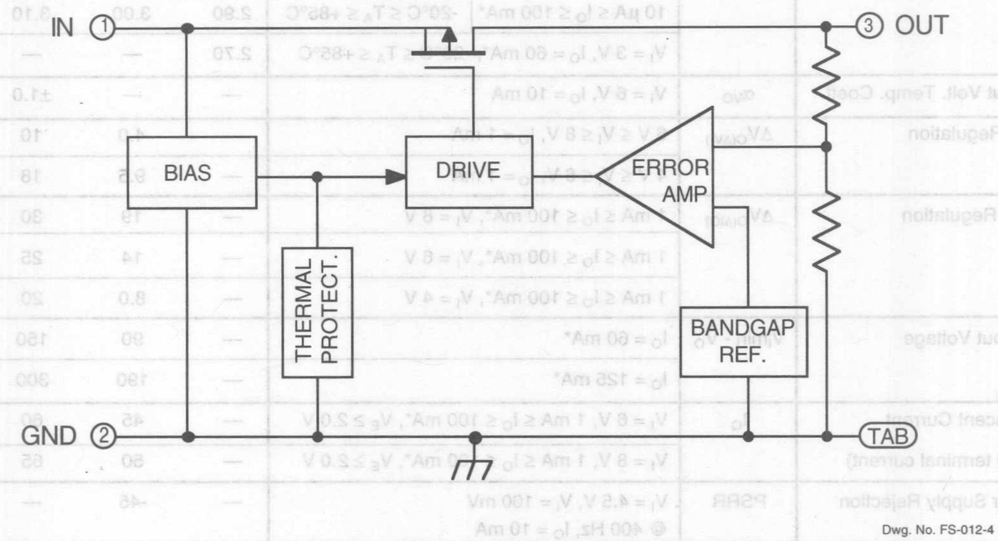
Storage Temperature Range,
T_S . . . . **-40°C to +150°C**

* Output current rating is limited by input voltage, duty cycle, and ambient temperature. Under any set of conditions, do not exceed a junction temperature of +150°C. See next page.

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Always order by complete part number: **A8184SLT**

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM ALLOWABLE OUTPUT CURRENT with device mounted on 2.24" x 2.24" (56.9 mm x 56.9 mm) solder-coated copper-clad board in still air.

	Maximum Allowable Output Current in Milliamperes with V_I = 8 V, T_J = 150°C, Period ≤10 s*								
	dc (Duty Cycle)								
T_A	100%	90%	80%	70%	60%	50%	40%	30%	20%
25°C	95	105	120	135	160	190	240	250	250
50°C	75	85	95	110	125	155	190	250	250
70°C	60	65	75	85	100	120	155	205	250
85°C	50	55	60	70	80	100	125	165	250

* $I_O = (T_J - T_A)/([V_I - V_O]\ R_{\theta JA} \bullet dc) = (150 - T_A)/(5 \bullet 258 \bullet dc)$

Output current rating can be increased (to 250 mA maximum) by heat sinking or reducing the input voltage. Conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

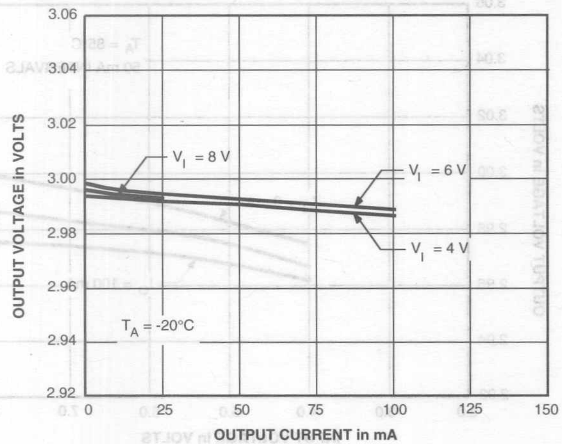
Characteristic	Symbol	Test Conditions		Limits Min.	Typ.	Max.	Units
Output Voltage	V_O	4 V ≤ V_I ≤ 8 V,	T_A = +25°C	2.95	3.00	3.05	V
		10 µA ≤ I_O ≤ 100 mA*	-20°C ≤ T_A ≤ +85°C	2.90	3.00	3.10	V
		V_I = 3 V, I_O = 60 mA*, -20°C ≤ T_A ≤ +85°C		2.70	—	—	V
Output Volt. Temp. Coeff.	α_{VO}	V_I = 6 V, I_O = 10 mA		—	—	±1.0	mV/°C
Line Regulation	$\Delta V_{O(\Delta VI)}$	6 V ≤ V_I ≤ 8 V, I_O = 1 mA		—	4.0	10	mV
		4 V ≤ V_I ≤ 6 V, I_O = 1 mA		—	9.5	18	mV
Load Regulation	$\Delta V_{O(\Delta IO)}$	1 mA ≤ I_O ≤ 100 mA*, V_I = 8 V		—	19	30	mV
		1 mA ≤ I_O ≤ 100 mA*, V_I = 6 V		—	14	25	mV
		1 mA ≤ I_O ≤ 100 mA*, V_I = 4 V		—	8.0	20	mV
Dropout Voltage	$V_I$min - V_O	I_O = 60 mA*		—	90	150	mV
		I_O = 125 mA*		—	190	300	mV
Quiescent Current	I_Q	V_I = 6 V, 1 mA ≤ I_O ≤ 100 mA*, V_E ≥ 2.0 V		—	45	60	µA
(GND terminal current)		V_I = 8 V, 1 mA ≤ I_O ≤ 100 mA*, V_E ≥ 2.0 V		—	50	65	µA
Power Supply Rejection Ratio	PSRR	V_I = 4.5 V, V_i = 100 mV @ 400 Hz, I_O = 10 mA		—	-45	—	dB
Output Noise Voltage	V_n	f = 10 Hz to 100 kHz, I_O = 10 mA: C_O = 0		—	1.0	—	µV/Hz
		C_O = 10 µF		—	2.0	—	µV/Hz
Thermal Shutdown Temp.	T_J			150	—	—	°C
Thermal Resistance	$R_{\theta JA}$	Mounted on 2.24" x 2.24" solder-coated copper-clad board in still air		—	258	—	°C/W

Typical values are at T_A = +25°C and are given for circuit design information only.

* Pulse test (≤20 ms). See previous page for duty cycle limitations.

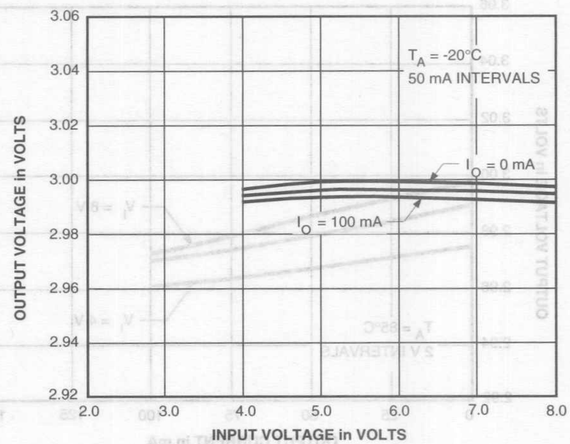
TYPICAL CHARACTERISTICS

LOAD REGULATION

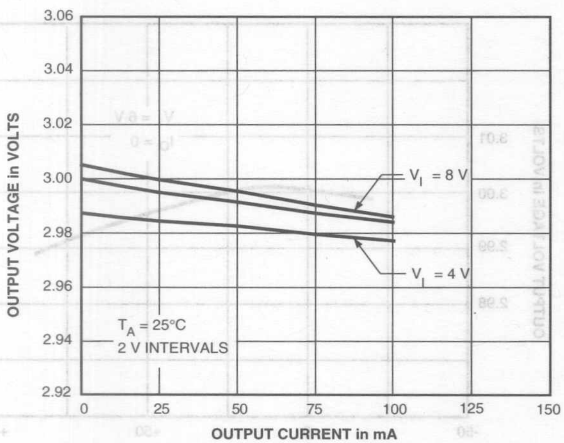


Dwg. No. GP-052-3

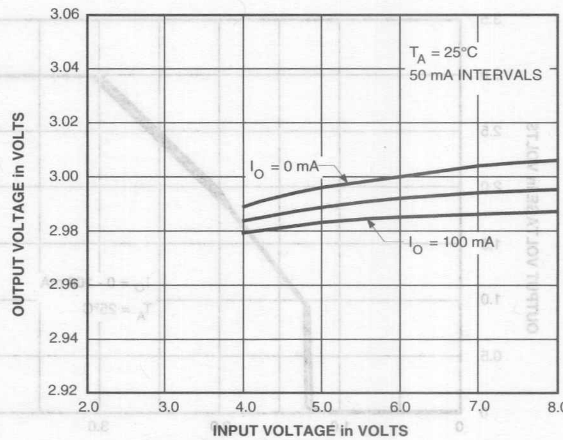
LINE REGULATION



Dwg. No. GP-053-3



Dwg. No. GP-052-4

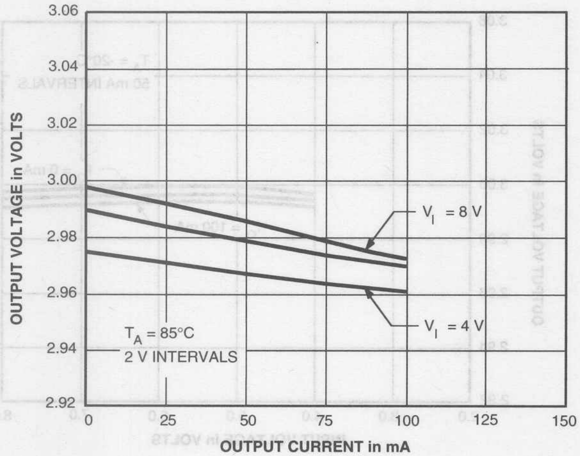


Dwg. No. GP-053-4

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

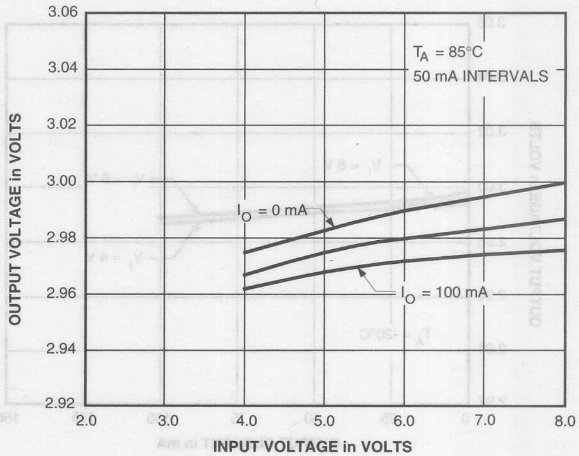
TYPICAL CHARACTERISTICS (cont'd)

LOAD REGULATION



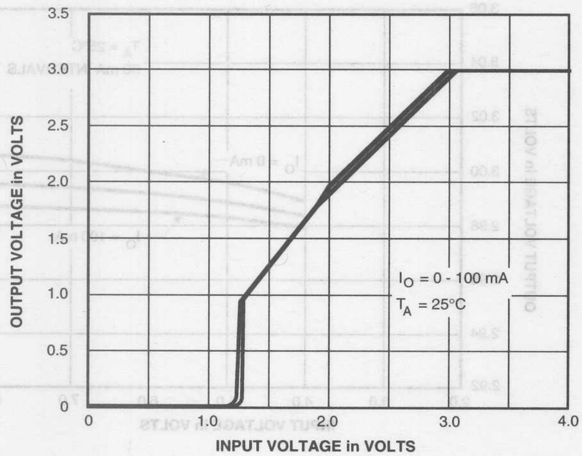
Dwg. No. GP-052-5

LINE REGULATION

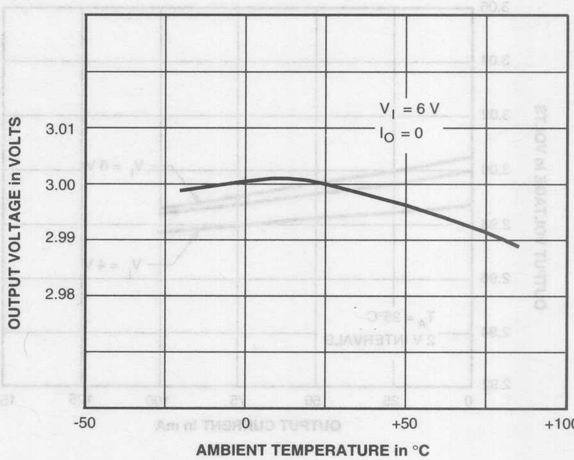


Dwg. No. GP-053-5

OUTPUT VOLTAGE



Dwg. No. GP-059

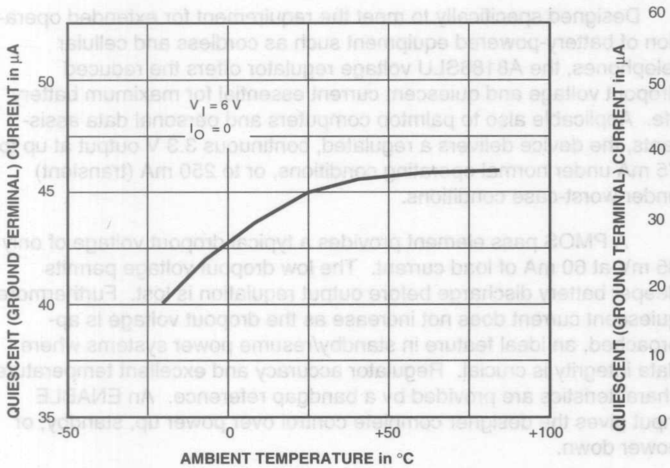


Dwg. No. GP-050-1

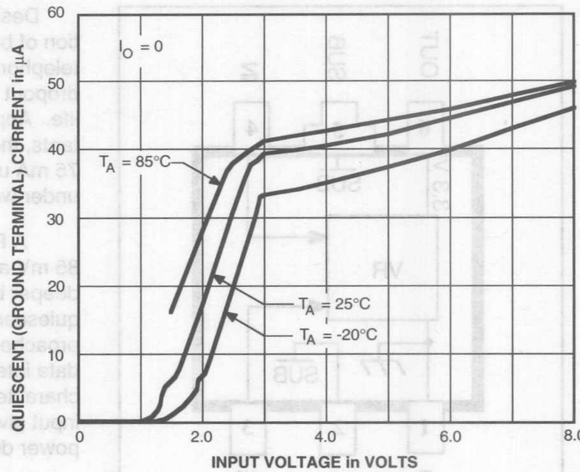
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (concluded)

QUIESCENT (GROUND TERMINAL) CURRENT

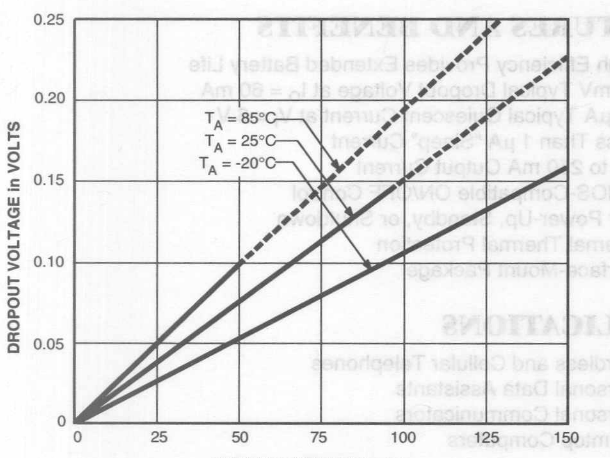


Dwg. No. GP-051-2



Dwg. No. GP-058

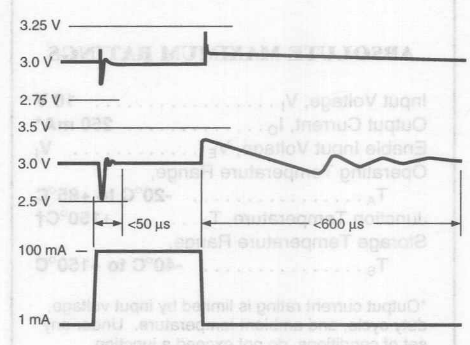
DROPOUT VOLTAGE



Dwg. No. GP-054-1

LOAD TRANSIENT PERFORMANCE

V_I = 3.2 V to 6.2 V, C_O as specified, T_A = 25°C



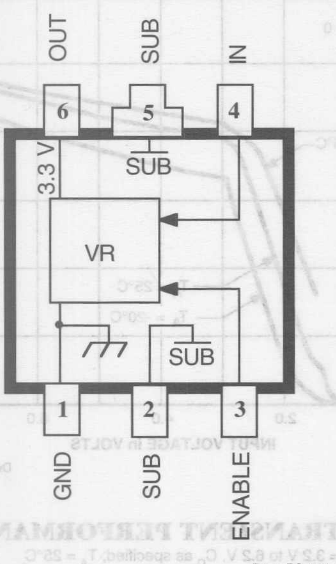
Dwg. No. WP-028

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

8186

27468.14

LOW-DROPOUT, 3.3 V REGULATOR — HIGH EFFICIENCY



Dwg. PS-021-1

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_I . . . . **10 V**
Output Current, I_O . . . . **250 mA***
Enable Input Voltage, V_E . . . . V_I
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Junction Temperature, T_J . . . . **+150°C†**
Storage Temperature Range,
T_S . . . . **-40°C to +150°C**

*Output current rating is limited by input voltage, duty cycle, and ambient temperature. Under any set of conditions, do not exceed a junction temperature of +150°C. See next page.

†Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Designed specifically to meet the requirement for extended operation of battery-powered equipment such as cordless and cellular telephones, the A8186SLU voltage regulator offers the reduced dropout voltage and quiescent current essential for maximum battery life. Applicable also to palmtop computers and personal data assistants, the device delivers a regulated, continuous 3.3 V output at up to 75 mA under normal operating conditions, or to 250 mA (transient) under worst-case conditions.

A PMOS pass element provides a typical dropout voltage of only 85 mV at 60 mA of load current. The low dropout voltage permits deeper battery discharge before output regulation is lost. Furthermore, quiescent current does not increase as the dropout voltage is approached, an ideal feature in standby/resume power systems where data integrity is crucial. Regulator accuracy and excellent temperature characteristics are provided by a bandgap reference. An ENABLE input gives the designer complete control over power up, standby, or power down.

This device is supplied in a 6-lead small-outline plastic package (similar to the SOT-89/TO-243AA) for surface-mount applications. The A8186SLU is rated for operation over a temperature range of -20°C to +85°C.

FEATURES AND BENEFITS

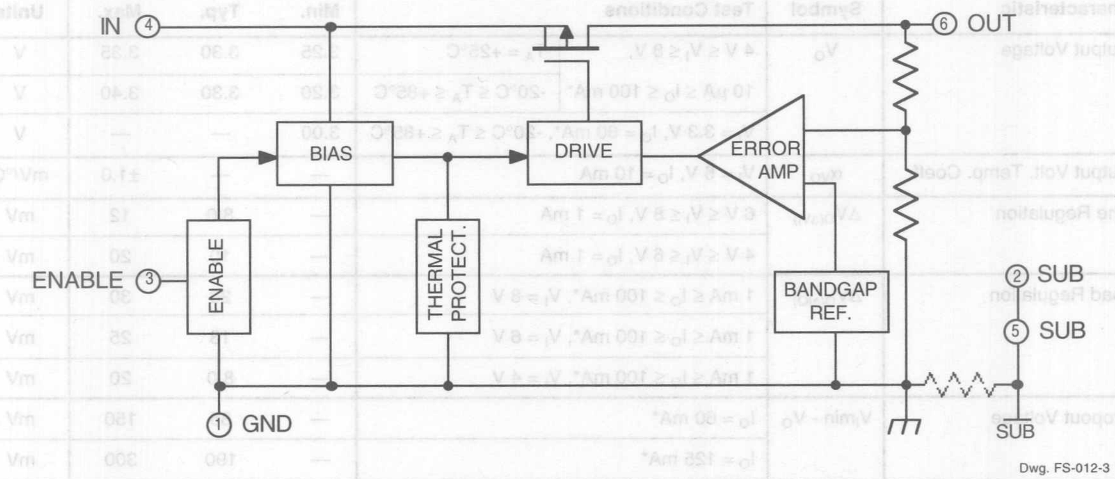
- High Efficiency Provides Extended Battery Life
- 85 mV Typical Dropout Voltage at I_O = 60 mA
- 45 µA Typical Quiescent Current at V_I = 6 V
  Less Than 1 µA "Sleep" Current
- Up to 250 mA Output Current
- CMOS-Compatible ON/OFF Control
  For Power-Up, Standby, or Shutdown
- Internal Thermal Protection
- Surface-Mount Package

APPLICATIONS

- Cordless and Cellular Telephones
- Personal Data Assistants
- Personal Communicators
- Palmtop Computers

Always order by complete part number: **A8186SLU** .

FUNCTIONAL BLOCK DIAGRAM



Terminal numbering is in accordance with EIA/JEDEC convention. Where EIAJ conventions apply, the tab is not numbered, resulting in terminal 6 being designated terminal 5.

For proper operation, terminals 1 and 2 must be externally connected together.

MAXIMUM ALLOWABLE OUTPUT CURRENT with device mounted on 2.24" x 2.24" (56.9 mm x 56.9 mm) solder-coated copper-clad board in still air.

	Maximum Allowable Output Current in Milliamperes with V_I = 8 V, T_J = 150°C, Period ≤10 s*								
	dc (Duty Cycle)								
T_A	100%	90%	80%	70%	60%	50%	40%	30%	20%
25°C	100	115	125	145	170	205	250	250	250
50°C	80	90	100	115	135	165	205	250	250
70°C	65	70	80	90	110	130	165	220	250
85°C	50	60	65	75	85	105	130	175	250

*$I_O = (T_J - T_A)/([V_I - V_O]\ R_{\theta JA} \bullet dc) = (150 - T_A)/(4.7 \bullet 258 \bullet dc)$
Output current rating can be increased (to 250 mA maximum) by heat sinking or reducing the input voltage. Conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

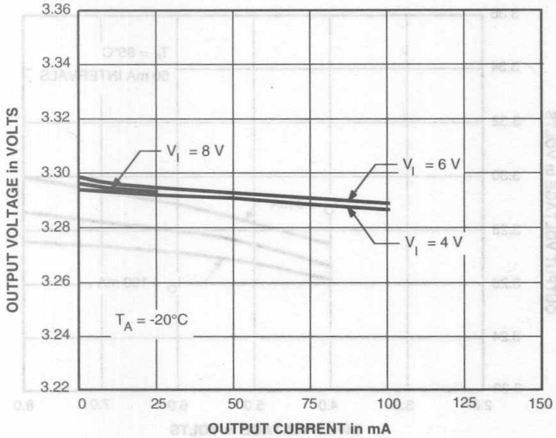
ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions		Limits Min.	Typ.	Max.	Units
Output Voltage	V_O	$4\ V \le V_I \le 8\ V$,	$T_A = +25°C$	3.25	3.30	3.35	V
		$10\ \mu A \le I_O \le 100\ mA^*$	$-20°C \le T_A \le +85°C$	3.20	3.30	3.40	V
		$V_I = 3.3\ V, I_O = 60\ mA^*, -20°C \le T_A \le +85°C$		3.00	—	—	V
Output Volt. Temp. Coeff.	α_{VO}	$V_I = 6\ V, I_O = 10\ mA$		—	—	±1.0	mV/°C
Line Regulation	$\Delta V_{O(\Delta VI)}$	$6\ V \le V_I \le 8\ V, I_O = 1\ mA$		—	8.0	12	mV
		$4\ V \le V_I \le 6\ V, I_O = 1\ mA$		—	10	20	mV
Load Regulation	$\Delta V_{O(\Delta IO)}$	$1\ mA \le I_O \le 100\ mA^*, V_I = 8\ V$		—	20	30	mV
		$1\ mA \le I_O \le 100\ mA^*, V_I = 6\ V$		—	13	25	mV
		$1\ mA \le I_O \le 100\ mA^*, V_I = 4\ V$		—	8.0	20	mV
Dropout Voltage	$V_I min - V_O$	$I_O = 60\ mA^*$		—	85	150	mV
		$I_O = 125\ mA^*$		—	190	300	mV
Quiescent Current	I_Q	$V_I = 6\ V, 1\ mA \le I_O \le 100\ mA^*, V_E \ge 2.0\ V$		—	45	60	µA
(GND terminal current)		$V_I = 8\ V, 1\ mA \le I_O \le 100\ mA^*, V_E \ge 2.0\ V$		—	50	65	µA
	$I_{Q(off)}$	$4\ V \le V_I \le 8\ V, V_E \le 0.8\ V$		—	0.05	1.0	µA
ENABLE Input Voltage	V_{EH}	$4\ V \le V_I \le 8\ V$,	Output ON	2.0	—	—	V
	V_{EL}	$-20°C \le T_A \le +85°C$	Output OFF	—	—	0.8	V
ENABLE Input Current	I_E	$T_A \le +85°C, V_E = V_I = 8\ V$		—	—	±0.1	µA
Power Supply Rejection Ratio	PSRR	$V_I = 4.5\ V, V_i = 100\ mV$ @ 400 Hz, $I_O = 10\ mA$		—	-45	—	dB
Output Noise Voltage	V_n	f = 10 Hz to 100 kHz,					
		$I_O = 10\ mA$: $C_O = 0$		—	1.0	—	µV/Hz
		$C_O = 10\ \mu F$		—	2.0	—	µV/Hz
Thermal Shutdown Temp.	T_J			150	—	—	°C
Thermal Resistance	$R_{\theta JA}$	Mounted on 2.24" x 2.24" solder-coated copper-clad board in still air		—	258	—	°C/W

Typical values are at T_A = +25°C and are given for circuit design information only.
* Pulse test (≤20 ms). See previous page for duty cycle limitations.

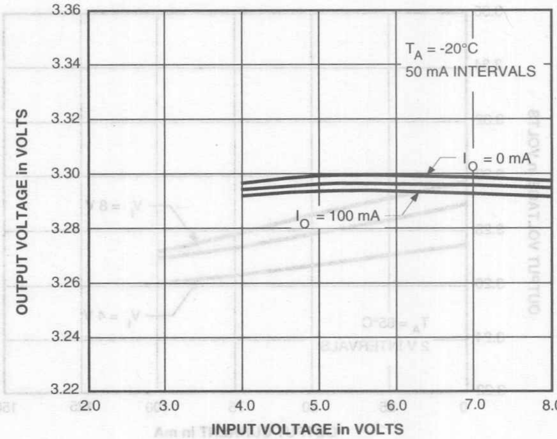
TYPICAL CHARACTERISTICS

LOAD REGULATION

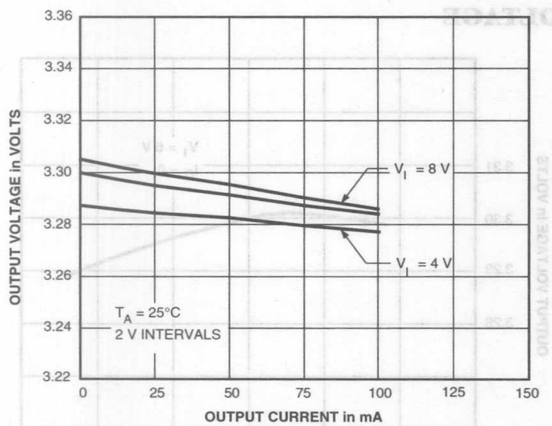


Dwg. GP-052-6

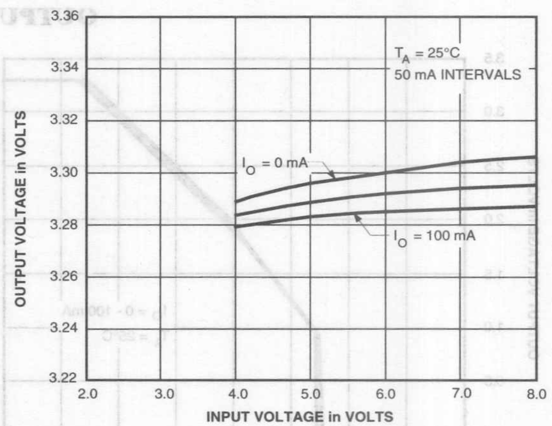
LINE REGULATION



Dwg. GP-053-6



Dwg. GP-052-7

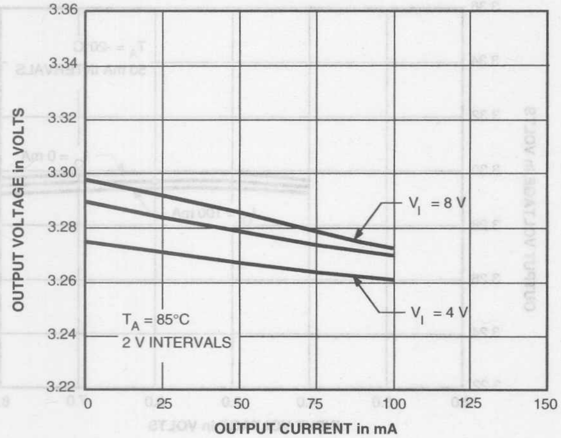


Dwg. GP-053-7

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

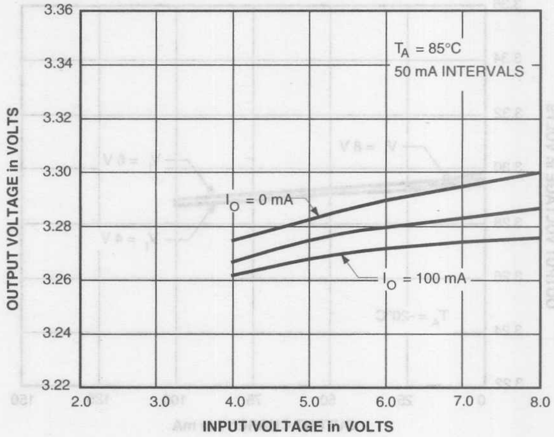
TYPICAL CHARACTERISTICS (cont'd)

LOAD REGULATION



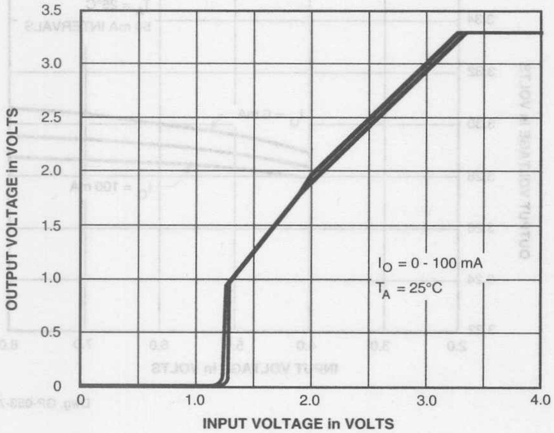
Dwg. GP-052-8

LINE REGULATION

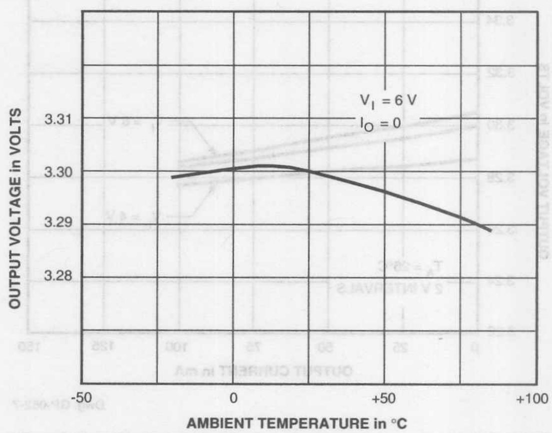


Dwg. GP-053-8

OUTPUT VOLTAGE



Dwg. GP-059-1

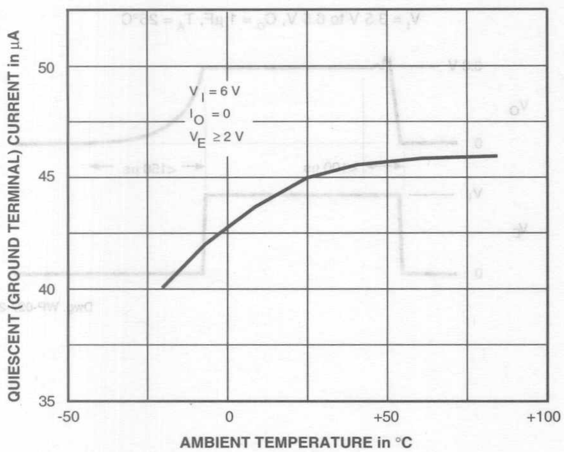


Dwg. GP-050-2

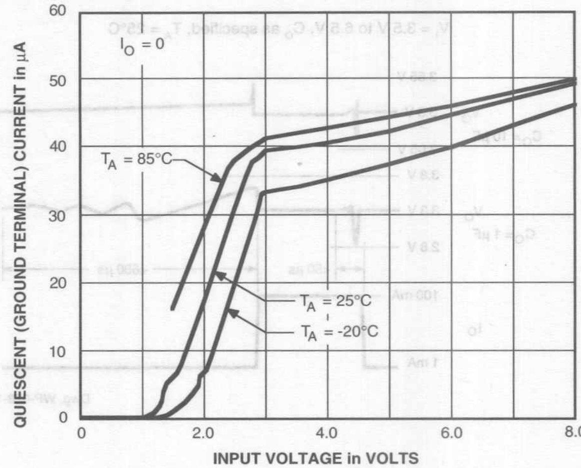
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (cont'd)

QUIESCENT (GROUND TERMINAL) CURRENT

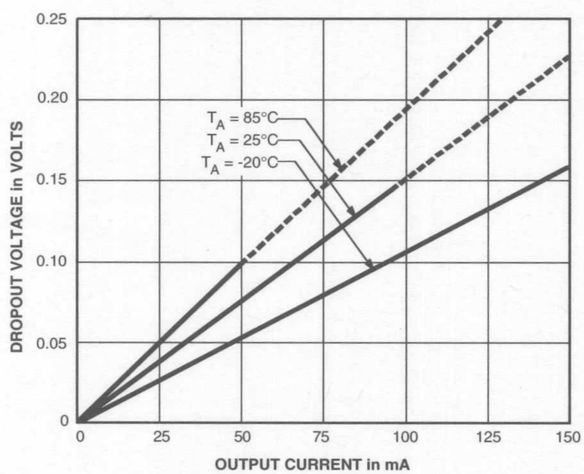


Dwg. GP-051-1



Dwg. GP-058

DROPOUT VOLTAGE

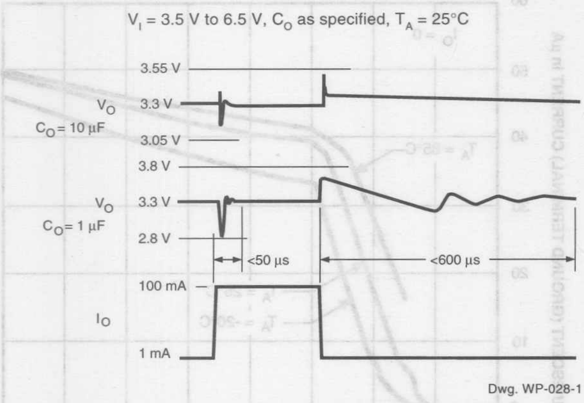


Dwg. GP-054-1

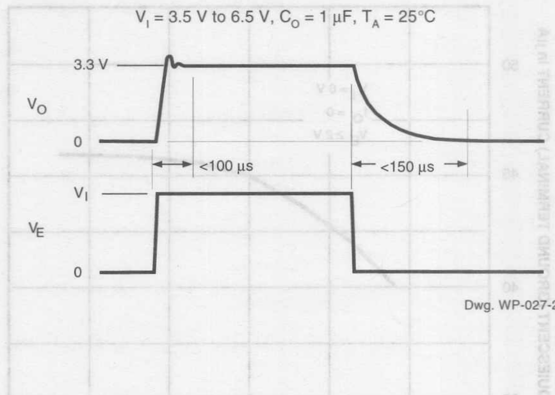
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (concluded)

LOAD TRANSIENT PERFORMANCE



ENABLE TRANSIENT PERFORMANCE



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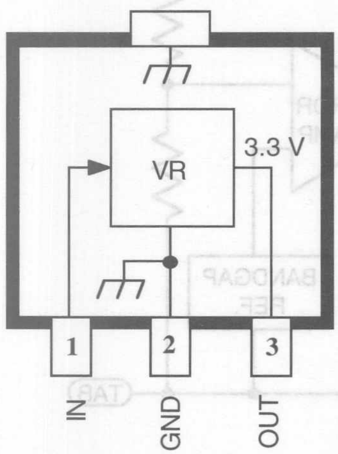
LOW-DROPOUT, 3.3 V REGULATOR — HIGH EFFICIENCY



Dwg. PS-022-1

Designed specifically to meet the requirement for extended operation of battery-powered equipment such as cordless and cellular telephones, the A8187SLT voltage regulator offers the reduced dropout voltage and quiescent current essential for maximum battery life. Applicable also to palmtop computers and personal data assistants, the device delivers a regulated, continuous 3.3 V output at up to 75 mA under normal operating conditions, or to 250 mA (transient) under worst-case conditions.

A PMOS pass element provides a typical dropout voltage of only 85 mV at 60 mA of load current. The low dropout voltage permits deeper battery discharge before output regulation is lost. Furthermore, quiescent current does not increase as the dropout voltage is approached, an ideal feature in standby/resume power systems where data integrity is crucial. Regulator accuracy and excellent temperature characteristics are provided by a bandgap reference.

This device is supplied in a small-outline plastic transistor package (SOT-89/TO-243AA) for surface-mount applications. The A8187SLT is rated for operation over a temperature range of -20°C to +85°C. A similar device with an ENABLE input for control over sequential power up, standby, or power down is the A8186SLU.

FEATURES AND BENEFITS

- High Efficiency Provides Extended Battery Life
- 85 mV Typical Dropout Voltage at I_O = 60 mA
- 45 µA Typical Quiescent Current at V_I = 6 V
- Up to 250 mA Output Current
- Internal Thermal Protection
- Surface-Mount Package

APPLICATIONS

- Cordless and Cellular Telephones
- Personal Data Assistants
- Personal Communicators
- Palmtop Computers

ABSOLUTE MAXIMUM RATINGS

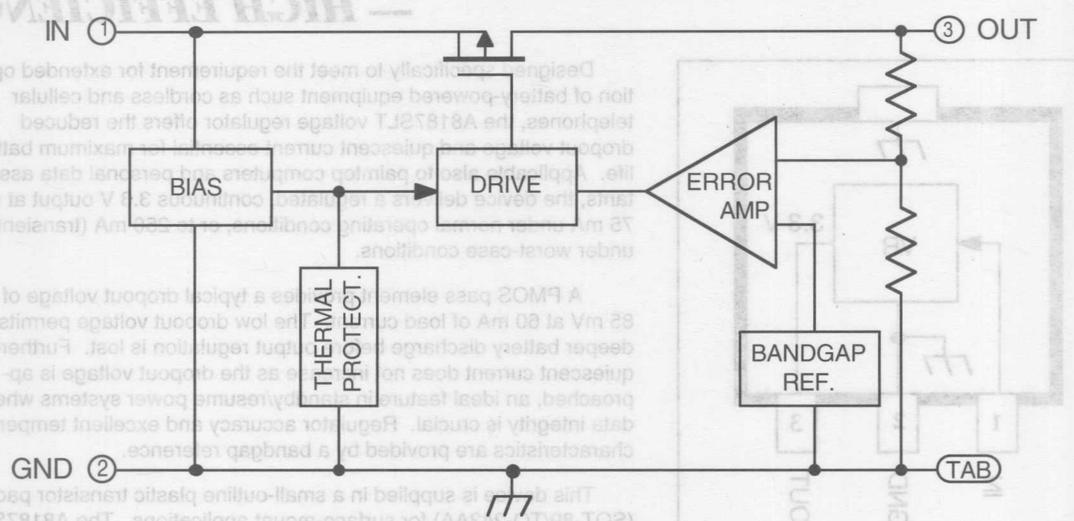
Input Voltage, V_I . . . . **10 V**
Output Current, I_O . . . . **250 mA***
Operating Temperature Range,
T_A . . . . **-20°C to +85°C**
Junction Temperature, T_J . . . . **+150°C†**
Storage Temperature Range,
T_S . . . . **-40°C to +150°C**

*Output current rating is limited by input voltage, duty cycle, and ambient temperature. Under any set of conditions, do not exceed a junction temperature of +150°C. See next page.

†Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

Always order by complete part number: **A8187SLT** .

FUNCTIONAL BLOCK DIAGRAM



Dwg. FS-012-4

MAXIMUM ALLOWABLE OUTPUT CURRENT with device mounted on 2.24" x 2.24" (56.9 mm x 56.9 mm) solder-coated copper-clad board in still air.

	Maximum Allowable Output Current in Milliamperes with V_I = 8 V, T_J = 150°C, Period ≤10 s*								
	dc (Duty Cycle)								
T_A	100%	90%	80%	70%	60%	50%	40%	30%	20%
25°C	100	115	125	145	170	205	250	250	250
50°C	80	90	100	115	135	165	205	250	250
70°C	65	70	80	90	110	130	165	220	250
85°C	50	60	65	75	85	105	130	175	250

*$I_O = (T_J - T_A)/([V_I - V_O]\, R_{\theta JA} \bullet dc) = (150 - T_A)/(4.7 \bullet 258 \bullet dc)$
Output current rating can be increased (to 250 mA maximum) by heat sinking or reducing the input voltage. Conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated but should be avoided.

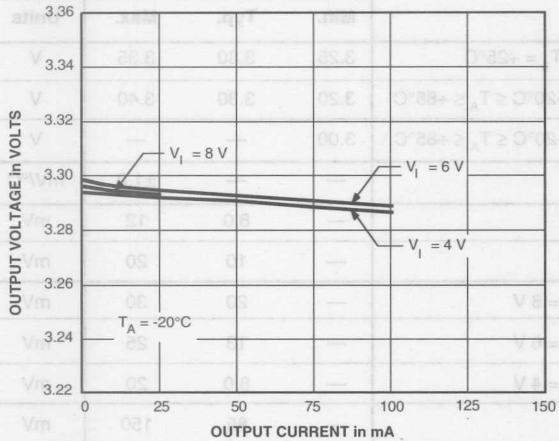
ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted).

Characteristic	Symbol	Test Conditions		Limits Min.	Limits Typ.	Limits Max.	Units
Output Voltage	V_O	$4\ V \le V_I \le 8\ V$,	T_A = +25°C	3.25	3.30	3.35	V
		$10\ \mu A \le I_O \le 100$ mA*	$-20°C \le T_A \le +85°C$	3.20	3.30	3.40	V
		V_I = 3.3 V, I_O = 60 mA*, $-20°C \le T_A \le +85°C$		3.00	—	—	V
Output Volt. Temp. Coeff.	α_{VO}	V_I = 6 V, I_O = 10 mA		—	—	±1.0	mV/°C
Line Regulation	$\Delta V_{O(\Delta VI)}$	$6\ V \le V_I \le 8\ V$, I_O = 1 mA		—	8.0	12	mV
		$4\ V \le V_I \le 6\ V$, I_O = 1 mA		—	10	20	mV
Load Regulation	$\Delta V_{O(\Delta IO)}$	$1\ mA \le I_O \le 100$ mA*, V_I = 8 V		—	20	30	mV
		$1\ mA \le I_O \le 100$ mA*, V_I = 6 V		—	13	25	mV
		$1\ mA \le I_O \le 100$ mA*, V_I = 4 V		—	8.0	20	mV
Dropout Voltage	$V_I min - V_O$	I_O = 60 mA*		—	85	150	mV
		I_O = 125 mA*		—	190	300	mV
Quiescent Current	I_Q	V_I = 6 V, $1\ mA \le I_O \le 100$ mA*		—	45	60	µA
(GND terminal current)		V_I = 8 V, $1\ mA \le I_O \le 100$ mA*		—	50	65	µA
Power Supply Rejection Ratio	PSRR	V_I = 4.5V, V_i = 100 mV @ 400 Hz, I_O = 10 mA		—	-45	—	dB
Output Noise Voltage	V_n	f = 10 Hz to 100 kHz, I_O = 10 mA: C_O = 0		—	1.0	—	µV/Hz
		C_O = 10 µF		—	2.0	—	µV/Hz
Thermal Shutdown Temp.	T_J			150	—	—	°C
Thermal Resistance	$R_{\theta JA}$	Mounted on 2.24" x 2.24" solder-coated copper-clad board in still air		—	258	—	°C/W

Typical values are at T_A = +25°C and are given for circuit design information only.
* Pulse test (≤20 ms). See previous page for duty cycle limitations.

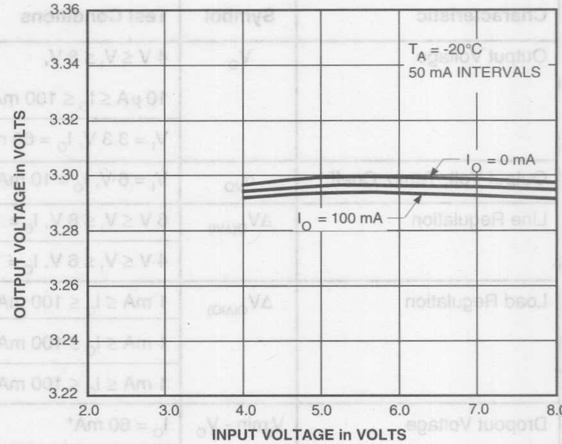
TYPICAL CHARACTERISTICS

LOAD REGULATION

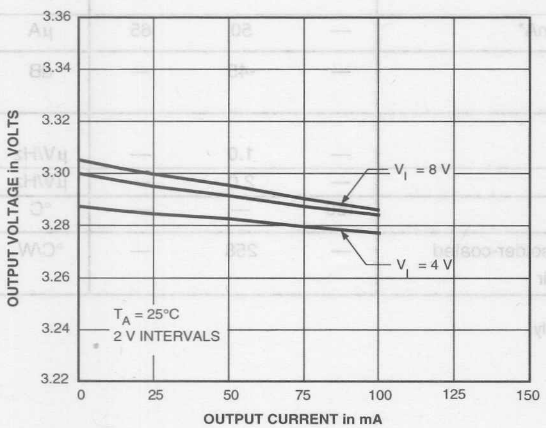


Dwg. GP-052-6

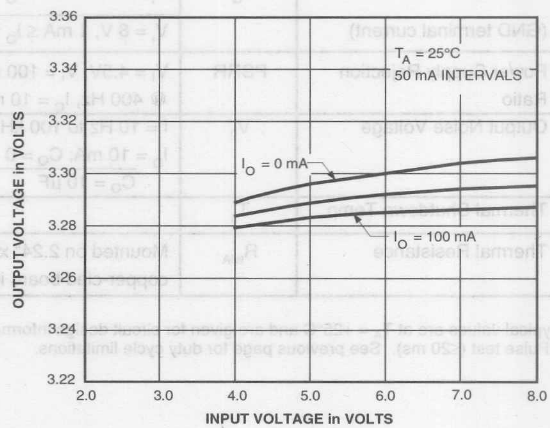
LINE REGULATION



Dwg. GP-053-6



Dwg. GP-052-7

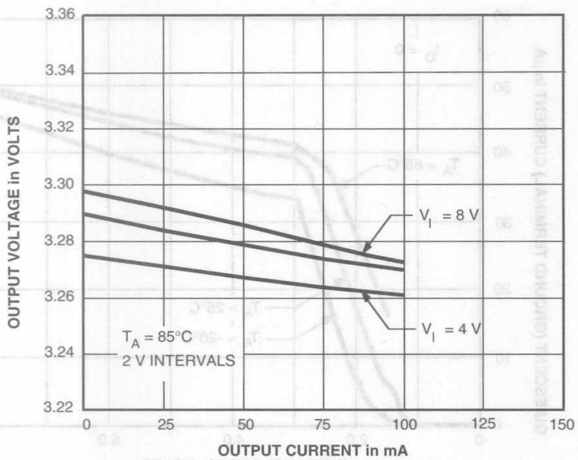


Dwg. GP-053-7

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

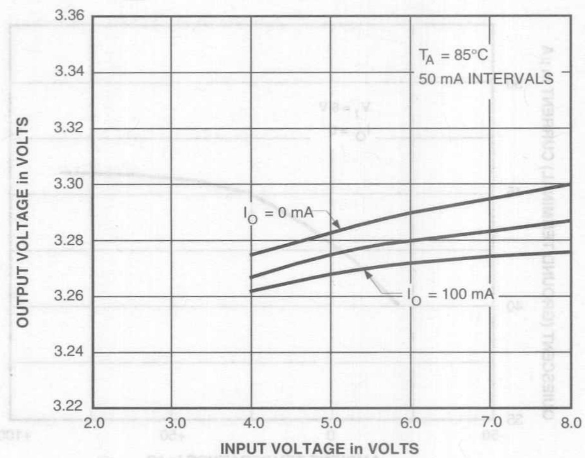
TYPICAL CHARACTERISTICS (cont'd)

LOAD REGULATION



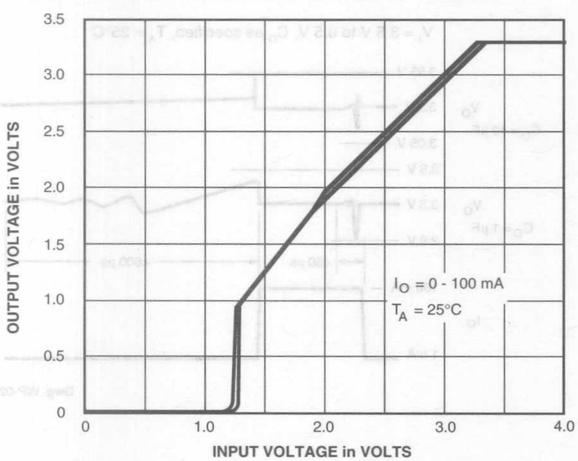
Dwg. GP-052-8

LINE REGULATION

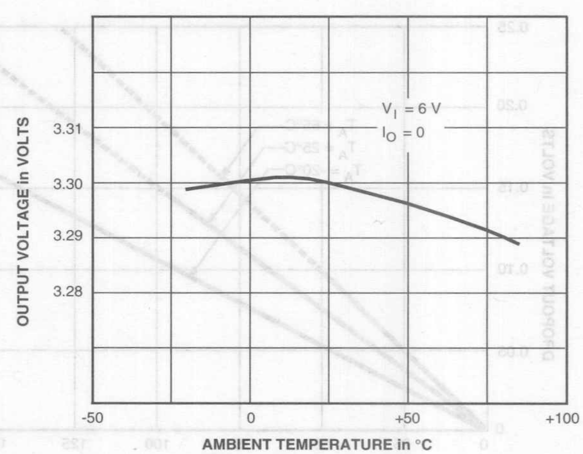


Dwg. GP-053-8

OUTPUT VOLTAGE



Dwg. GP-059-1

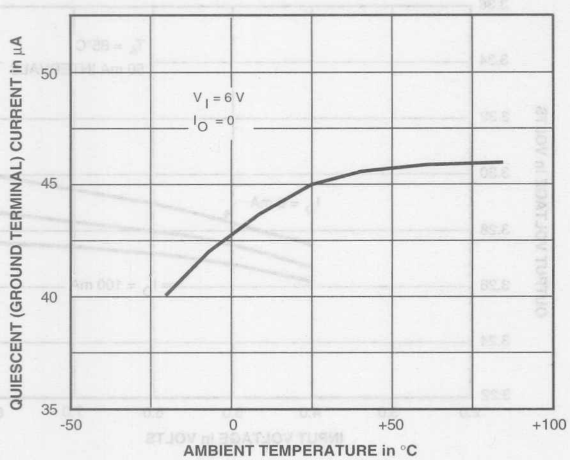


Dwg. GP-050-2

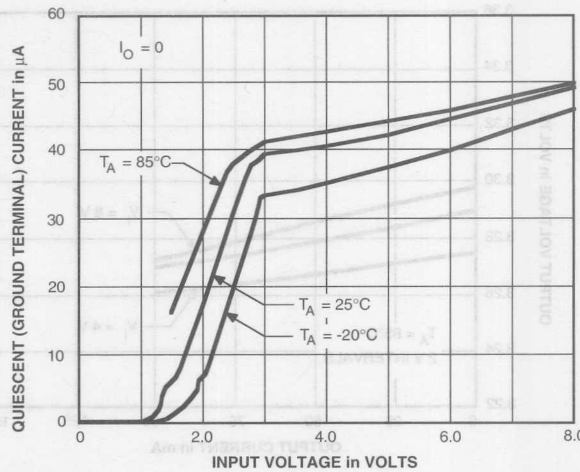
CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

TYPICAL CHARACTERISTICS (concluded)

QUIESCENT (GROUND TERMINAL) CURRENT

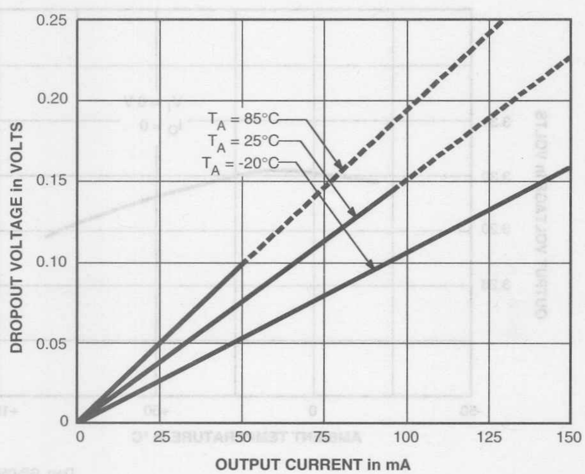


Dwg. GP-051-2



Dwg. GP-058

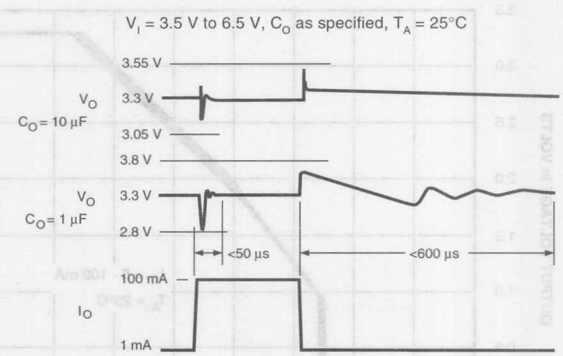
DROPOUT VOLTAGE



Dwg. GP-054-1

CAUTION: Maximum allowable duty cycle will be significantly less than 100% at high temperatures, at high input voltages, or at high output currents. See Maximum Allowable Output Current table.

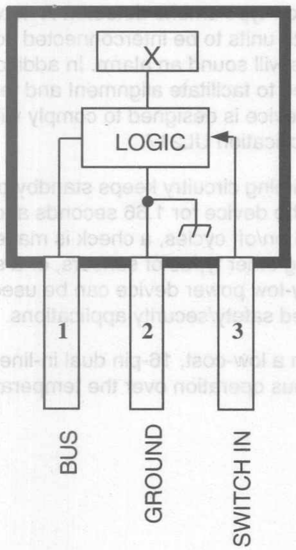
LOAD TRANSIENT PERFORMANCE



Dwg. WP-028-1

SECTION 7. TECHNICAL DATA FOR SAFETY & SECURITY ICs

MULTIPLEXED TWO-WIRE HALL-EFFECT SENSOR ICs



Dwg. PH-005

Pinning is shown viewed from branded side.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{BUS} . . . . **18 V**
Magnetic Flux Density, B . . . . . . **Unlimited**
Operating Temperature Range, T_A
A3054KU . . . . **-40°C to +125°C**
A3054SU . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . **-55°C to +150°C**
Package Power Dissipation,
P_D . . . . **635 mW**

The A3054KU and A3054SU Hall-effect sensors are digital magnetic sensing ICs capable of communicating over a two-wire power/signal bus. Using a sequential addressing scheme, the device responds to a signal on the bus and returns the diagnostic status of the IC, as well as the status of each monitored external magnetic field. As many as 30 sensors can function on the same two-wire bus. This IC is ideal for multiple sensor applications where minimizing the wiring harness size is desirable or essential.

Each device consists of high-resolution bipolar Hall-effect switching circuitry, the output of which drives high-density CMOS logic stages. The logic stages decode the address pulse and enable a response at the appropriate address. The combination of magnetic-field or switch-status sensing, low-noise amplification of the Hall-transducer output, and high-density decoding and control logic is made possible by the development of a new sensor DABiC™ (digital analog bipolar CMOS) fabrication technology.

Complete, detailed technical information on the A3054KU and A3054SU is shown in Section 4.

FEATURES

- Complete Multiplexed Hall-Effect ICs with Simple Sequential Addressing Protocol
- Allows Power and Communication Over a Two-Wire Bus (Supply/Signal and Ground)
- Up to 30 Hall-Effect Sensors Can Share a Bus
- Sensor Diagnostic Capabilities
- Magnetic-Field or Switch-Status Sensing
- Low Power of DABiC Technology Favors Battery-Powered and Mobile Applications
- Ideal for Automotive, Consumer, and Industrial Applications

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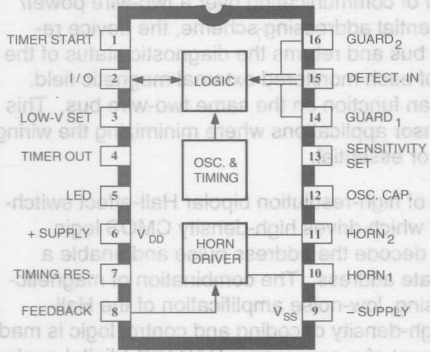
SMOKE DETECTOR WITH INTERCONNECT AND TIMER



Dwg. PC-004

Dwg. PC-004

The A5347CA is a low-current, CMOS circuit providing all of the required features for an ionization-type smoke detector. A networking capability allows as many as 125 units to be interconnected so that if any unit senses smoke, all units will sound an alarm. In addition, special features are incorporated to facilitate alignment and test of the finished smoke detector. This device is designed to comply with Underwriters Laboratories Specification UL217.

The internal oscillator and timing circuitry keeps standby power to a minimum by powering down the device for 1.66 seconds and sensing smoke for only 10 ms. Every 24 on/off cycles, a check is made for low battery condition. By substituting other types of sensors, or a switch for the ionization detector, this very-low power device can be used in numerous other battery-operated safety/security applications.

The A5347CA is supplied in a low-cost, 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of 0°C to +50°C.

FEATURES

- Interconnect Up to 125 Detectors
- Piezoelectric Horn Driver
- Guard Outputs for Detector Input
- Pulse Testing for Low Battery
- Power-ON Reset
- Internal Timer & Control for Reduced Sensitivity
- Built-In Hysteresis Reduces False Triggering

ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to V_{SS})

Supply Voltage Range,
V_{DD} .... **-0.5 V to +15 V**

Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**

Input Current, I_{IN} .... **10 mA**

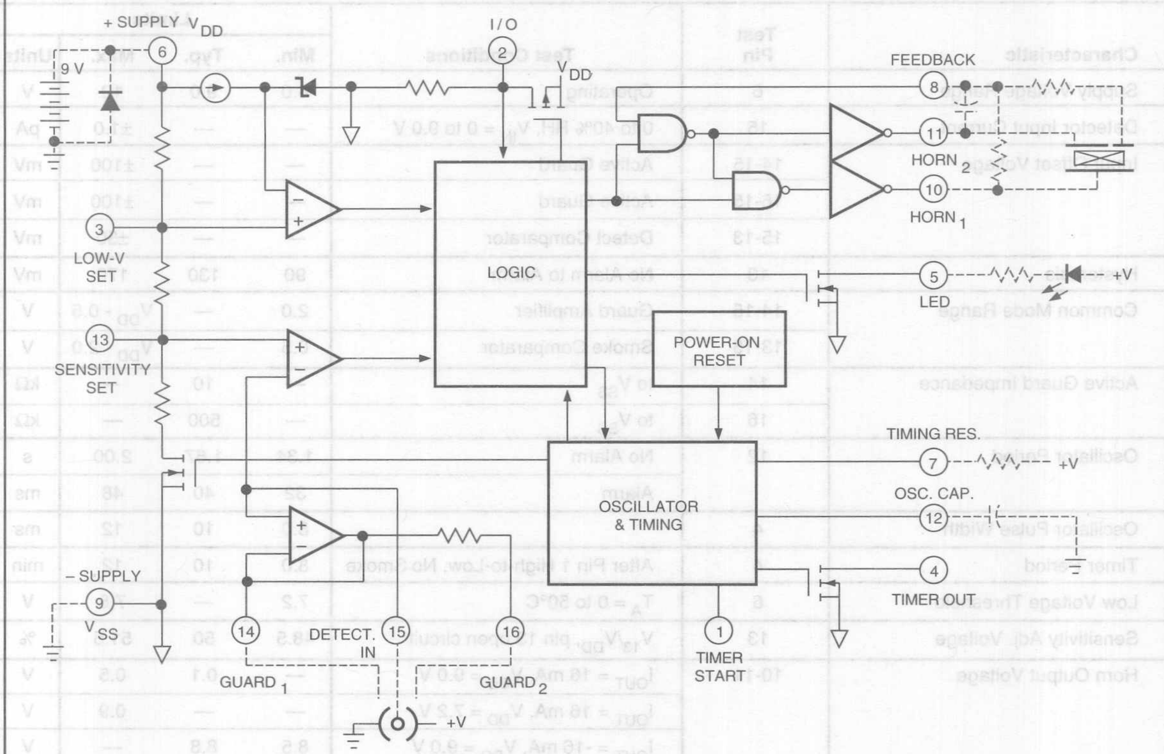
Operating Temperature Range,
T_A .... **0°C to +50°C**

Storage Temperature Range,
T_S .... **-55°C to +125°C**

CAUTION: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number: **A5347CA**.

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATION



Dwg. FC-001-2A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 9.0 V, V_{SS} = 0 V, C_{12} = 0.1 μF, R_7 = 8.2 MΩ (unless otherwise noted).

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	6	Operating	6.0	9.0	12	V
Detector Input Current	15	0 to 40% RH, V_{IN} = 0 to 9.0 V	—	—	±1.0	pA
Input Offset Voltage	14-15	Active Guard	—	—	±100	mV
	16-15	Active Guard	—	—	±100	mV
	15-13	Detect Comparator	—	—	±50	mV
Hysteresis	13	No Alarm to Alarm	90	130	170	mV
Common Mode Range	14-15	Guard Amplifier	2.0	—	V_{DD} - 0.5	V
	13-15	Smoke Comparator	0.5	—	V_{DD} - 2.0	V
Active Guard Impedance	14	to V_{SS}	—	10	—	kΩ
	16	to V_{SS}	—	500	—	kΩ
Oscillator Period	12	No Alarm	1.34	1.67	2.00	s
		Alarm	32	40	48	ms
Oscillator Pulse Width	4		8.0	10	12	ms
Timer Period	4	After Pin 1 High-to-Low, No Smoke	8.0	10	12	min
Low Voltage Threshold	6	T_A = 0 to 50°C	7.2	—	7.8	V
Sensitivity Adj. Voltage	13	V_{13}/V_{DD}, pin 13 open circuit	48.5	50	51.5	%
Horn Output Voltage	10-11	I_{OUT} = 16 mA, V_{DD} = 9.0 V	—	0.1	0.5	V
		I_{OUT} = 16 mA, V_{DD} = 7.2 V	—	—	0.9	V
		I_{OUT} = -16 mA, V_{DD} = 9.0 V	8.5	8.8	—	V
		I_{OUT} = -16 mA, V_{DD} = 7.2 V	6.3	—	—	V
Horn Output ON Time	10-11	Alarm	120	160	208	ms
		Low Battery	8.0	10	12	ms
Horn Output OFF Time	10-11	Alarm	60	80	104	ms
		Low Battery	32	40	48	s
Timer Start Logic Levels	1	V_{IH}	3.5	—	—	V
		V_{IL}	—	—	1.5	V
Timer Start Input Current	1	V_{IN} = 9.0 V	20	—	80	μA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.

Continued next page . . .

NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
Timer Out Output Current	4	V_{OUT} = 0.5 V	500	—	—	µA
LED Output ON Current	5	V_{DD} = 7.2 V, V_{OUT} = 1.0 V	10	—	—	mA
LED Output ON Time	5		8.0	10	12	ms
LED Output OFF Time	5	No Alarm, In Standby	32	40	48	s
		No Alarm, Timer Mode After Pin 1 High-to-Low	8.0	10	12	s
I/O Current	2	No Alarm, $V_{I/O} = V_{DD}$ - 2.0 V	25	—	60	µA
		Alarm, $V_{I/O} = V_{DD}$ - 2.0 V	-7.5			mA
I/O Alarm Voltage	2	External "Alarm" In	3.0	—	—	V
I/O Delay	2	"Alarm" Out	—	3.0	—	s
Supply Current	6	V_{DD} = 9.0 V, No Alarm, No Loads	—	5.0	9.0	µA
		V_{DD} = 12 V, No Alarm, No Loads	—		12	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.

NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

CIRCUIT DESCRIPTION

The A5347CA is a low-current CMOS circuit providing all of the required features for an ionization-type smoke detector.

Oscillator. An internal oscillator operates with a period of 1.67 seconds during no-smoke conditions. Every 1.67 seconds, internal power is applied to the entire circuit and a check is made for smoke. Every 24 clock cycles (40 seconds), the LED is pulsed and a check is made for low battery by comparing V_{DD} to an internal reference. Since very-low currents are used in the device, the oscillator capacitor at pin 12 should be a low-leakage type (PTFE, polystyrene, or polypropylene).

Detector Circuitry. When smoke is detected, the resistor divider network that sets the sensitivity (smoke trip point) is altered to increase the sensitivity set voltage (pin 13) by typically 130 mV with no external connections to pins 3 or 13. This provides hysteresis and reduces false triggering. An active guard is provided on both pins adjacent to the detector input (pin 15). The voltage at pins 14 and 16 will be within 100 mV of the input. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard amplifier is not power strobed and thus provides constant protection from surface leakage currents. The detector input has internal diode protection against static damage.

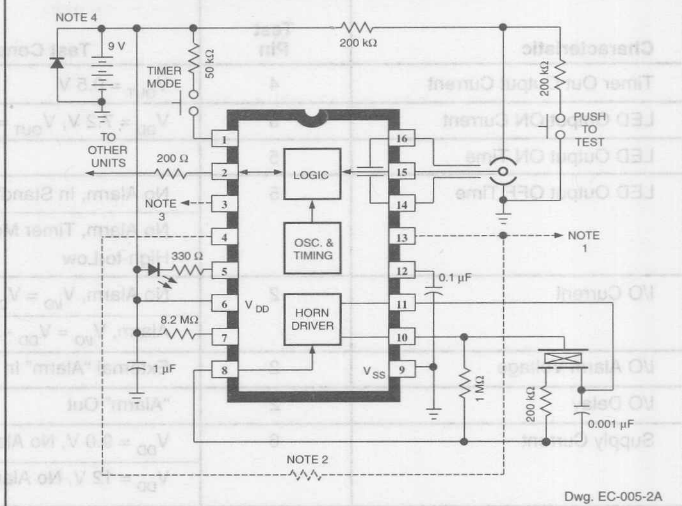
Alarm Circuitry. If smoke is detected, the oscillator period changes to 40 ms and the horn is enabled. The horn output is typically 160 ms ON, 80 ms OFF. During the OFF time, smoke is again checked and will inhibit further alarm output if smoke is not sensed. During smoke conditions the low battery alarm is inhibited and the LED is driven at a 1 Hz rate.

Sensitivity Adjust. The detector sensitivity to smoke is set internally by a voltage divider connected between V_{DD} and V_{SS}. The sensitivity can be externally adjusted to the individual characteristics of the ionization chamber by connecting a resistor between pin 13 and V_{DD}, or between pin 13 and V_{SS}.

Low Battery. The low battery threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The threshold can be increased by connecting a resistor between pin 3 and V_{DD}. The threshold can be decreased by connecting a resistor between pin 3 and V_{SS}. The battery voltage level is checked every 40 seconds during the 10 mA, 10 ms LED pulse. If an LED is not used, it should be replaced with an equivalent resistor (typically 500 Ω to 1000 Ω) such that the battery loading remains at 10 mA.

Timer. An internal timer is provided that can be used in various configurations to allow for a period of reduced smoke detector sensitivity ("hush"). When a high-to-low transition occurs at pin 1, the internal timer is reset, the timer mode enabled, and the circuit reset to a no alarm condition. The LED will flash at a 10 second rate. If the level of smoke is increased such that the reduced sensitivity level is reached, the device will go into the alarm condition. The timer, however, will continue to completion of the nominal 10-1/4 minute period (368 clock cycles). If the timer mode is not used, pin 1 should be tied low.

TYPICAL APPLICATION



NOTE 1: Use an external resistor to adjust sensitivity for a particular smoke chamber.

NOTE 2: Select resistor to reduce sensitivity during timer mode.

NOTE 3: A resistor to ground or V_{DD} may be added to this pin to modify low battery voltage threshold.

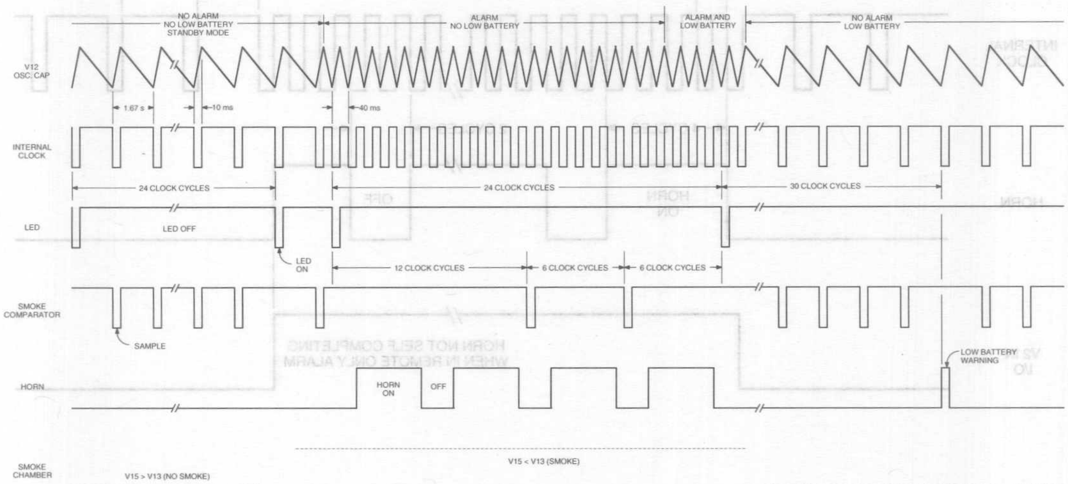
NOTE 4: Reverse battery protection must be supplied externally.

I/O. A connection is provided at pin 2 to allow multiple smoke detectors to be commoned. If any single unit detects smoke (I/O is driven high), all connected units will sound their associated horns after a nominal 3 second delay. The LED is suppressed when an alarm is signaled from an interconnected unit.

Testing. On power up, all internal counters are reset. Internal test circuitry allows for low battery check by holding pins 8 and 12 low during power up, then reducing V_{DD} and monitoring $HORN_1$ (pin 10). All functional tests can be accelerated by driving pin 12 with a 2 kHz square wave. The 10 ms strobe period must be maintained for proper operation of the comparator circuitry.

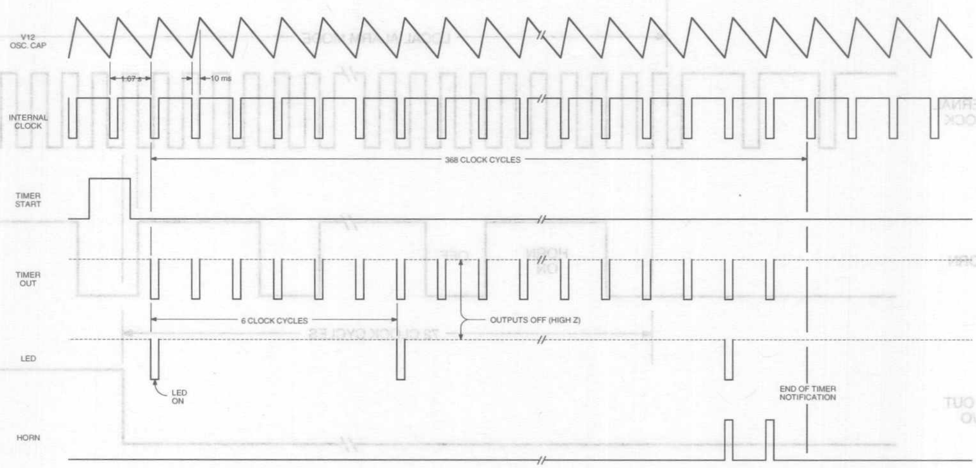
TIMING DIAGRAMS IN TYPICAL APPLICATION

NON-TIMER MODE



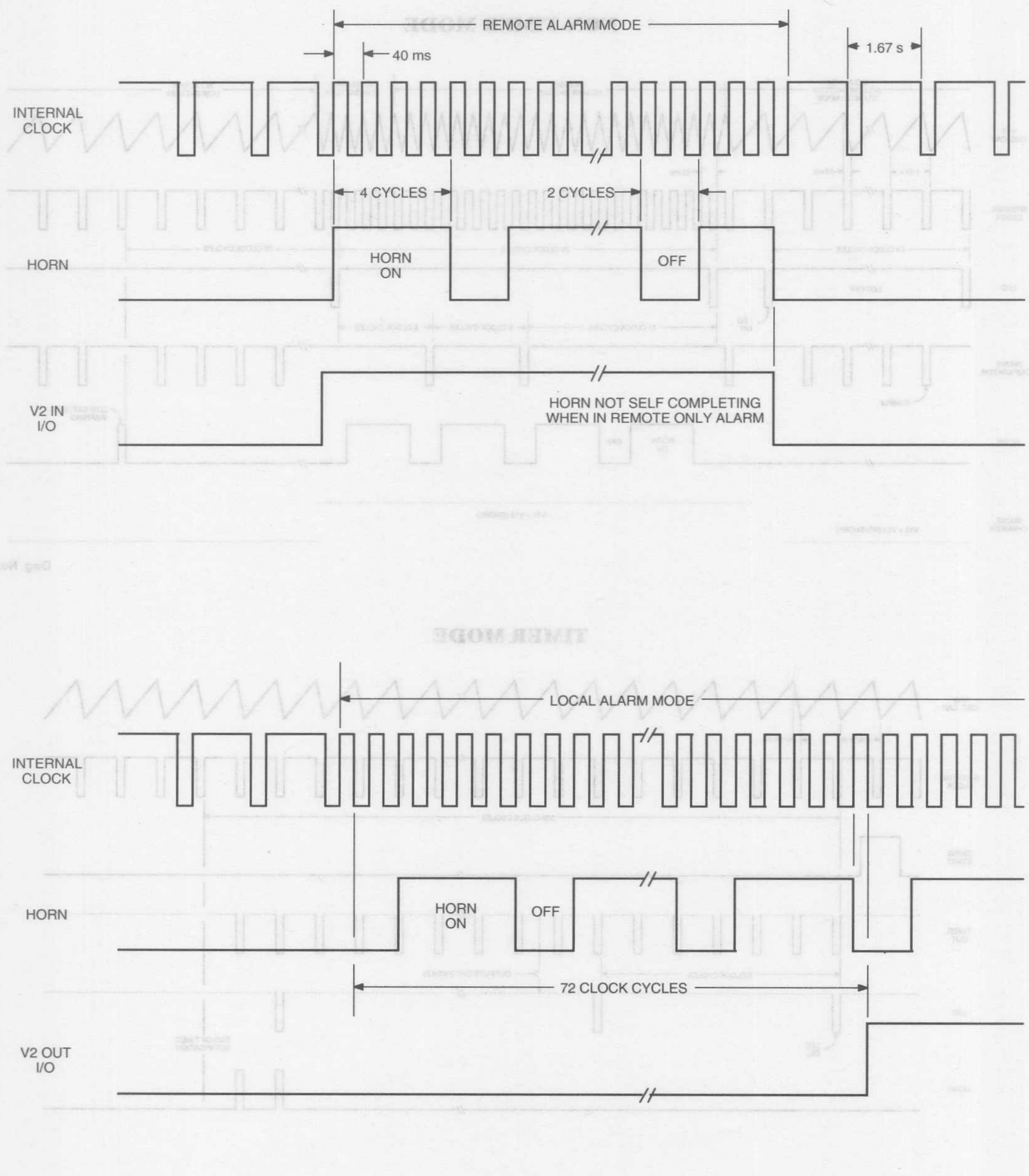
Dwg. No. WC-003

TIMER MODE



Dwg. No. WC-005

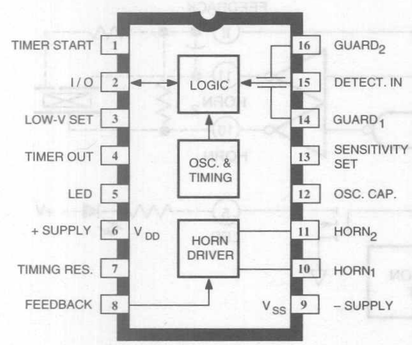
I/O OPERATION



Dwg. No. WC-004

5348

SMOKE DETECTOR WITH INTERCONNECT AND TIMER



Dwg. PC-004

Dwg. No. PC-004

The A5348CA is a low-current, CMOS circuit providing all of the required features for an ionization-type smoke detector. A networking capability allows as many as 125 units to be interconnected so that if any unit senses smoke, all units will sound an alarm. In addition, special features are incorporated to facilitate alignment and test of the finished smoke detector. This device is designed to comply with Underwriters Laboratories Specification UL217.

The internal oscillator and timing circuitry keeps standby power to a minimum by powering down the device for 1.66 seconds and sensing smoke for only 10 ms. Every 24 on/off cycles, a check is made for low battery condition. By substituting other types of sensors, or a switch for the ionization detector, this very-low power device can be used in numerous other battery-operated safety/security applications.

The A5348CA is supplied in a low-cost, 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of 0°C to +50°C.

ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to V_{SS})

Supply Voltage Range,
V_{DD} .... **-0.5 V to +15 V**
Reverse Battery (10.5 V) .... **20 s**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Input Current, I_{IN} .... **10 mA**
Operating Temperature Range,
T_A .... **0°C to +50°C**
Storage Temperature Range,
T_S .... **-55°C to +125°C**

CAUTION: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

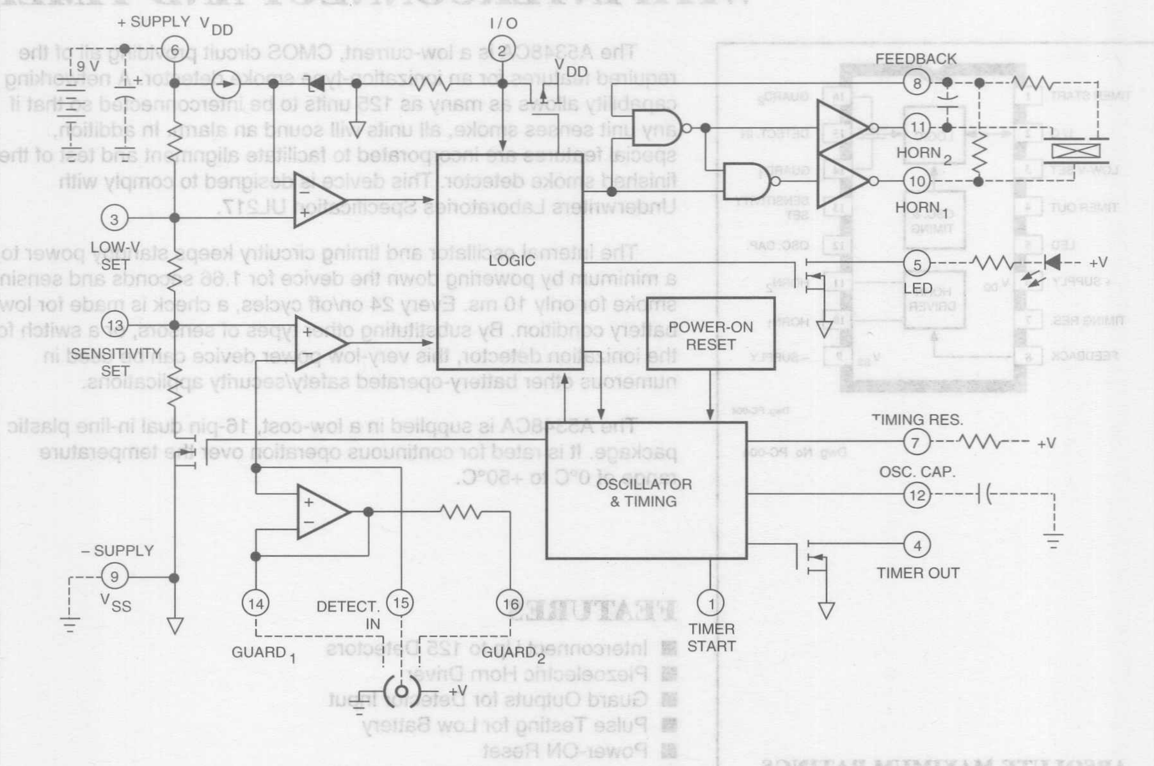
FEATURES

- Interconnect Up to 125 Detectors
- Piezoelectric Horn Driver
- Guard Outputs for Detector Input
- Pulse Testing for Low Battery
- Power-ON Reset
- Internal Reverse Battery Protection
- Internal Timer & Control for Reduced Sensitivity
- Built-In Hysteresis Reduces False Triggering

Always order by complete part number: **A5348CA** .

5348
SMOKE DETECTOR WITH INTERCONNECT AND TIMER

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATION



Dwg. No. FC-001B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 9.0 V, V_{SS} = 0 V, C_{12} = 0.1 μF, R_7 = 8.2 MΩ (unless otherwise noted).

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	6	Operating	6.0	9.0	12	V
Detector Input Current	15	0 to 40% RH, V_{IN} = 0 to 9.0 V	—	—	±1.0	pA
Input Offset Voltage	14-15	Active Guard	—	—	±100	mV
	16-15	Active Guard	—	—	±100	mV
	15-13	Detect Comparator	—	—	±50	mV
Hysteresis	13	No Alarm to Alarm	90	130	170	mV
Common Mode Range	14-15	Guard Amplifier	2.0	—	V_{DD} - 0.5	V
	13-15	Smoke Comparator	0.5	—	V_{DD} - 2.0	V
Active Guard Impedance	14	to V_{SS}	—	10	—	kΩ
	16	to V_{SS}	—	500	—	kΩ
Oscillator Period	12	No Alarm	1.34	1.67	2.00	s
		Alarm	32	40	48	ms
Oscillator Pulse Width	4		8.0	10	12	ms
Timer Period	4	After Pin 1 High-to-Low, No Smoke	8.0	10	12	min
Low Voltage Threshold	6	T_A = 0 to 50°C	7.2	—	7.8	V
Sensitivity Adj. Voltage	13	V_{13}/V_{DD}, pin 13 open circuit	48.5	50	51.5	%
Horn Output Voltage	10-11	I_{OUT} = 16 mA, V_{DD} = 9.0 V	—	0.1	0.5	V
		I_{OUT} = 16 mA, V_{DD} = 7.2 V	—	—	0.9	V
		I_{OUT} = -16 mA, V_{DD} = 9.0 V	8.5	8.8	—	V
		I_{OUT} = -16 mA, V_{DD} = 7.2 V	6.3	—	—	V
Horn Output ON Time	10-11	Alarm	120	160	208	ms
		Low Battery	8.0	10	12	ms
Horn Output OFF Time	10-11	Alarm	60	80	104	ms
		Low Battery	32	40	48	s
Timer Start Logic Levels	1	V_{IH}	3.5	—	—	V
		V_{IL}	—	—	1.5	V
Timer Start Input Current	1	V_{IN} = 9.0 V	20	—	80	μA

Continued next page . . .

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.
NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
Timer Out Output Current	4	V_{OUT} = 0.5 V	500	—	—	µA
LED Output ON Current	5	V_{DD} = 7.2 V, V_{OUT} = 1.0 V	10	—	—	mA
LED Output ON Time	5		8.0	10	12	ms
LED Output OFF Time	5	No Alarm, In Standby	32	40	48	s
		No Alarm, Timer Mode After Pin 1 High-to-Low	8.0	10	12	s
I/O Current	2	No Alarm, $V_{I/O}$ = V_{DD} - 2.0 V	25	—	60	µA
		Alarm, $V_{I/O}$ = V_{DD} - 2.0 V	-7.5			mA
I/O Alarm Voltage	2	External "Alarm" In	3.0	—	—	V
I/O Delay	2	"Alarm" Out	—	3.0	—	s
Supply Current	6	V_{DD} = 9.0 V, No Alarm, No Loads	—	5.0	9.0	µA
		V_{DD} = 12 V, No Alarm, No Loads	—	—	12	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.
NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

CIRCUIT DESCRIPTION

The A5348CA is a low-current CMOS circuit providing all of the required features for an ionization-type smoke detector.

Oscillator. An internal oscillator operates with a period of 1.67 seconds during no-smoke conditions. Every 1.67 seconds, internal power is applied to the entire circuit and a check is made for smoke. Every 24 clock cycles
(40 seconds), the LED is pulsed and a check is made for low battery by comparing V_{DD} to an internal reference.
Since very-low currents are used in the device, the oscillator capacitor at pin 12 should be a low-leakage type
(PTFE, polystyrene, or polypropylene).

Detector Circuitry. When smoke is detected, the resistor divider network that sets the sensitivity (smoke trip point) is altered to increase the sensitivity set voltage (pin 13) by typically 130 mV with no external connections to pins 3 or 13. This provides hysteresis and reduces false triggering. An active guard is provided on both pins adjacent to the detector input (pin 15). The voltage at pins 14 and 16 will be within 100 mV of the input. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard amplifier is not power strobed and thus provides constant protection from surface leakage currents. The detector input has internal diode protection against static damage.

Alarm Circuitry. If smoke is detected, the oscillator period changes to 40 ms and the horn is enabled. The horn output is typically 160 ms ON, 80 ms OFF. During the OFF time, smoke is again checked and will inhibit further alarm output if smoke is not sensed. During smoke conditions the low battery alarm is inhibited and the LED is driven at a 1 Hz rate.

Sensitivity Adjust. The detector sensitivity to smoke is set internally by a voltage divider connected between V_{DD} and V_{SS}. The sensitivity can be externally adjusted to the individual characteristics of the ionization chamber by connecting a resistor between pin 13 and V_{DD}, or between pin 13 and V_{SS}.

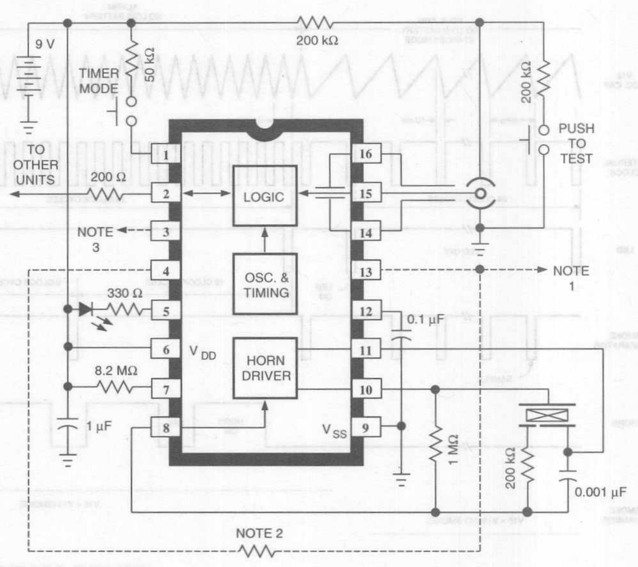
Low Battery. The low battery threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The threshold can be increased by connecting a resistor between pin 3 and V_{DD}. The threshold can be decreased by connecting a resistor between pin 3 and V_{SS}. The battery voltage level is checked every 40 seconds during the 10 mA, 10 ms LED pulse. If an LED is not used, it should be replaced with an equivalent resistor (typically 500 Ω to 1000 Ω) such that the battery loading remains at 10 mA.

Timer. An internal timer is provided that can be used in various configurations to allow for a period of reduced smoke detector sensitivity ("hush"). When a high-to-low transition occurs at pin 1, the internal timer is reset, the timer mode enabled, and the circuit reset to a no alarm condition. The LED will flash at a 10 second rate. If the level of smoke is increased such that the reduced sensitivity level is reached, the device will go into the alarm condition. The timer, however, will continue to completion of the nominal 10-1/4 minute period (368 clock cycles). If the timer mode is not used, pin 1 should be tied low.

I/O. A connection is provided at pin 2 to allow multiple smoke detectors to be commoned. If any single unit detects smoke (I/O is driven high), all connected units will sound their associated horns after a nominal 3 second delay. The LED is suppressed when an alarm is signaled from an interconnected unit.

Testing. On power up, all internal counters are reset. Internal test circuitry allows for low battery check by holding pins 8 and 12 low during power up, then reducing V_{DD} and monitoring $HORN_1$ (pin 10). All functional tests can be accelerated by driving pin 12 with a 2 kHz square wave. The 10 ms strobe period must be maintained for proper operation of the comparator circuitry.

TYPICAL APPLICATION



Dwg. EC-005A

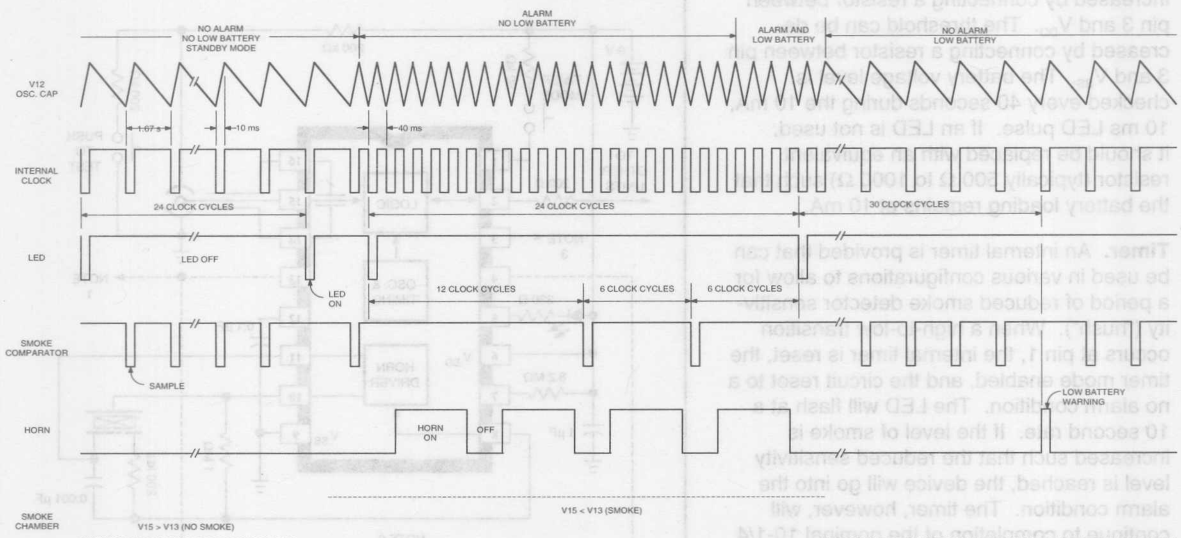
NOTE 1: Use an external resistor to adjust sensitivity for a particular smoke chamber.

NOTE 2: Select resistor to reduce sensitivity during timer mode.

NOTE 3: A resistor to ground or V_{DD} may be added to this pin to modify low battery voltage threshold.

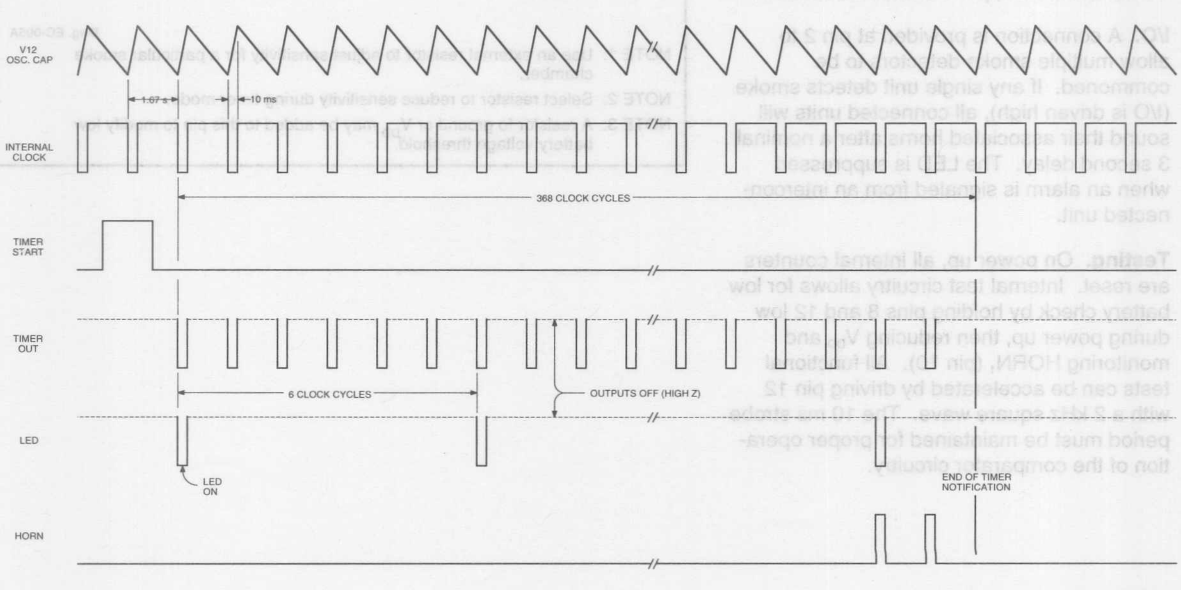
TIMING DIAGRAMS IN TYPICAL APPLICATION

NON-TIMER MODE



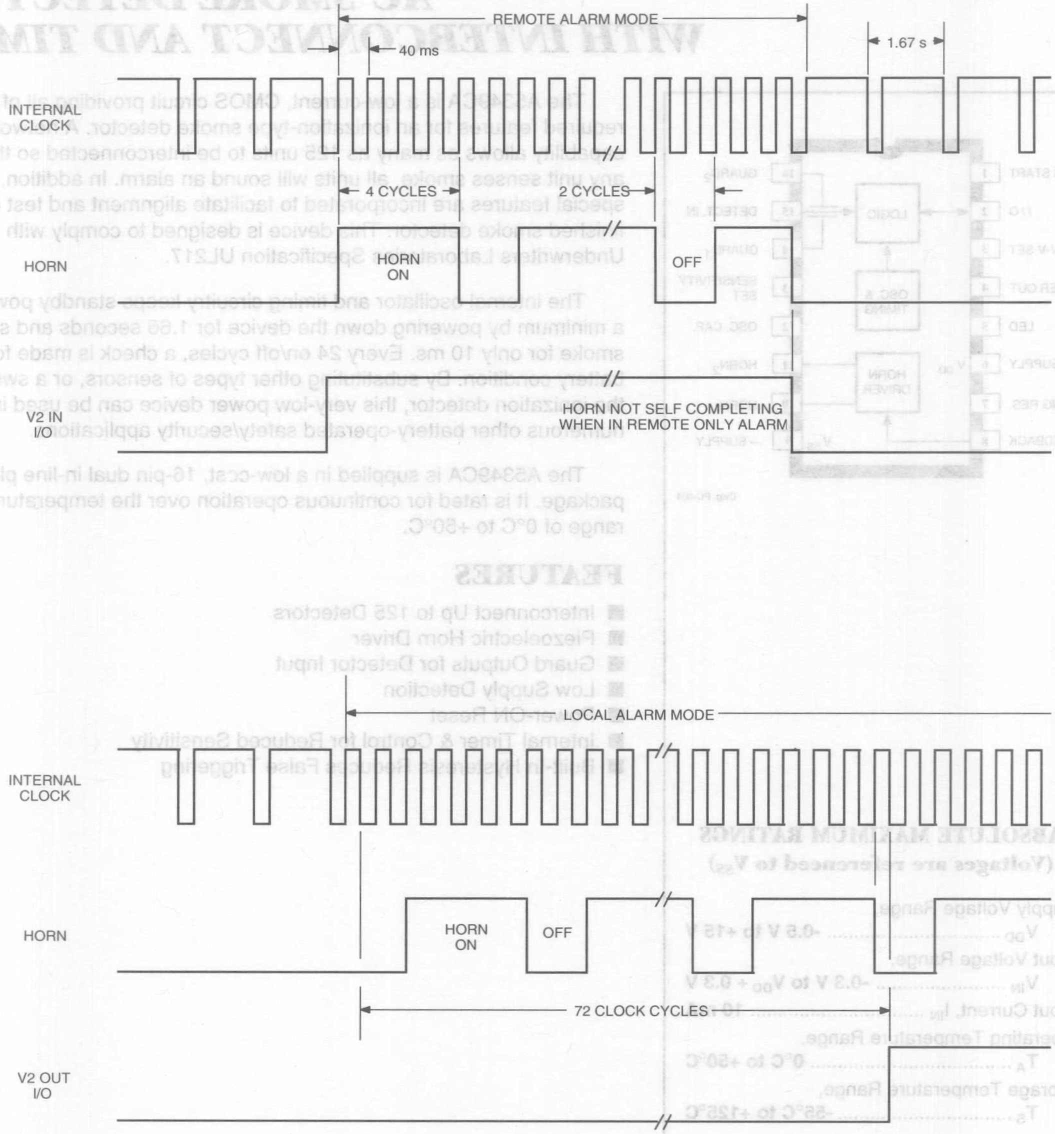
Dwg. No. WC-003

TIMER MODE



Dwg. No. WC-005

I/O OPERATION

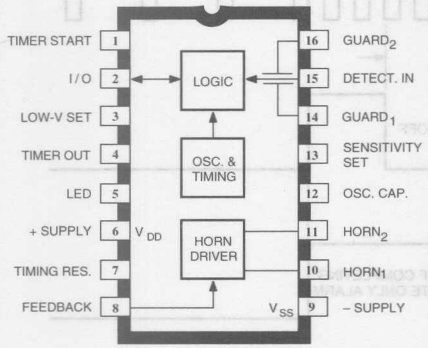


Dwg. No. WC-004

5349

26110.4

AC SMOKE DETECTOR WITH INTERCONNECT AND TIMER



Dwg. PC-004

The A5349CA is a low-current, CMOS circuit providing all of the required features for an ionization-type smoke detector. A networking capability allows as many as 125 units to be interconnected so that if any unit senses smoke, all units will sound an alarm. In addition, special features are incorporated to facilitate alignment and test of the finished smoke detector. This device is designed to comply with Underwriters Laboratories Specification UL217.

The internal oscillator and timing circuitry keeps standby power to a minimum by powering down the device for 1.66 seconds and sensing smoke for only 10 ms. Every 24 on/off cycles, a check is made for low battery condition. By substituting other types of sensors, or a switch for the ionization detector, this very-low power device can be used in numerous other battery-operated safety/security applications.

The A5349CA is supplied in a low-cost, 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of 0°C to +50°C.

FEATURES

- Interconnect Up to 125 Detectors
- Piezoelectric Horn Driver
- Guard Outputs for Detector Input
- Low Supply Detection
- Power-ON Reset
- Internal Timer & Control for Reduced Sensitivity
- Built-In Hysteresis Reduces False Triggering

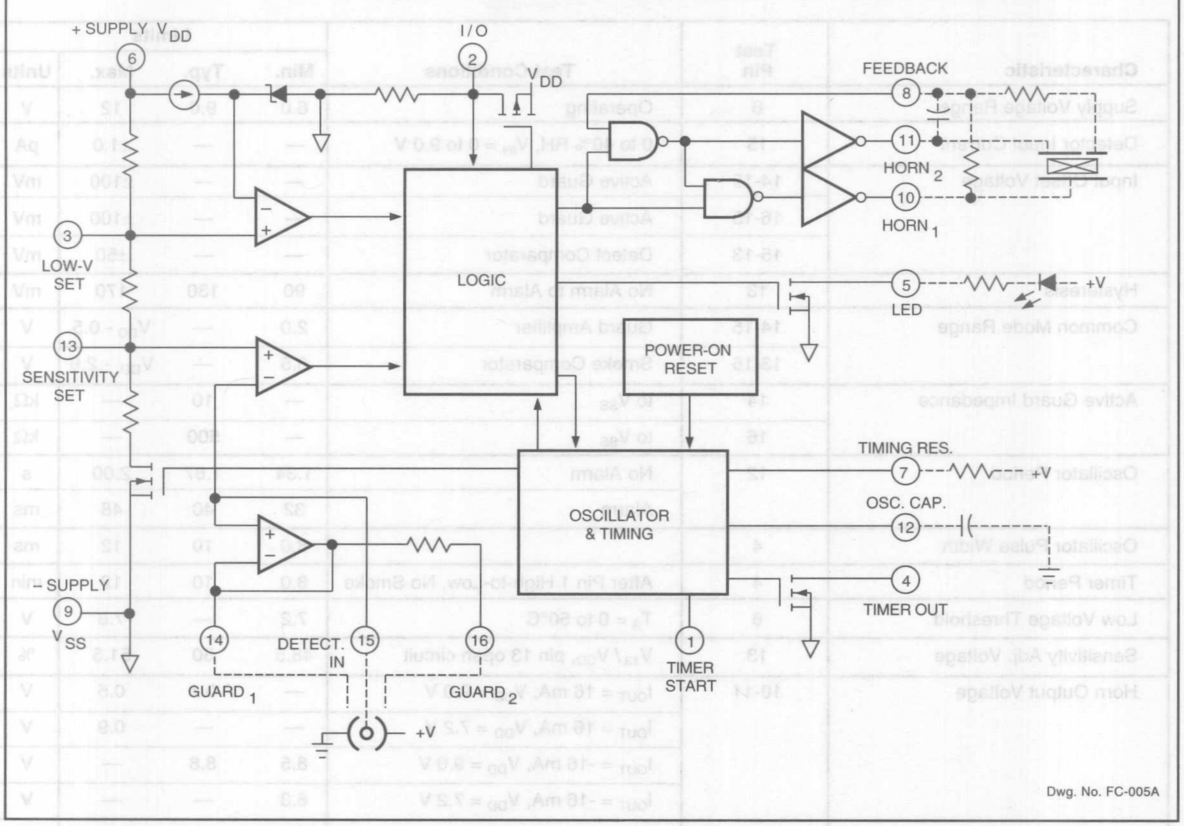
ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to V_{SS})

Supply Voltage Range,
V_{DD} .... **-0.5 V to +15 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Input Current, I_{IN} .... **10 mA**
Operating Temperature Range,
T_A .... **0°C to +50°C**
Storage Temperature Range,
T_S .... **-55°C to +125°C**

CAUTION: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Always order by complete part number: **A5349CA**.

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 9.0 V, V_{SS} = 0 V, C_{12} = 0.1 μF, R_7 = 8.2 MΩ (unless otherwise noted).

Characteristic	Test Pin	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	6	Operating	6.0	9.0	12	V
Detector Input Current	15	0 to 40% RH, V_{IN} = 0 to 9.0 V	—	—	±1.0	pA
Input Offset Voltage	14-15	Active Guard	—	—	±100	mV
	16-15	Active Guard	—	—	±100	mV
	15-13	Detect Comparator	—	—	±50	mV
Hysteresis	13	No Alarm to Alarm	90	130	170	mV
Common Mode Range	14-15	Guard Amplifier	2.0	—	V_{DD} - 0.5	V
	13-15	Smoke Comparator	0.5	—	V_{DD} - 2.0	V
Active Guard Impedance	14	to V_{SS}	—	10	—	kΩ
	16	to V_{SS}	—	500	—	kΩ
Oscillator Period	12	No Alarm	1.34	1.67	2.00	s
		Alarm	32	40	48	ms
Oscillator Pulse Width	4		8.0	10	12	ms
Timer Period	4	After Pin 1 High-to-Low, No Smoke	8.0	10	12	min
Low Voltage Threshold	6	T_A = 0 to 50°C	7.2	—	7.8	V
Sensitivity Adj. Voltage	13	V_{13} / V_{DD}, pin 13 open circuit	48.5	50	51.5	%
Horn Output Voltage	10-11	I_{OUT} = 16 mA, V_{DD} = 9.0 V	—	0.1	0.5	V
		I_{OUT} = 16 mA, V_{DD} = 7.2 V	—	—	0.9	V
		I_{OUT} = -16 mA, V_{DD} = 9.0 V	8.5	8.8	—	V
		I_{OUT} = -16 mA, V_{DD} = 7.2 V	6.3	—	—	V
Horn Output ON Time	10-11	Alarm	120	160	208	ms
		Low Battery	8.0	10	12	ms
Horn Output OFF Time	10-11	Alarm	60	80	104	ms
		Low Battery	32	40	48	s
Timer Start Logic Levels	1	V_{IH}	3.5	—	—	V
		V_{IL}	—	—	1.5	V
Timer Start Input Current	1	V_{IN} = 9.0 V	20	—	80	μA
Timer Out Output Current	4	V_{OUT} = 0.5 V	500	—	—	μA

Continued next page . . .

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.
NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

ELECTRICAL CHARACTERISTICS continued

Characteristic	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
LED Output ON Current	5	V_{DD} = 7.2 V, V_{OUT} = 1.0 V	10	—	—	mA
LED Output ON Time	5	Local Alarm		constant OFF		
		Timer Mode, No Alarm		8.35		s
LED Output OFF Time	5	No Alarm, In Standby		constant ON		s
		No Alarm, Timer Mode After Pin 1 High-to-Low		1.67		s
I/O Current	2	No Alarm, $V_{I/O} = V_{DD} - 2.0$ V	25	—	60	µA
		Alarm, $V_{I/O} = V_{DD} - 2.0$ V	-7.5	—	—	mA
I/O Alarm Voltage	2	External "Alarm" In	3.0			V
I/O Delay	2	"Alarm" Out		3.0		s
Supply Current	6	V_{DD} = 9.0 V, No Alarm, No Loads		5.0	9.0	µA
		V_{DD} = 12 V, No Alarm, No Loads	—	—	12	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.
NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} < V_{13}$; No Alarm (No Smoke) Condition as $V_{15} > V_{13}$.

CIRCUIT DESCRIPTION

The A5349CA is a low-current CMOS circuit providing all of the required features for an ionization-type smoke detector.

Oscillator. An internal oscillator operates with a period of 1.67 seconds during no-smoke conditions. Every 1.67 seconds, internal power is applied to the entire circuit and a check is made for smoke. Every 24 clock cycles (40 seconds), a check is made for low supply by comparing V_{DD} to an internal reference. Since very-low currents are used in the device, the oscillator capacitor at pin 12 should be a low-leakage type (PTFE, polystyrene, or polypropylene).

Detector Circuitry. When smoke is detected, the resistor divider network that sets the sensitivity (smoke trip point) is altered to increase the sensitivity set voltage (pin 13) by typically 130 mV with no external connections to pins 3 or 13. This provides hysteresis and reduces false triggering. An active guard is provided on both pins adjacent to the detector input (pin 15). The voltage at pins 14 and 16 will be within 100 mV of the input. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active-guard amplifier is not power strobed and thus provides constant protection from surface leakage currents. The detector input has internal diode protection against static damage.

Alarm Circuitry. If smoke is detected, the oscillator period changes to 40 ms and the horn is enabled. The horn output is typically 160 ms ON, 80 ms OFF. During the OFF time, smoke is again checked and will inhibit further alarm output if smoke is not sensed. During smoke conditions the low-supply alarm is inhibited.

LED. The LED is continuously ON during the standby mode indicating the unit is receiving power. During a remote alarm condition the LED remains ON. The LED is OFF during a local alarm condition.

Sensitivity Adjust. The detector sensitivity to smoke is set internally by a voltage divider connected between V_{DD} and V_{SS}. The sensitivity can be externally adjusted to the individual characteristics of the ionization chamber by connecting a resistor between pin 13 and V_{DD}, or between pin 13 and V_{SS}.

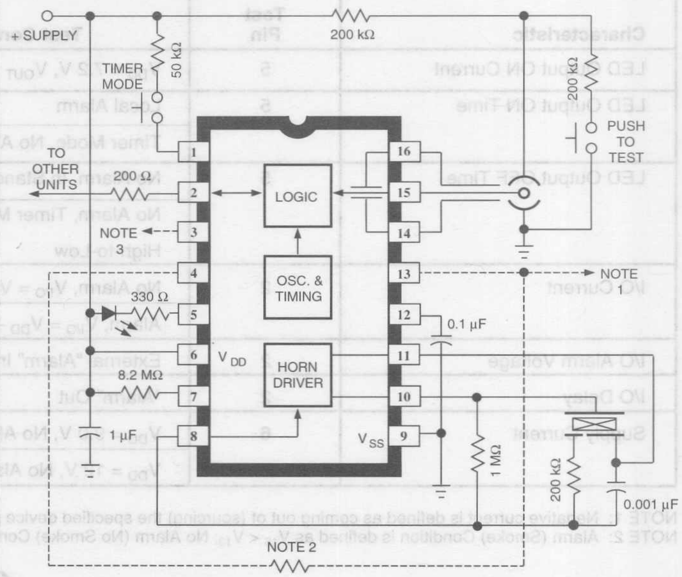
Low Supply. The low supply threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The threshold can be increased by connecting a resistor between pin 3 and V_{DD}. The threshold can be decreased by connecting a resistor between pin 3 and V_{SS}. The supply voltage level is checked every 40 seconds.

Timer. An internal timer is provided that can be used in various configurations to allow for a period of reduced smoke detector sensitivity ("hush"). When a high-to-low transition occurs at pin 1, the internal timer is reset, the timer mode enabled, and the circuit reset to a no-alarm condition (the LED will flash at a 10 second rate). If the level of smoke is increased such that the reduced sensitivity level is reached, the device will go into the alarm condition. The timer, however, will continue to completion of the nominal 10-1/4 minute period (368 clock cycles). If the timer mode is not used, pin 1 should be tied low.

I/O. A connection is provided at pin 2 to allow multiple smoke detectors to be commoned. If any single unit detects smoke (I/O is driven high), all connected units will sound their associated horns after a nominal 3 second delay. The LED remains ON when an alarm is signaled from an interconnected unit and a local smoke condition does not exist.

Testing. On power up, all internal counters are reset. Internal test circuitry allows for low-battery check by holding pins 8 and 12 low during power up, then reducing V_{DD} and monitoring $HORN_1$ (pin 10). All functional tests can be accelerated by driving pin 12 with a 2 kHz square wave. The 10 ms strobe period must be maintained for proper operation of the comparator circuitry.

TYPICAL APPLICATION

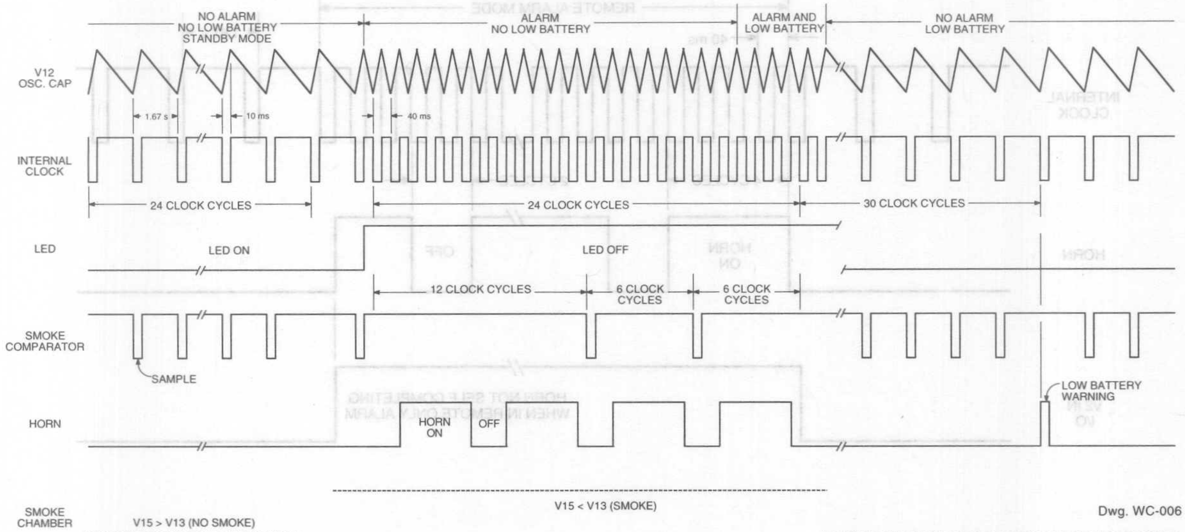


Dwg. No. EC-005-1A

NOTE 1: Use an external resistor to adjust sensitivity for a particular smoke chamber.
NOTE 2: Select resistor to reduce sensitivity during timer mode.
NOTE 3: A resistor to ground or V_{DD} may be added to this pin to modify low battery voltage threshold.
NOTE 4: Reverse supply protection must be supplied externally.

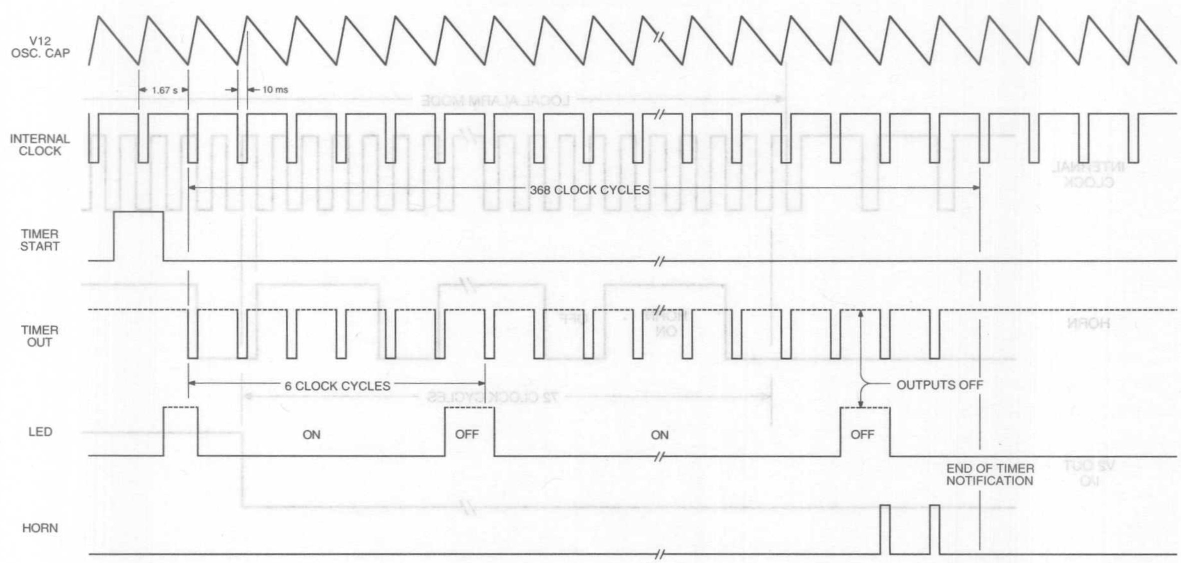
TIMING DIAGRAMS IN TYPICAL APPLICATION

NON-TIMER MODE



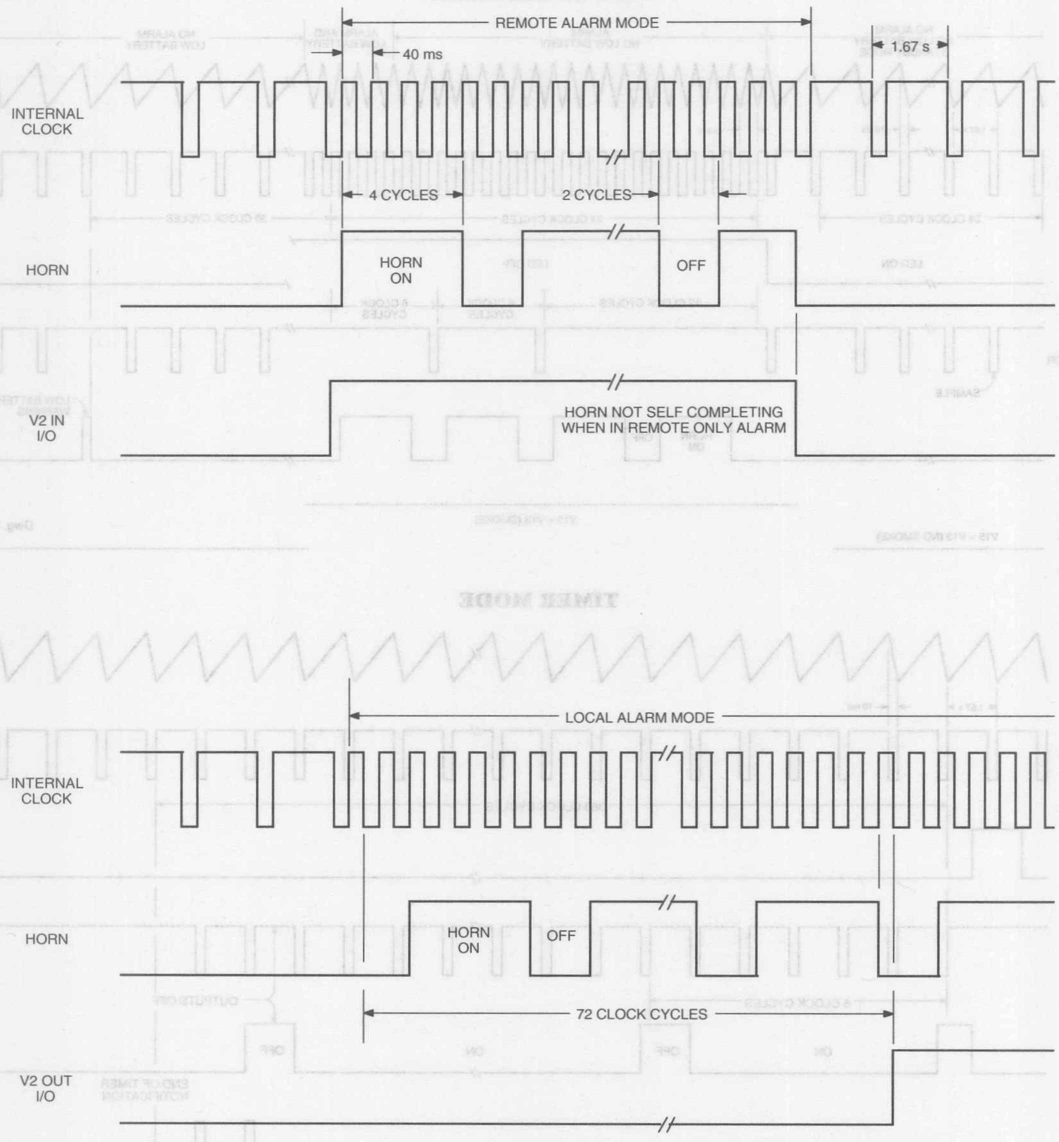
Dwg. WC-006

TIMER MODE



Dwg. WC-007

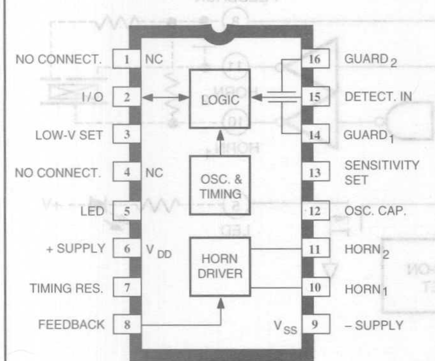
I/O OPERATION



Dwg. WC-004

5350

SMOKE DETECTOR WITH INTERCONNECT



Dwg. No. PC-004-1

The A5350CA is a low-current, CMOS circuit providing all of the required features for an ionization-type smoke detector. A networking capability allows as many as 125 units to be interconnected so that if any unit senses smoke, all units will sound an alarm. In addition, special features are incorporated to facilitate alignment and test of the finished smoke detector. This device is designed to comply with Underwriters Laboratories Specification UL217.

The internal oscillator and timing circuitry keeps standby power to a minimum by powering down the device for 1.66 seconds and sensing smoke for only 10 ms. Every 24 on/off cycles, a check is made for low battery condition. By substituting other types of sensors, or a switch for the ionization detector, this very-low power device can be used in numerous other battery-operated safety/security applications.

The A5350CA is supplied in a low-cost, 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of 0°C to +50°C.

ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to V_{SS})

Supply Voltage Range,
V_{DD} .... **-0.5 V to +15 V**
Reverse Battery (10.5 V) .... **20 s**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Input Current, I_{IN} .... **10 mA**
Operating Temperature Range,
T_A .... **0°C to +50°C**
Storage Temperature Range,
T_S .... **-55°C to +125°C**

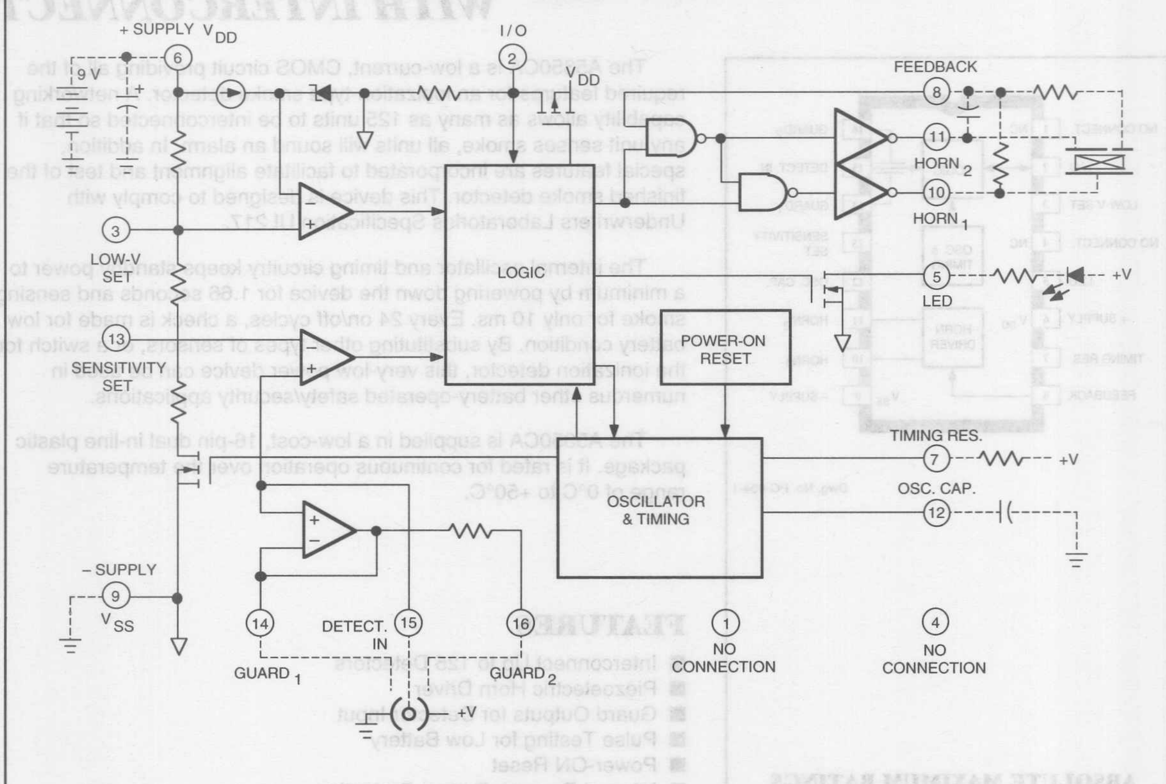
CAUTION: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FEATURES

- Interconnect Up to 125 Detectors
- Piezoelectric Horn Driver
- Guard Outputs for Detector Input
- Pulse Testing for Low Battery
- Power-ON Reset
- Internal Reverse Battery Protection

Always order by complete part number: A5350CA

FUNCTIONAL BLOCK DIAGRAM AND TYPICAL APPLICATION



Dwg. No. FC-001-3

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 9.0\ V$, $V_{SS} = 0\ V$, $C_{12} = 0.1\ \mu F$, $R_7 = 8.2\ M\Omega$ (unless otherwise noted).

Characteristic	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	6	Operating	6.0	9.0	12	V
Detector Input Current	15	0 to 40% RH, V_{IN} = 0 to 9.0 V			±1.0	pA
Input Offset Voltage	14-15	Active Guard	—	—	±100	mV
	16-15	Active Guard			±100	mV
	15-13	Detect Comparator	—	—	±50	mV
Common Mode Range	14-15	Guard Amplifier	2.0		V_{DD} - 0.5	V
	13-15	Smoke Comparator	0.5	—	V_{DD} - 2.0	V
Active Guard Impedance	14	to V_{SS}		10		kΩ
	16	to V_{SS}		500		kΩ
Oscillator Period	12	No Alarm	1.34	1.67	2.00	s
		Alarm	32	40	48	ms
Oscillator Pulse Width	4		8.0	10	12	ms
Low Voltage Threshold	6	T_A = 0 to 50°C	7.2		7.8	V
Horn Output Voltage	10-11	I_{OUT} = 16 mA, V_{DD} = 9.0 V	—	0.1	0.5	V
		I_{OUT} = 16 mA, V_{DD} = 7.2 V			0.9	V
		I_{OUT} = -16 mA, V_{DD} = 9.0 V	8.5	8.8	—	V
		I_{OUT} = -16 mA, V_{DD} = 7.2 V	6.3			V
Horn Output ON Time	10-11	Alarm	120	160	208	ms
		Low Battery	8.0	10	12	ms
Horn Output OFF Time	10-11	Alarm	60	80	104	ms
		Low Battery	32	40	48	s
LED Output ON Current	5	V_{DD} = 7.2 V, V_{OUT} = 1.0 V	10	—	—	mA
LED Output ON Time	5		8.0	10	12	ms
LED Output OFF Time	5	No Alarm, In Standby	32	40	48	s
I/O Current	2	No Alarm, $V_{I/O}$ = V_{DD} - 2.0 V	25	—	60	µA
		Alarm, $V_{I/O}$ = V_{DD} - 2.0 V	-7.5	—	—	mA
I/O Alarm Voltage	2	External "Alarm" In	3.0	—	—	V
I/O Delay	2	"Alarm" Out	—	3.0	—	s
Supply Current	6	V_{DD} = 9.0 V, No Alarm, No Loads	—	5.0	9.0	µA
		V_{DD} = 12 V, No Alarm, No Loads	—	—	12	µA

NOTE 1: Negative current is defined as coming out of (sourcing) the specified device pin.

NOTE 2: Alarm (Smoke) Condition is defined as $V_{15} > V_{13}$; No Alarm (No Smoke) Condition as $V_{15} < V_{13}$.

CIRCUIT DESCRIPTION

The A5350CA is a low-current CMOS circuit providing all of the required features for an ionization-type smoke detector.

Oscillator. An internal oscillator operates with a period of 1.67 seconds during no-smoke conditions. Every 1.67 seconds, internal power is applied to the entire circuit and a check is made for smoke. Every 24 clock cycles (40 seconds), the LED is pulsed and a check is made for low battery by comparing V_{DD} to an internal reference. Since very-low currents are used in the device, the oscillator capacitor at pin 12 should be a low-leakage type (PTFE, polystyrene, or polypropylene).

Detector Circuitry. An active guard is provided on both pins adjacent to the detector input (pin 15). The voltage at pins 14 and 16 will be within 100 mV of the input. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard amplifier is not power strobed and thus provides constant protection from surface leakage currents. The detector input has internal diode protection against static damage.

Alarm Circuitry. If smoke is detected, the oscillator period changes to 40 ms and the horn is enabled. The horn output is typically 160 ms ON, 80 ms OFF. During the OFF time, smoke is again checked and will inhibit further alarm output if smoke is not sensed. During smoke conditions the low battery alarm is inhibited and the LED is driven at a 1 Hz rate.

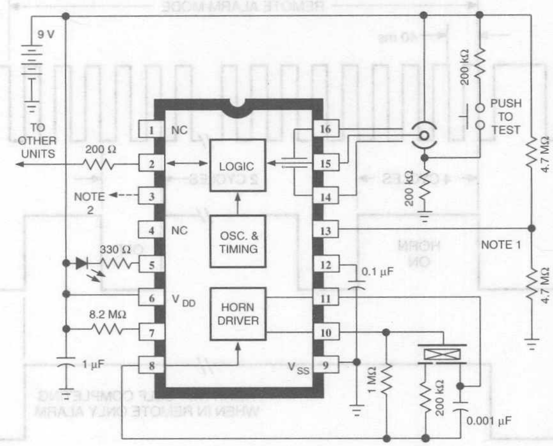
Sensitivity Adjust. The detector sensitivity must be externally adjusted to the individual characteristics of the ionization chamber by connecting resistors between pin 13 and V_{DD}, and between pin 13 and V_{SS}.

Low Battery. The low battery threshold is set internally by a voltage divider connected between V_{DD} and V_{SS}. The threshold can be increased by connecting a resistor between pin 3 and V_{DD}. The threshold can be decreased by connecting a resistor between pin 3 and V_{SS}. The battery voltage level is checked every 40 seconds during the 10 mA, 10 ms LED pulse. If an LED is not used, it should be replaced with an equivalent resistor (typically 500 Ω to 1000 Ω) such that the battery loading remains at 10 mA.

I/O. A connection is provided at pin 2 to allow multiple smoke detectors to be commoned. If any single unit detects smoke (I/O is driven high), all connected units will sound their associated horns after a nominal 3 second delay. The LED is suppressed when an alarm is signaled from an interconnected unit.

Testing. On power up, all internal counters are reset. Internal test circuitry allows for low battery check by holding pins 8 and 12 low during power up, then reducing V_{DD} and monitoring $HORN_1$ (pin 10). All functional tests can be accelerated by driving pin 12 with a 2 kHz square wave. The 10 ms strobe period must be maintained for proper operation of the comparator circuitry.

TYPICAL APPLICATION

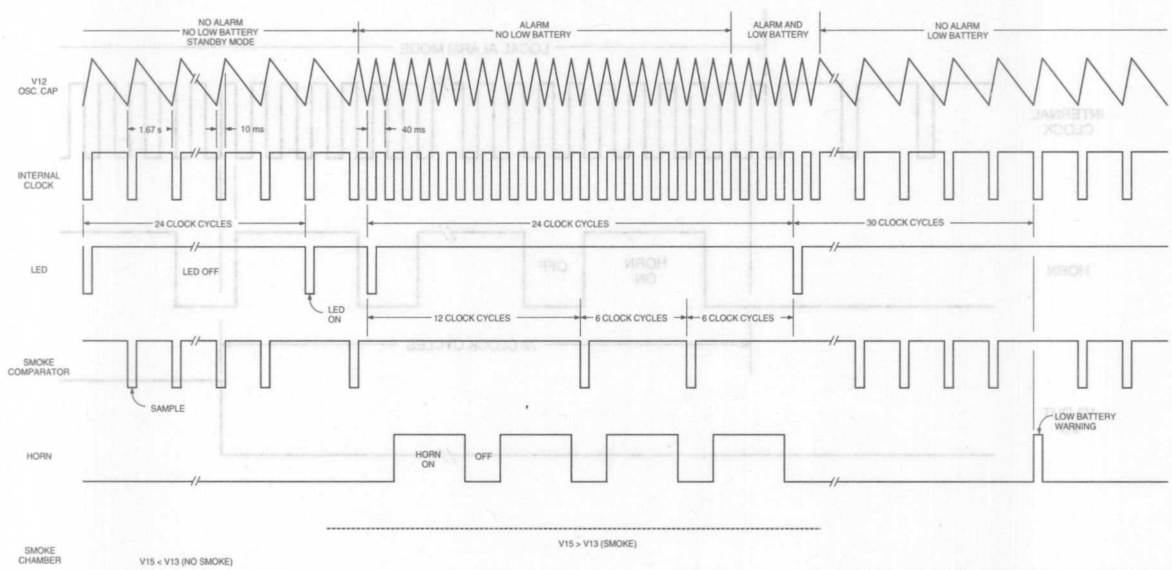


Dwg. EC-005-3

NOTE 1: An external resistor divideris used to adjust sensitivity for the particular smoke chamber.

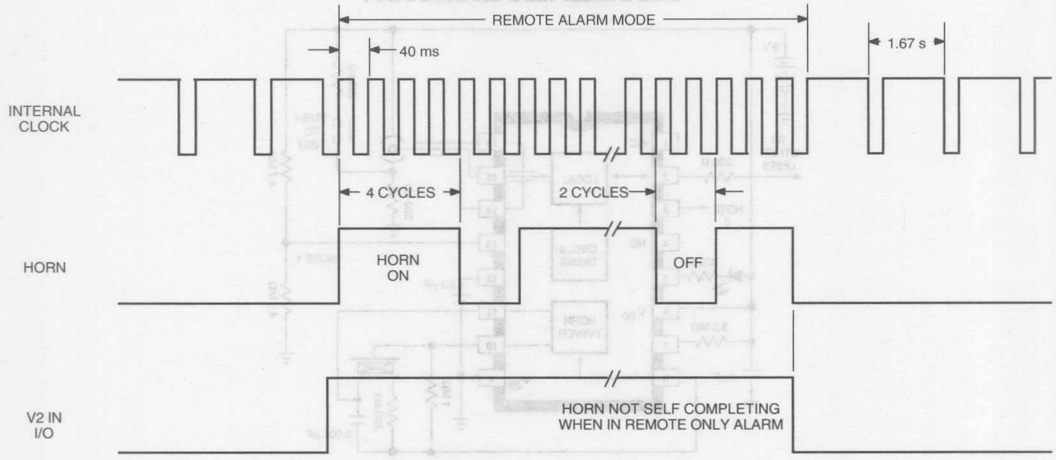
NOTE 2: A resistor to ground or V_{DD} may be added to this pin to modify low battery voltage threshold.

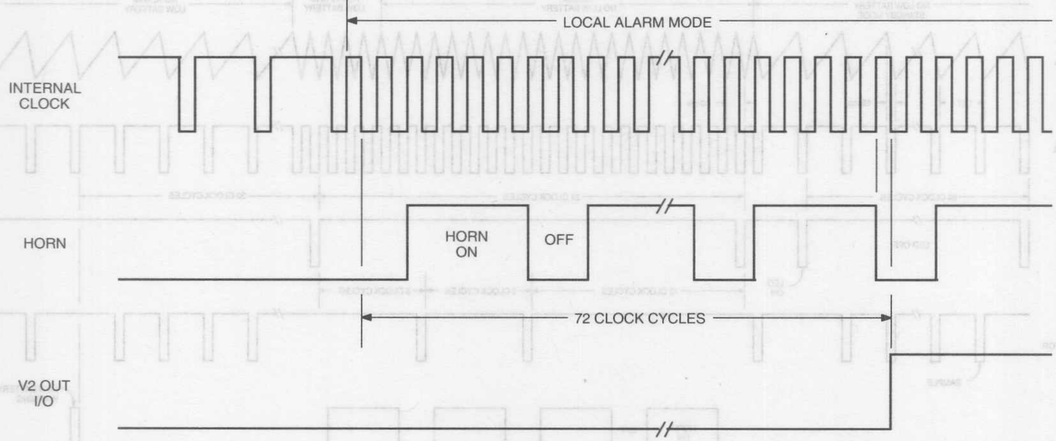
TIMING DIAGRAMS IN TYPICAL APPLICATION



Dwg. No. WC-003-1

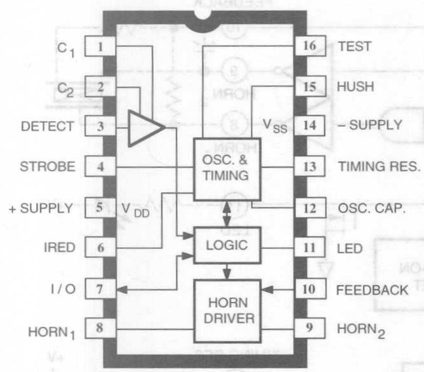
I/O OPERATION





Dwg. No. WC-004

PHOTOELECTRIC SMOKE DETECTOR WITH INTERCONNECT AND TIMER



Dwg. PC-007

The A5358CA is a low-current BiCMOS circuit providing all of the required features for a photoelectric type smoke detector. This device can be used in conjunction with an infrared photoelectric chamber to sense scattered light from smoke particles. Special features are incorporated in the design to facilitate calibration and testing of the finished detector. The device is designed to comply with Underwriters Laboratories Specification UL217.

A variable-gain photo amplifier can be directly interfaced to an infrared emitter/detector pair. The amplifier gain levels are determined by two external capacitors that are then internally selected depending on the operating mode. Low gain is selected during standby and timer modes. During a local alarm this low gain is increased (internally) by ~10% to reduce false triggering. High gain is used during the push-button test and during standby to periodically monitor the chamber sensitivity.

The internal oscillator and timing circuitry keeps standby power to a minimum by sensing for smoke every 10 seconds in a 10 µs window. A special three-stage speedup sensing scheme is incorporated to minimize the time to an audible alarm and also to reduce false triggering. Also, two consecutive cycles of degraded chamber sensitivity are required for a warning signal to occur.

The A5358CA is supplied in a low-cost 16-pin dual in-line plastic package. It is rated for continuous operation over the temperature range of -25°C to 75°C.

ABSOLUTE MAXIMUM RATINGS (Voltages are referenced to V_{SS})

Supply Voltage Range,
V_{DD} .... **-0.5 V to +15 V**
Input Voltage Range,
V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Input Current, I_{IN} .... **10 mA**
Operating Temperature Range,
T_A .... **0°C to +50°C**
Storage Temperature Range,
T_S .... **-55°C to +125°C**

CAUTION: CMOS devices have input static protection but are susceptible to damage if exposed to extremely high static electrical charges.

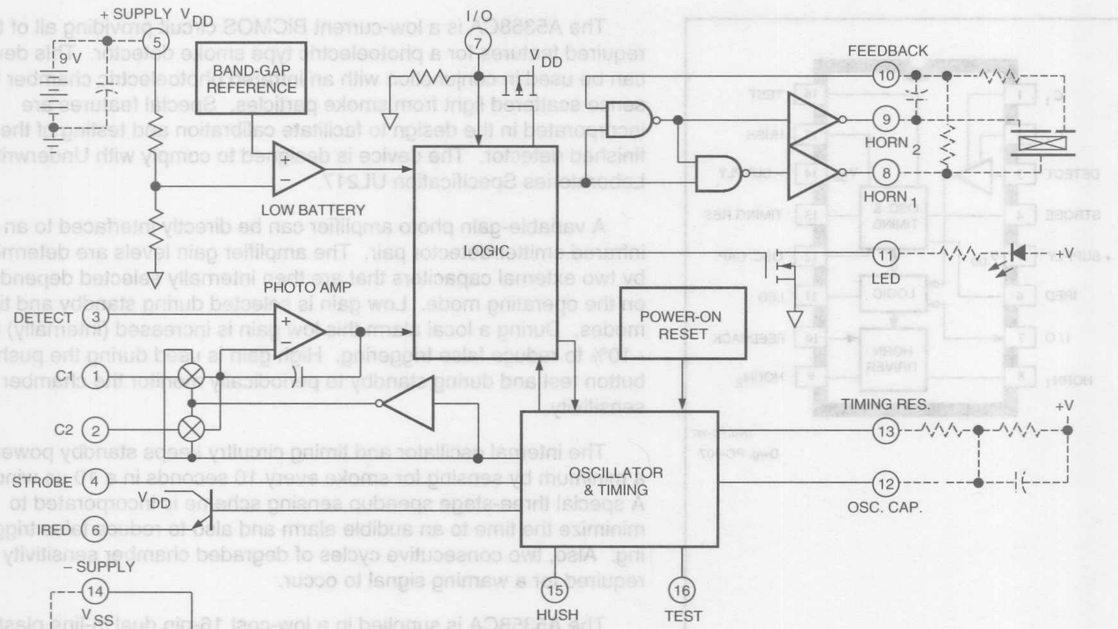
FEATURES

- Interconnect Up to 75 Detectors
- Piezoelectric Horn Driver
- All Internal Low-Battery Detection
- Power-ON Reset
- Internal Timer & Control for Reduced Sensitivity
- Built-In Circuits to Reduce False Triggering
- 6 V to 12 V Operating Voltage Range
- ESD-Protection Circuitry on All Pins

Always order by complete part number: **A5358CA** .

PHOTOELECTRIC SMOKE DETECTOR WITH INTERCONNECT AND TIMER

FUNCTIONAL BLOCK DIAGRAM



Dwg. FC-006

DC ELECTRICAL CHARACTERISTICS at $T_A = +25°C, V_{SS} = 0 V$.

Symbol	Parameter	Test Conditions	Test Pin	V_{DD}	Limits Min.	Typ.	Max	Units
V_{DD}	Supply Voltage Range		5	–	6.0	–	12	V
I_{DD}	Operating Supply Current	Average Standby Configured per Figure 1	5	12	–	–	12	µA
		During Strobe ON, I_{RED} OFF, Configured per Figure 1	5	12	–	–	2.0	mA
		During Strobe ON, I_{RED} ON, Configured per Figure 1	5	12	–	–	3.0	mA
V_{IL}	Low-Level Input Voltage		7	9	–	–	1.5	V
			10	9	–	–	2.7	V
			16	9	–	–	7.0	V
			15	9	–	–	0.5	V
V_{IH}	High-Level Input Voltage		7	9	3.2	–	–	V
			10	9	6.3	–	–	V
			16	9	8.5	–	–	V
			15	9	1.6	–	–	V
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, Strobe Active, Pin 12 @ V_{DD}	1, 2	12	–	–	100	nA
		$V_{IN} = V_{DD}$	3, 10, 12	12	–	–	100	nA
I_{IL}	Input Leakage Low	$V_{IN} = V_{ST}$, Strobe Active, Pin 12 @ V_{DD}	1, 2, 3	12	-100	–	–	nA
		$V_{IN} = V_{SS}$	10, 12	12	-100	–	–	nA
			15	12	-100			nA
I_{IN}	Input Pull-Down Current	$V_{IN} = V_{DD}$	16, 15	9	0.5	–	10	µA
		No Local Smoke, $V_{IN} = V_{DD}$	7	9	20	–	80	µA
		No Local Smoke, V_{IN} = 17 V	7	12	–	–	140	µA
V_{OL}	Low-Level Output Voltage	I_O = 10 mA	11	6.5	–	–	0.6	V
		I_O = 16 mA	8, 9	6.5	–	–	1.0	V
		I_O = 5 mA	13	6.5	–	0.5	–	V
V_{OH}	High-Level Output Voltage	I_O= -16 mA	8, 9	6.5	5.5	–	–	V
V_{ST}	Strobe Output Voltage	Inactive I_O = -1µA	4	12	V_{DD} - 0.1	–	–	V
		Active, I_O = 100 µA to 500 µA		9	V_{DD} - 4.75	–	V_{DD} - 5.25	V
$\Delta V_{ST(\Delta VDD)}$	Line Regulation	Active, V_{DD} = 6 V to 12 V		–	–	-60	–	dB
α_{ST}	Strobe Temperature Coeff.	V_{DD} = 6 V to 12 V	4	–	–	0.01	–	%/°C

Continued...

DC ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{SS} = 0 V. continued

Symbol	Parameter	Test Conditions	Test Pin	V_{DD}	Limits Min.	Typ.	Max	Units
V_{IRED}	I_{RED} Output Voltage	Inactive I_O = 1 µA	6	12	–	–	0.1	V
		Active I_O = -6 mA		9	2.85	3.1	3.35	V
$\Delta V_{IRED(\Delta VDD)}$	Line Regulation	Active, V_{DD} = 6 V to 12 V			–	-35	–	dB
α_{IRED}	I_{RED} Temperature Coefficient	V_{DD} = 6 V to 12 V	6	–	–	+0.40	–	%/°C
I_{OH}	High-Level Output Current	V_{DD} = Alarm, I/O active $V_O = V_{DD}$ - 3 V	7	9	-6.0	–	–	mA
I_{OZ}	OFF Leakage Current High	$V_O = V_{DD}$	11, 13	12	–	–	1.0	µA
I_{OZ}	OFF Leakage Current Low	$V_O = V_{SS}$	11, 13	12	–	–	-1.0	µA
$V_{DD(th)}$	Low V_{DD} Alarm Threshold		5	-	6.9	7.2	7.5	V
V_{IC}	Common Mode Voltage	Any Alarm Condition	1, 2, 3	-	V_{DD} - 4	–	V_{DD} - 2	V

AC ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{SS} = 0 V, in typical application (unless otherwise noted).

Symbol	Parameter	Test Conditions	Test Pin	V_{DD}	Limits Min.	Limits Typ.	Limits Max	Units
t_{osc}	Oscillator Period		12	9	9.4	10.5	11.5	ms
t_{led1}	Led Pulse Period	No Local or Remote Smoke	11	9	39	–	48	s
t_{led2}		Remote Smoke Only	11	9	None	–	–	
t_{led3}		Local Smoke or Test	11	9	0.60	0.67	0.74	s
t_{led4}		Timer Mode, No Alarm	11	9	9.67	10.8	11.8	s
$t_{w(led)}$	Led Pulse Width		11	9	9.5	–	11.5	ms
t_{st1}	Strobe Pulse Period	No Local or Remote Smoke	4	9	9.6	–	11.9	s
t_{st2}		After 1 of 3 Valid Samples	4	9	2.42	2.70	2.96	s
t_{st3}		After 2 of 3 Valid Samples and During Local Alarm	4	9	1.21	1.34	1.47	s
t_{st4}		Remote Alarm	4	9	9.67	10.8	11.8	s
t_{st5}		Chamber Test or Low Supply Test, No Local Alarm	4	9	38.9	–	47.1	s
t_{st6}		Pushbutton Test No Alarm	4	9	300	336	370	ms
$t_{w(st)}$	Strobe Pulse Width		11	9	9.5	–	11.5	ms
t_{ired1}	I_{RED} Pulse Period	No Local or Remote Smoke	4	9	9.6	–	11.9	s
t_{ired2}		After 1 of 3 Valid Samples	4	9	2.42	2.70	2.96	s
t_{ired3}		After 2 of 3 Valid Samples and During Local Alarm	4	9	1.21	1.34	1.47	s
t_{ired4}		Remote Alarm	4	9	9.67	10.8	11.8	s
t_{ired5}		Chamber Test, No Local Alarm	4	9	38.9	–	47.1	s
t_{ired6}		Pushbutton Test, No Alarm	4	9	300	336	370	ms
$t_{w(ired)}$	I_{RED} Pulse Width		6	9	94	–	116	µs
$t_{r(ired)}$	I_{RED} Rise Time		6		–	–	30	µs
$t_{f(ired)}$	I_{RED} Fall Time		6				200	µs
$t_{d(io)}$	I/O to Active Delay	Local Alarm	7	9	–	0	–	s
$t_{r(io)}$	Rising Edge on I/O to Alarm	No Local Alarm	7	9	–	–	1.34	s
t_{horn}	Horn Warning Pulse Period	Low Supply and Degraded Chamber Sensitivity	8, 9	9	38.9	–	47.1	s

Continued...

AC ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{SS} = 0 V, in typical application (unless otherwise noted). continued

Test Symbol	Parameter	Test Conditions	Limits Pin	V_{DD}	Min.	Typ.	Max	Units
$t_{w(horn)}$	Horn Warning Pulse Width	Low Supply and Degraded Chamber Sensitivity	8, 9	9	9.5	–	11.5	ms
$t_{on(horn)}$	Horn ON TIME	Local or Remote Alarm	8, 9	9	–	252	–	ms
$t_{off(horn)}$	Horn OFF Time	Local or Remote Alarm	8, 9	9	–	84	–	ms

PIN AND CIRCUIT DESCRIPTION

(In Typical Application)

PIN 1 (C_1)

A capacitor connected to this pin determines the gain of the photo amplifier during the push-to-test mode and during the chamber monitor test. A typical value for this high-gain mode is 0.047 µF but should be selected based on the photo chamber background reflections reaching the detector and the desired level of sensitivity. $A_e \approx 1+(C_1/10)$ where C_1 is in pF. A_e should not exceed 10 000.

PIN 2 (C_2)

A capacitor connected to this pin determines the gain of the photo amplifier during standby. A typical value for this low-gain mode is 4700 pF but should be selected based on a specific photo chamber and the desired level of sensitivity to smoke. $A_e \approx 1+(C_2/10)$ where C_2 is in pF. A_e should not exceed 10 000. This gain increases by a nominal 10% after a local alarm is detected (three consecutive detections). **Coupling of other signals to C_2 (C_1 and the DETECT inputs also) must be minimized.**

A resistor must be installed in series with C_2.

PIN 3 (DETECT)

This is the input to the photo amplifier and is connected to the cathode of the photo diode. The photo diode is operated at zero bias and should have low dark-leakage current and low capacitance.

PIN 4 (STROBE)

This output provides a strobed, regulated voltage of V_{DD} – 5 V. The minus side of all internal and external photo amplifier circuitry is referenced to this pin.

PIN 5 (V_{DD})

This pin is connected to the most-positive supply potential and can range from 6 V to 12 V with respect to V_{SS}.

PIN 6 (I_{RED})

This output provides a pulsed base current for the external npn transistor, which drives the IR emitter. Its beta should be greater than 100. The I_{RED} output is not active, to minimize noise impact, when the horn and visible LED outputs are active.

PIN 7 (I/O)

A connection at this pin allows multiple smoke detectors to be interconnected. If a local smoke condition occurs, this pin is driven high. As an input, this pin is sampled nominally every 1.35 seconds during standby. Any local-alarm condition causes this pin to be ignored as an input.

This pin has an on-chip pull-down resistor and must be left unconnected if not used. In application, there is a series current-limiting resistor to other smoke alarms.

PIN 8 ($HORN_1$)
PIN 9 ($HORN_2$)
PIN 10 (FEEDBACK)

These three pins are used in conjunction with external passive components and a self-resonating piezoelectric transducer. $HORN_1$ is connected to the piezo metal support electrode; the complementary output, $HORN_2$, is connected to the ceramic electrode and the FEEDBACK input to the feedback electrode.

Continued...

PIN AND CIRCUIT DESCRIPTION continued

A continuous modulated tone indicates either a local or remote alarm condition. A short (10 ms) chirp indicates a low-battery condition or degraded chamber sensitivity. The low-battery chirp occurs almost simultaneous with the visible LED flash. If the FEEDBACK pin is not used, it must be connected to V_{DD} or V_{SS}.

PIN 11 (LED)

This open-drain NMOS output is used to directly drive a visible LED. The load for the low-battery test is applied to this output. The low-battery test does not occur coincident with any other test or alarm signal. The LED also indicates detector status as follows (with component values as in the typical application, all times nominal):

Standby	- Pulses every 43 seconds.
Local Smoke	- Pulses every 0.67 second.
Remote Alarm	- No pulses.
Test Mode	- Pulses every 0.67 second.
Timer Mode	- Pulses every 10 seconds.

PIN 12 (OSC. CAP.)

A capacitor between this pin and V_{DD}, along with a parallel resistor, forms part of a two-terminal oscillator and sets the internal clock low time. With component values as shown, this nominal time is 11 ms and essentially the oscillator period.

PIN 13 (TIMING RES.)

A resistor between this pin and OSC. CAP. (pin 12) is part of the two-terminal oscillator and sets the internal clock high time, which is also the I_{RED} pulse width. With component values as shown, this nominal time is 105 µs.

PIN 14 (V_{SS})

This pin is connected to the most negative supply potential (usually ground).

PIN 15 (HUSH)

This input pin serves two purposes in normal operation. It serves as an enable for the internal 10-minute (nominal) timer and also as the reference for the smoke comparator during the timer mode. This reference is established by a resistive divider between V_{DD} and STROBE (R_{X1} and R_{X2}). This allows the detector to have a different sensitivity set point during the timer mode. If the timer mode is not used, this pin can be left open or connected to V_{SS}, which disables this mode.

PIN 16 (TEST)

This pin has an internal pull-down device and is used to manually invoke two test modes and a Timer Mode.

The Push-to-Test Mode is initiated by a high logic level on this pin (usually the depression of a normally open push-button switch to V_{DD}). After one oscillator cycle, I_{RED} pulses every 336 ms (nominal) and amplifier gain is increased by internal selection of C_1. Background reflections in the smoke chamber can be used to simulate a smoke condition. After the third I_{RED} pulse, a successful test (three consecutive simulated smoke conditions) activates the horn drivers and the I/O pin. When the push-button is released, the input returns to V_{SS} due to the internal pull down. After one oscillator cycle, the amplifier gain returns to normal and after three additional I_{RED} pulses (less than one second), the device exits this

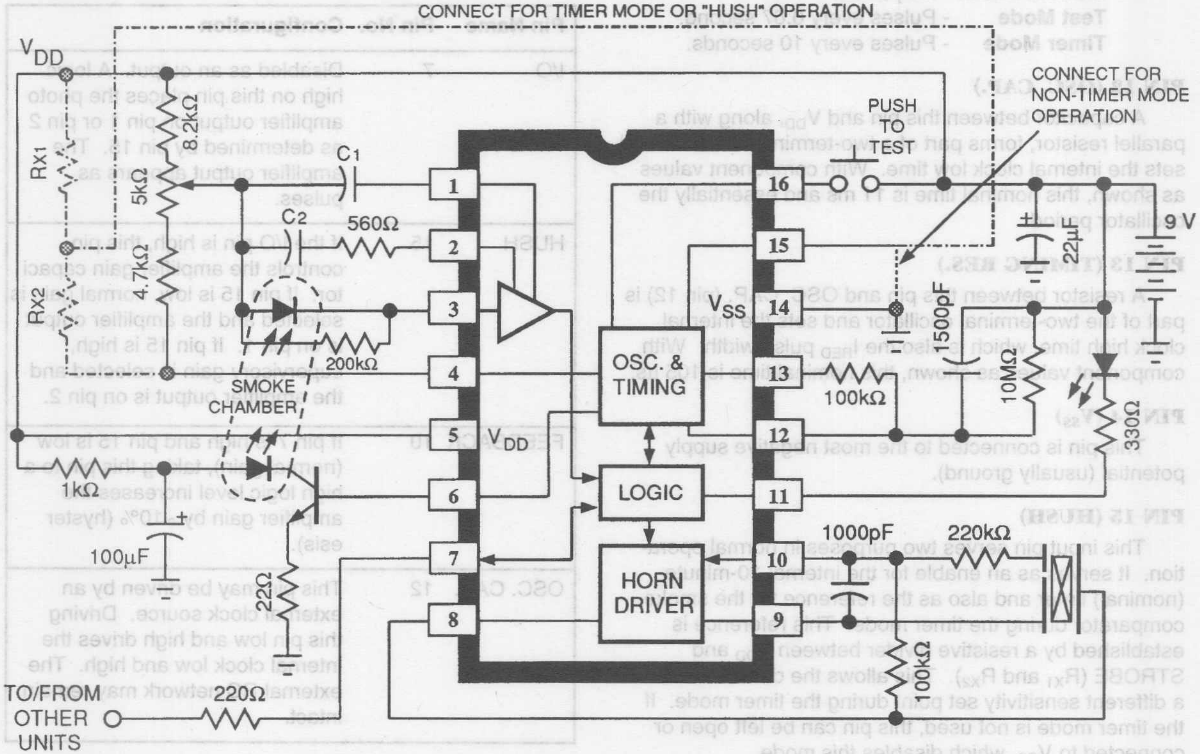
Pin Name	Pin No.	Configuration
I/O	7	Disabled as an output. A logic high on this pin places the photo amplifier output on pin 1 or pin 2 as determined by pin 15. The amplifier output appears as pulses.
HUSH	15	If the I/O pin is high, this pin controls the amplifier gain capaci tor. If pin 15 is low, normal gain is selected and the amplifier output is on pin 1. If pin 15 is high, supervisory gain is selected and the amplifier output is on pin 2.
FEEDBACK	10	If pin 7 is high and pin 15 is low (normal gain), taking this pin to a high logic level increases the amplifier gain by ~10% (hyster esis).
OSC. CAP.	12	This pin may be driven by an external clock source. Driving this pin low and high drives the internal clock low and high. The external RC network may remain intact.

mode and returns to standby. This high-to-low transition on pin 16 also resets and starts the 10 minute hush timer (timer mode).

The Diagnostic Test Mode is initiated by pulling this pin below V_{SS} and continuously sourcing 400 µA from the pin for at least one clock cycle on the OSC. CAP. pin. This mode is used to facilitate calibration and test of the IC and the assembled detector. In this mode, certain device pins are reconfigured as described below. In this mode, the I_{RED} pulse rate is increased to one every OSC. CAP. cycle and the STROBE pin is always active. To exit this mode, the test pin is floated for at least one OSC. CAP. cycle.

Pin Name	Pin No.	Configuration
$HORN_1$	8	This pin is reconfigured as the smoke integrator output. Three consecutive smoke detections will cause this pin to go high and three consecutive no-smoke detections cause this pin to go low.
LED	11	This pin becomes a low-battery indicator. The open-drain NMOS output is normally OFF. If V_{DD} falls below the low-battery thresh old, the output turns ON.

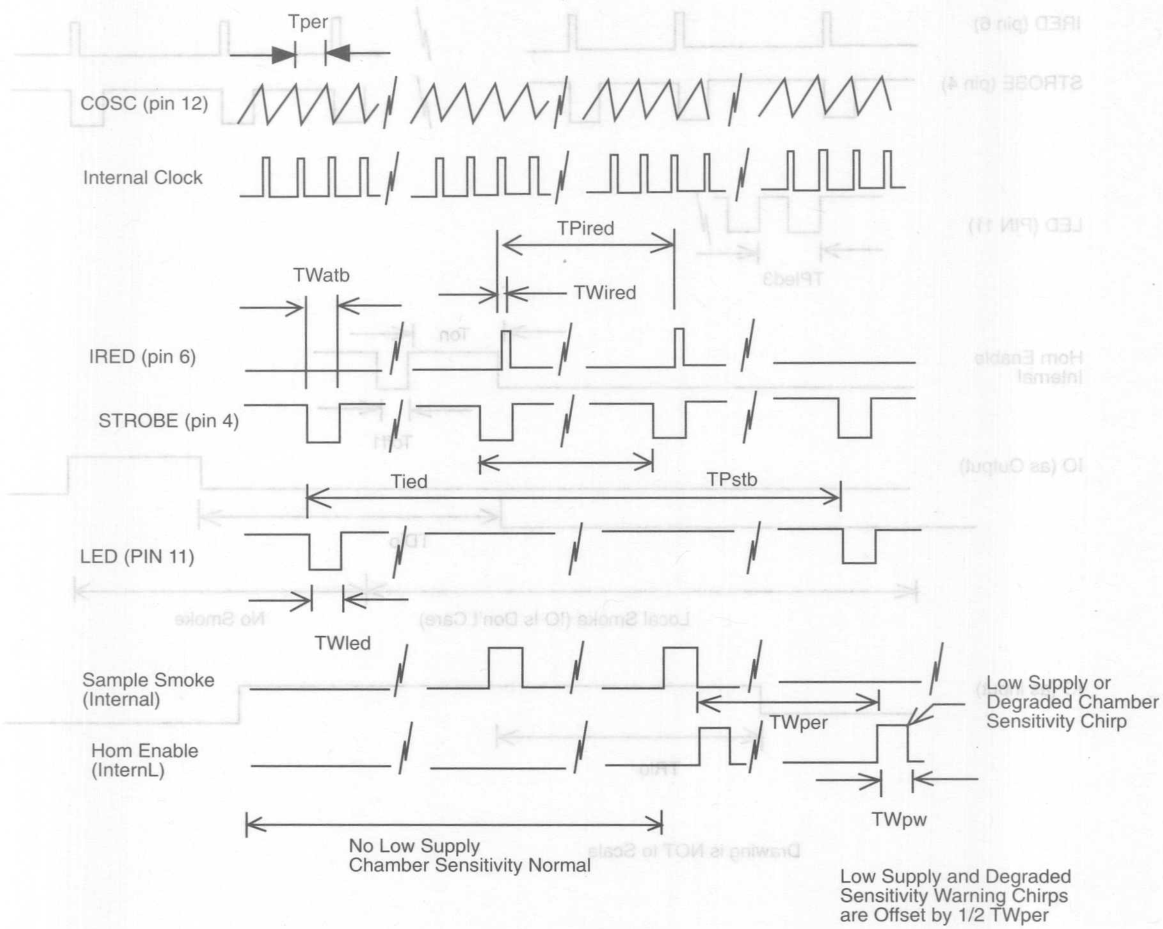
TYPICAL APPLICATION



Dwg. EC-006

STANDBY TIMING DIAGRAM

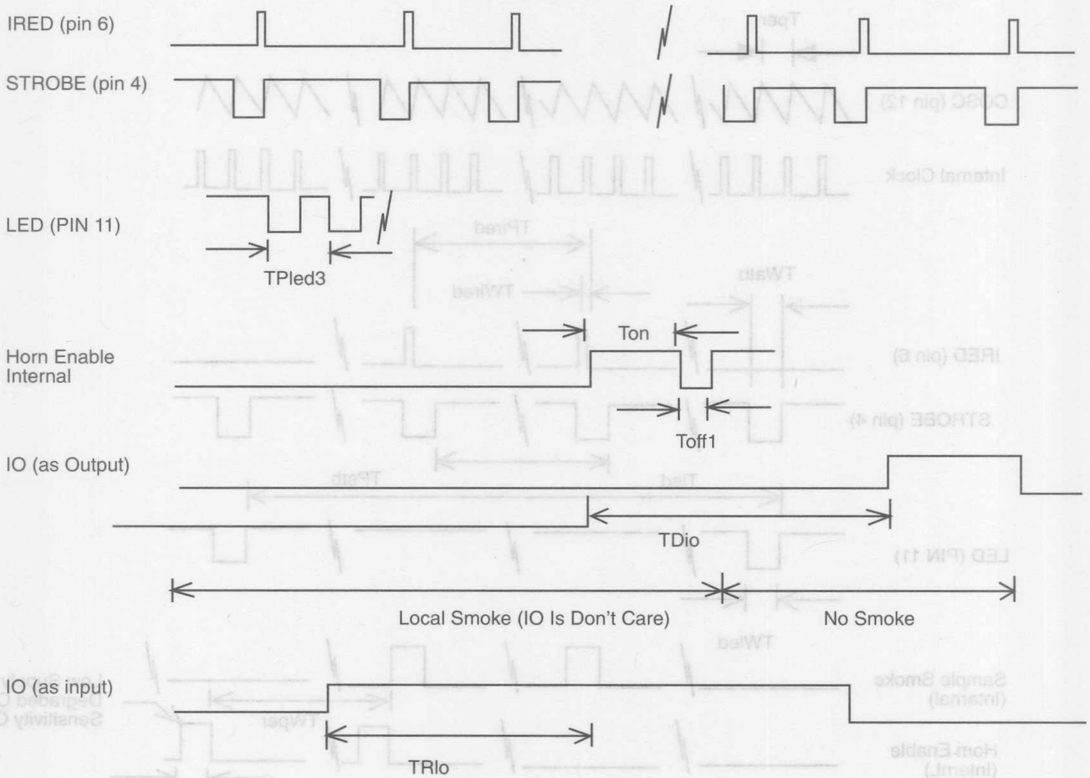
FIGURE 4



NOT to Scale

LOCAL ALARM TIMING DIAGRAM

FIGURE 5



Drawing is NOT to Scale

SECTION 8. TECHNICAL DATA FOR DISCRETE TRANSISTORS, DIODES, AND ARRAYS

QUICK GUIDE

TO ALLEGRO DISCRETE DEVICES

Series 1N	JEDEC-registered general-purpose and Zener diodes. See Series TMPD and TMPZ.
Series 2N	JEDEC-registered general-purpose, small-signal, switching, and field-effect transistors in TO-92/TO-226AA plastic packages. See also Series TMPT and TP.
Series BA	Pro-Electron registered diodes in SOT-23/TO-236AB surface-mount packages.
Series BZX84	Pro-Electron registered Zener diodes in SOT-23/TO-236AB surface-mount packages. Nominal voltage ratings from 3.9 volts to 56 volts are available.
Series MPS	General-purpose transistors in TO-92/TO-226AA plastic packages; generally with E-B-C pinning.
Series TH-	Discrete semiconductors in unpackaged, chip form. Contact local office for information.
Series TMPD	General-purpose, Schottky, and dual diodes in SOT-23/TO-236AB surface-mount packages.
Series TMPT	General-purpose, small-signal, and switching transistors in SOT-23/TO-236AB surface-mount packages.
Series TMPZ	Zener diodes in SOT-23/TO-236AB surface-mount packages. Nominal voltage ratings from 4.3 volts to 33 volts are available.
Series TND	Diode arrays in 14- or 16-pin dual in-line plastic packages. Eight isolated diodes or arrays of 8 to 15 diodes in common-anode or common-cathode configurations are available .
Series TP	General-purpose, small-signal, and switching transistors in TO-92/TO-226AA plastic packages. Interchangeable with JEDEC-registered and industry-standard devices in TO-98/TO-226AD plastic packages.
Series TPQ	Four isolated transistors in 14-pin dual in-line plastic packages. Quad NPN, quad PNP, and dual complementary pairs are available.
	See also, high-current multiple Darlington arrays in Section 3.

INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	Pinning 2	Pinning 3	Ratings (Page)
1N914	Diode	TMPD914	TO-236AB	A	NC	K	8-17
1N4148	Diode	TMPD4148	TO-236AB	A	NC	K	8-17
1N5230	Zener	TMPZ5230	TO-236AB	A	NC	K	8-27
1N5231	Zener	TMPZ5231	TO-236AB	A	NC	K	8-27
1N5232	Zener	TMPZ5232	TO-236AB	A	NC	K	8-27
1N5234	Zener	TMPZ5234	TO-236AB	A	NC	K	8-27
1N5236	Zener	TMPZ5236	TO-236AB	A	NC	K	8-27
1N5237	Zener	TMPZ5237	TO-236AB	A	NC	K	8-27
1N5239	Zener	TMPZ5239	TO-236AB	A	NC	K	8-27
1N5240	Zener	TMPZ5240	TO-236AB	A	NC	K	8-27
1N5242	Zener	TMPZ5242	TO-236AB	A	NC	K	8-27
1N5243	Zener	TMPZ5243	TO-236AB	A	NC	K	8-27
1N5249	Zener	TMPZ5249	TO-236AB	A	NC	K	8-27
1N5254	Zener	TMPZ5254	TO-236AB	A	NC	K	8-27
1N5711	Schottky	TMPD5711	TO-236AB	A	NC	K	8-17
2N2222	NPN	TPQ2222	14-Pin Dip	Quad Transistor Array			8-30
		TPQ6502	14-Pin DIP	Dual Complementary Pair			8-30
2N2222A	NPN	TMPT2222A	TO-236AB	B	E	C	8-5
		TP2222A	TO-226AA	E	B	C	8-4
		TPQ2222A	14-Pin DIP	Quad Transistor Array			8-30
2N2907	PNP	TPQ6502	14-Pin DIP	Dual Complementary Pair			8-30
2N2907A	PNP	TMPT2907A	TO-236AB	B	E	C	8-11
		TP2907A	TO-226AA	E	B	C	8-10
		TPQ2907A	14-Pin DIP	Quad Transistor Array			8-30
2N3416	NPN	2N3416	TO-226AA	E	C	B	8-4
2N3417	NPN	2N3417	TO-226AA	E	C	B	8-4
2N3904	NPN	2N3904	TO-226AA	E	B	C	8-4
		TMPT3904	TO-236AB	B	E	C	8-5
		TPQ3904	14-Pin DIP	Quad Transistor Array			8-30
2N3906	PNP	2N3906	TO-226AA	E	B	C	8-10
		TMPT3906	TO-236AB	B	E	C	8-11
		TPQ3906	14-Pin DIP	Quad Transistor Array			8-30

For devices in unpackaged, chip form, contact local office.

DISCRETE SEMICONDUCTORS
INDEX AND CROSS REFERENCE

Industry Number	Type	Allegro Number(s)	Allegro Package	Pinning 1	Pinning 2	Pinning 3	Ratings (Page)
2N4401	NPN	2N4401	TO-226AA	E	B	C	8-4
		TMPT4401	TO-236AB	B	E	C	8-5
2N4403	PNP	2N4403	TO-226AA	E	B	C	8-10
		TMPT4403	TO-236AB	B	E	C	8-11
2N5087	PNP	TMPT5087	TO-236AB	B	E	C	8-11
2N5088	NPN	2N5088	TO-226AA	E	B	C	8-4
2N5089	NPN	TMPT5089	TO-236AB	B	E	C	8-5
2N5308	NPN	2N5308	TO-226AA	E	C	B	8-4
2N5401	PNP	2N5401	TO-226AA	E	B	C	8-10
		TMPT5401	TO-236AB	B	E	C	8-11
2N6427	NPN	2N6427	TO-226AA	E	B	C	8-4
		TMPT6427	TO-236AB	B	E	C	8-5
A8920SLR	Schottky	A8920SLR	TO-236AB	A1	K2	KA	8-32
BAS16	Diode	BAS16	TO-236AB	A	NC	K	8-17
BAV70	Dual Diode	BAV70	TO-236AB	A1	A2	K	8-17
BAV99	Dual Diode	BAV99	TO-236AB	A1	K2	AK	8-17
BAW56	Dual Diode	BAW56	TO-236AB	K1	K2	A	8-17
BZX84C5V1	Zener	BZX84C5V1	TO-236AB	A	NC	K	8-27
BZX84C5V6	Zener	BZX84C5V6	TO-236AB	A	NC	K	8-27
BZX84C6V2	Zener	BZX84C6V2	TO-236AB	A	NC	K	8-27
BZX84C12	Zener	BZX84C12	TO-236AB	A	NC	K	8-27
MPSA06	NPN	MPSA06	TO-226AA	E	B	C	8-4
		TMPTA06	TO-236AB	B	E	C	8-5
MPSA13	NPN	MPSA13	TO-226AA	E	B	C	8-4
MPSA14	NPN	MPSA14	TO-226AA	E	B	C	8-4
MPSA42	NPN	MPSA42	TO-226AA	E	B	C	8-4
		TMPTA42	TO-236AB	B	E	C	8-5
MPSA56	PNP	MPSA56	TO-226AA	E	B	C	8-10
		TMPTA56	TO-236AB	B	E	C	8-11
TMPD...	Diode	Various	TO-236AB		Various		8-17
TMPT...	Transistor	See 2N...	TO-236AB		Various		See 2N...
TMPTA...	Transistor	See MPSA...	TO-236AB		Various		See MPSA...
TMPZ...	Zener	See 1N...	TO-236AB		Various		8-27
TND...	Array	TND...	14 or 16-Pin DIP		6-to-15 Diode Array		8-29
TP...	Transistor	See 2N...	TO-226AA		Various		See 2N...
TPQ...	Array	TPQ...	14-Pin DIP		Quad Darlington Array		8-30

For devices in unpackaged, chip form, contact local office.

NPN TRANSISTORS

TO-92/TO-226AA

'2N' and 'TP' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TP2222A	500	75	40	6.0	10	60	100	300	150	10	0.3	150	250	20	8.0	225	—	EBC
2N3416	500	50	50	5.0	100	50	75	225	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3417	500	50	50	5.0	100	50	180	540	2.0	4.5	0.3	50	—	—	—	—	—	ECB
2N3904	200	60	40	6.0	50	30	100	300	10	1.0	0.2	10	300	10	4.0	—	5.0	EBC
2N4401	500	60	40	6.0	100	30	100	300	150	1.0	0.4	150	250	20	6.5	225	—	EBC
2N5088	100	35	30	—	50	20	300	900	0.1	5.0	0.5	10	—	—	4.0	—	3.0	EBC
2N5308	500	40	40	12	100	40	7k	70k	2.0	5.0	1.4	200	60	2.0	10	—	—	ECB
2N6427	500	40	40	12	50	30	10k	100k	10	5.0	1.2	50	130	10	7.0	—	10	EBC

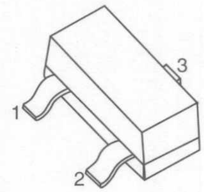
NOTES: 1) Maximum at typical JEDEC conditions.
2) $V_{(BR)CES}$

'MPS' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
MPSA06	800	80	80	4.0	100	80	50	—	100	1.0	0.25	100	100	10	—	—	—	EBC
MPSA13	500	30[2]	—	10	100	30	10k	—	100	5.0	1.5	100	125	10	—	—	—	EBC
MPSA14	500	30[2]	—	10	100	30	20k	—	100	5.0	1.5	100	125	10	—	—	—	EBC
MPSA42	500	300	300	6.0	100	200	40	—	30	10	0.5	20	50	10	3.0	—	—	EBC

NOTES: 1) Maximum at typical JEDEC conditions.
2) $V_{(BR)CES}$

NPN TRANSISTORS



SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TMPT2222A	1P	75	40	6.0	10	60	100	300	150	10	0.3	150	250	20	8.0	225	—	BEC
TMPT3904	1A	60	40	6.0	50	30	100	300	10	1.0	0.2	10	300	10	4.0	200	5.0	BEC
TMPT4401	2X	60	40	6.0	100	30	100	300	150	1.0	0.4	150	250	20	6.5	225	—	BEC
TMPT5089	1R	30	25	—	50	15	400	1200	0.1	5.0	0.5	10	—	—	4.0	—	2.0	BEC
TMPT6427	1V	40	40	12	50	30	10k	100k	10	5.0	1.2	50	130	10	7	—	10	BEC
TMPTA06	1G	80	80	4.0	100	80	50	—	100	1.0	0.25	100	100	10	—	—	—	BEC
TMPTA42	1D	300	300	6.0	100	200	40	—	30	10	0.5	20	50	10	3.0	—	—	BEC

NOTES: 1) Maximum at typical JEDEC conditions.
2) $V_{(BR)CES}$

PNP TRANSISTORS

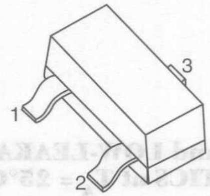
TO-92/TO-226AA

'2N' and 'TP' DEVICE TYPES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TP2907A	500	60	60	5.0	10	50	100	300	150	10	0.4	150	200	50	8.0	100	—	EBC
2N3906	200	40	40	5.0	—	—	100	300	10	1.0	0.25	10	250	10	4.5	225	4.0	EBC
2N4403	500	40	40	5.0	—	—	100	300	150	2.0	0.4	150	200	20	10	225	—	EBC
2N5401	300	160	150	5.0	50	120	60	240	10	5.0	0.2	10	100	10	6.0	—	8.0	EBC
MPSA56	800	80	80	4.0	100	80	50	—	100	1.0	0.25	100	50	100	—	—	—	EBC

NOTES: 1) Maximum at typical JEDEC conditions.
2) $V_{(BR)CES}$

PNP TRANSISTORS



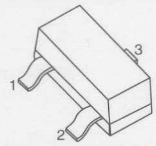
SOT-23/TO-236AB

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain h_{FE} Max.	DC Current Gain @ I_C (mA)	DC Current Gain @ V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Pinning 1, 2, 3
TMPT2907A	2F	60	60	5.0	10	50	100	300	150	10	0.4	150	200	50	8.0	100	—	BEC
TMPT3906	2A	40	40	5.0	—	—	100	300	10	1.0	0.25	10	250	10	4.5	225	4.0	BEC
TMPT4403	2T	40	40	5.0	—	—	100	300	150	2.0	0.4	150	200	20	10	225	—	BEC
TMPT5087	2Q	50	50	—	50	35	250	800	0.1	5.0	0.3	10	40	0.5	4.0	—	2.0	BEC
TMPT5401	2L	160	150	5.0	50	120	60	240	10	5.0	0.2	10	100	10	6.0	—	8.0	BEC
TMPTA56	2G	80	80	4.0	100	80	50	—	100	1.0	0.25	100	50	100	—	—	—	BEC

NOTES: 1) Maximum at typical JEDEC conditions.
2) $V_{(BR)CES}$

DIODES



SOT-23/TO-236AB

'TMPD' GENERAL-PURPOSE and LOW-LEAKAGE DIODES ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Device Type	Description	Marking	I_F Max. (mA)	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max. (nA)	t_{rr} Max. (ns)	C_O Max. (pF)	Pinning 1, 2, 3
TMPD914	General-Purpose	5D	600	100	1.0	10	25	4.0	6.0	A NC K
TMPD2836	Common Anode	A2	500	75	1.0	10	0.10	6.0	4.0	K1 K2 A
TMPD2838	Common Cathode	A6	500	75	1.0	10	0.10	6.0	4.0	A1 A2 K
TMPD4148	General-Purpose	5D	600	100	1.0	10	25	4.0	4.0	A NC K
TMPD6050	Low Leakage	5A	600	70	1.1	100	0.10	10	2.5	A NC K
TMPD7000	Dual In-Series	5C	600	100	1.1	100	0.30	15	1.5	A1 K2 A/K

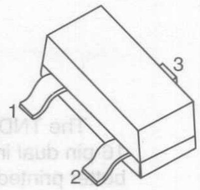
'TMPD' SCHOTTKY DIODES (see also A8920SLR) ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Device Type	V_{BR} Min. (V)	V_F Max. I_F = 1 mA (V)	V_F Max. I_F = 10 mA (mA)	I_R Max. V_R = 1 V (nA)	I_R Max. V_R = 20 V (nA)	I_R Max. V_R = 50 V (nA)	C_O Max. (pF)	Pinning 1, 2, 3
TMPD5711	70	0.41	0.75	—	50	200	2.0	A NC K
TMPD6916	40	0.34	0.47	100	200	—	5.0	A NC K
TMPD6924	70	0.41	0.75	—	—	200	2.0	A NC K

PRO-ELECTRON DEVICE TYPES ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Device Type	Description	Marking	I_F Max. (mA)	V_{BR} Min. (V)	V_F Max. (V)	V_F @I_F (mA)	I_R Max. (nA)	t_{rr} Max. (ns)	C_O Max. (pF)	Pinning 1, 2, 3
BAS16	General-Purpose	A6	600	75	0.72	1.0	1000	6.0	2.0	A NC K
BAV70	Common Cathode	A4	100	70	0.86	10	5000	6.0	1.5	A1 A2 K
BAV99	Dual In-Series	A7	70	70	1.1	50	2500	6.0	2.0	A1 K2 A/K
BAW56	Common Anode	A1	70	70	1.1	50	2500	6.0	2.0	K1 K2 A

ZENER DIODES



SOT-23/TO-236AB

'TMPZ' ZENER DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	Zener Voltage Min. (V)	Zener Voltage Nom. (V)	Zener Voltage Max. (V)	Zener Voltage $@I_{ZT}$ (mA)	Leakage Current Max (μA)	Leakage Current $@V_R$ (V)	Zener Impedance Max. Z_{ZT} (Ω)	Zener Impedance $@I_{ZT}$ (mA)	Pinning 1, 2, 3
TMPZ5230	8E	4.47	4.7	4.94	20	5.0	2.0	19	20	A NC K
TMPZ5231	8F	4.85	5.1	5.36	20	5.0	2.0	17	20	A NC K
TMPZ5232	8G	5.32	5.6	5.88	20	5.0	3.0	11	20	A NC K
TMPZ5234	8J	5.98	6.2	6.51	20	3.0	4.0	7.0	20	A NC K
TMPZ5236	8L	7.13	7.5	7.88	20	3.0	6.0	6.0	20	A NC K
TMPZ5237	8M	7.79	8.2	8.61	20	3.0	6.5	8.0	20	A NC K
TMPZ5239	8P	8.65	9.1	9.56	20	3.0	7.0	10	20	A NC K
TMPZ5240	8Q	9.50	10	10.5	20	3.0	8.0	17	20	A NC K
TMPZ5242	8S	11.4	12	12.6	20	1.0	9.1	30	20	A NC K
TMPZ5243	8T	12.4	13	13.7	9.5	0.5	9.9	13	9.5	A NC K
TMPZ5249	8Z	18.1	19	20.0	6.6	0.1	14.0	23	6.6	A NC K
TMPZ5254	81E	25.7	27	28.4	4.6	0.1	21.0	41	4.6	A NC K

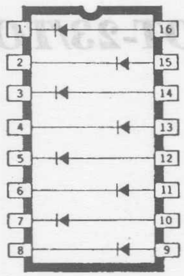
'BZX84' ZENER DIODES
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	Marking	Zener Voltage Min. (V)	Zener Voltage Nom. (V)	Zener Voltage Max. (V)	Zener Voltage $@I_{ZT}$ (mA)	Leakage Current Max (μA)	Leakage Current $@V_R$ (V)	Zener Impedance Max. Z_{ZT} (Ω)	Zener Impedance $@I_{ZT}$ (mA)	Pinning 1, 2, 3
BZX84C5V1	Z2	4.8	5.1	5.4	5.0	2.0	2.0	60	5.0	A NC K
BZX84C5V6	Z3	5.2	5.6	6.0	5.0	1.0	2.0	40	5.0	A NC K
BZX84C6V2	Z4	5.8	6.2	6.6	5.0	3.0	4.0	10	5.0	A NC K
BZX84C12	Y2	11.4	12.0	12.7	5.0	0.1	8.0	25	5.0	A NC K

DIODE ARRAYS

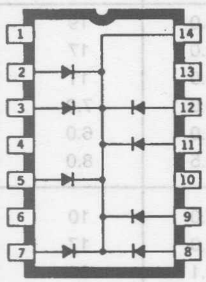
The TND series consists of diode arrays packaged in 14-pin and 16-pin dual in-line plastic packages for easy automatic insertion and better printed circuit board density.

In addition to the diode characteristics for standard products shown here, arrays consisting of diodes with 1N3070, 1N3595, 1N3600, 1N4153, or 1N4447 characteristics can be furnished on request. Other package configurations are available on special order.



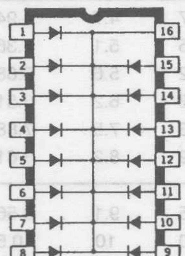
Dwg. No. A-10,903

TND903
TND908
TND918



Dwg. No. A-13,359

TND933
TND940



Dwg. No. A-10,901

TND905

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

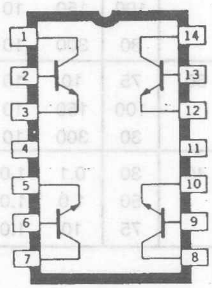
	V_{BR}	V_F		I_R			V_{BR}	V_F		I_R	
Device Type	Min. (V)	Max. (V)	$@I_F$ (mA)	Max. (nA)	@ V_R (V)	Device Type	Min. (V)	Max. (V)	$@I_F$ (mA)	Max (nA)	@ V_V (V)
TND903	75	1.0	100	—	—	TND933	60	1.0	100	100	40
TND905	100	1.0	10	—	—	TND940	40	1.0	100	100	25
TND908	100	1.0	10	—	—						
TND918	75	1.0	50	—	—						

SERIES TPQ

QUAD TRANSISTOR ARRAYS

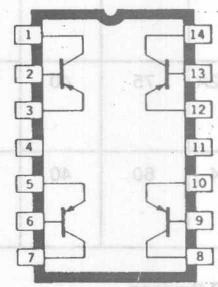
Series TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent devices.

All of these devices are furnished in a 14-pin dual in-line plastic package. The molded package is identical to that used with most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.



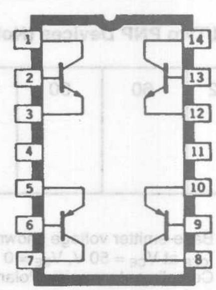
Dwg. No. A-10,050A

TPQ2222
TPQ2222A
TPQ3904



Dwg. No. A-10,051A

TPQ2907A
TPQ3906



Dwg. No. A-10,053A

TPQ6502

ABSOLUTE MAXIMUM RATINGS

Power Dissipation, P_D
(Each Transistor) .... **500 mW**
(Total Package) .... **2.0 W***
Operating Temperature Range,
T_A .... **-55°C to +150°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

* Derate at the rate of 16 mW/°C above T_A = +25°C

SERIES TPQ
QUAD TRANSISTOR ARRAYS

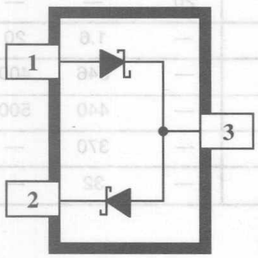
ELECTRICAL CHARACTERISTICS at T_A = +25°C

Part Number	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max (nA)	I_{CBO} @ V_{CB} (V)	DC Current Gain h_{FE} Min.	DC Current Gain Conditions I_C (mA)	DC Current Gain Conditions V_{CE} (V)	Saturation Voltage V_{CE} Max. (V)	Saturation Voltage V_{BE} Max. (V)	Saturation Voltage @ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	C_{ob} Max. (pF)	Similar Discrete Devices
Four NPN Devices															
TPQ2222	60	40	5.0	50	50	75 100 30	10 150 300	10 10 10	0.40 1.60	1.30 2.60	150 300	200	20	8.0	2N2222
TPQ2222A	75	40	6.0	50	50	75 100 30	10 150 300	10 10 10	0.40 1.60	1.30 2.60	150 300	200	20	8.0	2N2222A
TPQ3904	60	40	6.0	50	40	30 50 75	0.1 1.0 10	1.0 1.0 1.0	0.20	0.85	10	250	10	4.0	2N3904
Four PNP Devices															
TPQ2907A	-60	-60	-5.0	50	-30	75 100 50	10 150 300	-10 -10 -10	-0.40 -1.60	-1.30 -2.60	150 300	200	50	8.0	2N2907A
TPQ3906	-40	-40	-5.0	50	-30	40 60 75	0.1 1.0 10	-1.0 -1.0 -1.0	-0.25	-0.85	10	200	10	4.5	2N3906
Two NPN/Two PNP Devices (Note 3)															
TPQ6502	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907

NOTE: 1. Base-emitter voltage shown is $V_{BE(ON)}$ at indicated I_C, V_{CE} = 5.0 V.
2. I_{CES} at V_{CE} = 50 V, V_{BE} = 0
3. Complimentary pairs. Polarity shown is for NPN devices.NOTE:

8920

DUAL SCHOTTKY DIODE



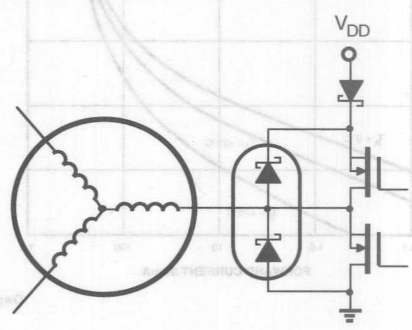
Dwg. No. PD-002

Schottky barrier diodes combine high rectification efficiency with high switching speeds and low series resistance. The A8920SLR dual-diode is designed specifically for hard-disk drive applications requiring low voltage drop rectification of the spindle motor back-EMF during power-down head retraction. It is supplied in a 3-lead small-outline transistor package (SOT-23/TO-236AB) for surface-mounting for use over the operating temperature range of -20°C to +85°C.

FEATURES

- Low Forward Voltage Drop 440 mV Typical at 150 mA
- 500 mA Forward Current
- 20 V Reverse Voltage

TYPICAL APPLICATION



Dwg. No. ED-002

ABSOLUTE MAXIMUM RATINGS at T_A=+25°C

Forward Current, I_F .... **500 mA**
Reverse Voltage, V_R .... **20 V**
Operating Temperature Range,
T_A .... **-20°C to +85°C**
Storage Temperature Range,
T_S .... **-65°C to +150°C**

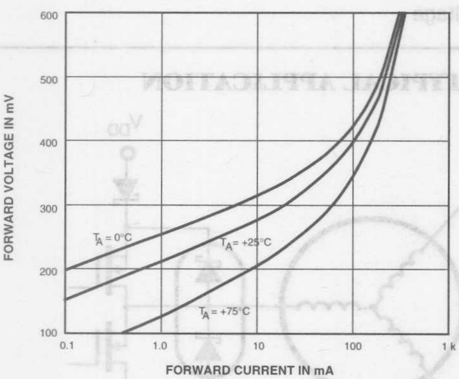
Always order by complete part number: **A8920SLR**.

8920
DUAL SCHOTTKY DIODE

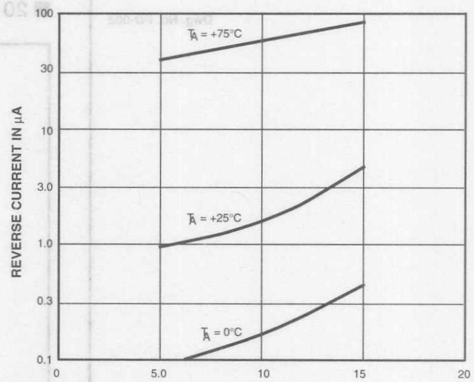
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Reverse Breakdown Voltage	$V_{(BR)}$	$I_R = 100\ \mu A$	20	—	—	V
Reverse Leakage Current	I_R	$V_R = 10\ V$	—	1.6	20	µA
Forward Voltage	V_F	$I_F = 50\ mA$	—	346	400	mV
		$I_F = 150\ mA$	—	440	500	mV
Junction Capacitance	C_T	$V_R = 0\ V$, f = 1 MHz	—	370	—	pF
Reverse Recovery Time	t_{rr}	$I_F = I_R = 100\ mA$	—	32	—	ns

TYPICAL CHARACTERISTICS



Dwg. GD-003



Dwg. GD-004

SOT-23 TRANSISTORS

All transistor and diode device types are constantly monitored through ongoing mechanical and moisture tests. The reliability chart below shows typical data from moisture tests (pressure cooker and humidity life tests) and mechanical tests, including those for intermittent operating life and thermal shock. Solderability testing is performed on a regular sample basis. Individual process data is available on request.

Test	MIL-S-750 Method	Test Conditions	Unit Hours	Number of Failures	Failure Rate in FITs[1, 2]	MTBF[1, 2] (hours)
High-Temperature Storage	1031.4	$T_A = +150°C$ 1000 hours	4.42×10^6	4	1187	8.42×10^5
Steady-State Operating Life	1026.3	$T_A = +25°C$ 1000 hours $P_D = 350$ mW $V_{CB} = 0.8\ V_{(BR)CEO}$	5.23×10^6	5	1205	8.30×10^5
High-Temperature Reverse Bias		$T_A = +125°C$ 1000 hours $V_{CB} = 0.8\ V_{(BR)CEO}$	8.10×10^6	12	1680	5.95×10^5
Pressure Cooker		15 psig $T_A = +115°C$ 96 hours	5.57×10^5	3	7511	1.33×10^5
Humidity Life Test		$T_A = +85°C$ Rel. Hmd. = 85%	5.03×10^6	3	831	1.20×10^6
Intermittent Operating Life	1036	$T_A = +25°C$ 1000 hours $P_D = 350$ mW $V_{CB} = 0.8\ V_{(BR)CEO}$ $t_{on} = 120$ s $t_{off} = 120$ s	3.81×10^6	2	817	1.22×10^6

NOTES: 1. For confidence level of 60%.
2. Cumulative rate (includes infant mortalities).

SECTION 9. PACKAGE INFORMATION

PACKAGE INFORMATION

PACKAGE THERMAL CHARACTERISTICS

Allegro Package Code	Package Type (Common Package Designators)	Qty-Type of Terminals	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
A	Plastic Dual In-Line (DIP or PDIP)	14-Pin	60	38
		16-Pin	60	38
		18-Pin	60	25
		20-Pin	55	25
		22-Pin	50	21
		28-Pin	45	16
		40-Pin	36	—
B	Semi-Tab Plastic Dual In-Line (DIP or PDIP)	8-Pin	60	6*
		14-Pin	45	6*
		16-Pin	43	6*
		22-Pin	40	6*
		24-Pin	40	6*
EA	Semi-Tab Plastic Leaded Chip Carrier (PLCC or PQCC)	28-J Lead	40	6*
		44-J Lead	—	6*
EB	Semi-Tab Plastic Leaded Chip Carrier (PLCC or PQCC)	28-J Lead	36	6*
		44-J Lead	30	6*
EP	Square Plastic Leaded Chip Carrier (PLCC or PQCC)	20-J Lead	59	35
		28-J Lead	55	30
		44-J Lead	46	25
JT	Low-Profile Quad Flatpack (L-PQFP)	64-Lead	42†	—
K	Plastic Single In-Line (SIP or PSIP)	4-Lead	177	—
KA	Plastic Single In-Line (SIP or PSIP)	5-Lead	164	—
L	Plastic Small-Outline Transistor (SO or SOT)	3-Gull Wing	575	—
	Plastic Small-Outline IC (SO, SOIC, or SOL)	8-Gull Wing	108	45
		14-Gull Wing	95	33
LB	Semi-Tab Plastic Small-Outline IC (SO, SOIC, or SOL)	16-Gull Wing	67	6*
		20-Gull Wing	60	6*
		24-Gull Wing	55	6*
LL	Plastic Long-Leaded Small-Outline Transistor (SO or SOT)	3-Lead	258	—

* $R_{\theta JT}$

† Mounted on 2.5" x 3.5" (63.5mm x 89mm) multilayer board.

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

PACKAGE THERMAL CHARACTERISTICS

Allegro Package Code	Package Type (Common Package Designators)	Qty-Type of Terminals	$R_{\theta JA}$ (°C/W)	$R_{\theta JC}$ (°C/W)
LW	Wide-Body Plastic Small-Outline IC (SO, SOIC, or SOL)	16-Gull Wing	80	—
		18-Gull Wing	80	—
		20-Gull Wing	70	17
		28-Gull Wing	66	—
M	Mini Plastic Dual In-Line (DIP or PDIP)	8-Pin	80	55
U	Plastic Mini Single In-Line (SIP)	3-Lead	184	—
UA	Plastic Ultra-Mini Single In-Line (SIP)	3-Lead	206	—
W	Power-Tab Plastic Single In-Line (SIP)	12-Lead	36	2*
		18-Lead	28	9*
—	Plastic Transistor (TO-92/TO-226AA)	3-Lead	200	—
Z	Power-Tab Plastic Single In-Line (SIP)	3-Lead	67	3*
		5-Lead	65	3*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specification takes precedence.

* $R_{\theta JT}$

PACKAGE INFORMATION

THERMAL DESIGN FOR PLASTIC INTEGRATED CIRCUITS

Proper thermal design is essential for reliable operation of many electronic circuits. Under severe thermal stress, leakage currents increase, materials decompose, and components drift in value or fail. Present-day linear integrated circuits are capable of delivering 5 to 10 watts of continuous power. Previously, such power levels came only with discrete metal can power transistors. It was relatively easy to determine the thermal resistance of these devices and attach a massive heat sink. However, in many markets, economic factors now dictate the use of molded dual in-line plastic packaged monolithic circuits. The guidelines to be discussed will provide the circuit design engineer with information on maintaining junction temperature below a safe limit under worst case conditions.

DESIGN CONSIDERATIONS

Four factors must be considered before the required heat-sinking can be determined. These are:

1. Maximum ambient temperature

2. Maximum allowable chip temperature

3. Junction-to-ambient thermal resistance

4. Continuous chip power dissipation

Maximum ambient temperature for the integrated circuit is normally between +70°C and +85°C and is usually dependent on the case material. In most applications, however, the limiting factor is the associated discrete components and a limit of about +50°C is specified. The maximum allowable chip temperature is usually +150°C for silicon.

Thermal resistance is the all-important design factor. It is composed of several individual elements, some of which are determined by the integrated circuits manufacturer, and some by the user.

CHIP POWER DISSIPATION

The chip power dissipation should be obtainable from the manufacturer's specifications. In most applications it is a variable and determined by the user when he specifies the circuit variables.

HEAT DISSIPATION

In any circuit involving power, a major design objective is to reduce the temperature of the components in order to improve reliability, reduce cost, or improve operation. The logical place to start is with the heat-producing component itself. First, keep the amount of heat

generated to a minimum. Second, get rid of the heat that must be generated.

Heat generation can be minimized through proper circuit design. Heat dissipation is a function of thermal resistance.

With the typical discrete component, heat dissipation can be accomplished by fastening it directly to the chassis. Dual in-line plastic packaged integrated circuits, however, are quite a bit different. Their shape is not conducive to fastening directly to the chassis, they are normally installed in a plastic socket or on a printed wiring board, and the heat producing chip is not readily accessible.

Some users specify unusual packages so as to get the heat sink as close as possible to the chip and/or provide an attachment point for an external heat sink. A common factor in many of these special designs is that the lead frame is an integral part of the heat sink.

Since the plastic package may have a thermal resistance of between 50 and 100°C/W and the lead frame a thermal resistance of only 10 to 20°C/W, this would seem like the best route to go.

STANDARD PACKAGES

The most common lead frame material has been Kovar (an iron-nickel-cobalt alloy). Its coefficient of expansion is close to that of silicon thereby minimizing mechanical stresses. However, Kovar has a relatively high thermal resistance and consequently is not suitable for standard lead frames in high power dissipation circuits. For these applications, copper or copper-alloy lead frames should be used. Additionally, some type of added heat sinking may be necessary. Thus lead frame configurations are being altered from the standard 14-pin or 16-pin designs.

Rapidly becoming an industry standard is the "bat-wing" package. This package is the same size as a dual in-line package, but the center portion of the frame is left as tabs. These tabs can be soldered to a heat sink or inserted directly into a socket. The worst case thermal resistance of various lead frames ($R_{\theta JC}$) is given below.

Lead Frame	Thermal Resistance
14-pin Kovar	47°C/W
14-pin copper	38°C/W
"Bat-wing"	13°C/W

WHICH HEAT SINK?

If the integrated circuit manufacturer has done his job well, the chip-to-ambient thermal resistance wil be minimized for maximum chip power dissipation. It would appear that even the Kovar lead frame would be adequate for most applications. However, the total thermal resistance ($R_{\theta JA}$) is also dependent on a stag-nant layer of air at the lead frame-ambient interface which will suport a temperature gradient. The total thermal resistance of a non-heat sinked dual in-line plastic package is therefore much higher. Since air is a natural thermal insulator, maximum heat transfer is through convection and the total thermal resistance will decrease some at high power levels.

Lead Frame	Total Thermal Resistance	Max. Power Diss. (W) at 50°C T_A, 150°C T_J
14-Pin Kovar	120°C/W	0.83
14-Pin Copper	60°C/W	1.67
"Bat-Wing"	45°C/W	2.22

Ignoring any safety margin and device performance, even the "bat-wing" is now only barely adequate for many power driver applications. The obvious solution is the use of an external heat sink.

Actual performance in a specific situation depends on factors such as the proximity of objects interfering with air flow, heat radiated or convected from other components, atmospheric pressure, and humidity. A good safety factor is therefore in order.

Heat sinks for plastic dual in-line packages can be of almost unlimited variety in design, material, and finish. Economics will normally play a very important role in the selection of any heat sink.

The least expensive and easiest to fabricate heat sink is the plain copper sheet. It is also very effective in reducing the total thermal resistance. The necessary dimensions can be obtained from Figure 1. These heat sinks are square in geometry, 0.015 inches thick, mounted vertically on each side of the lead frame, and with a dull or painted surface (Figure 2). The heat sinks should be soldered directly to the lead frame (approximately 0.3°C/W interface thermal resistance)

The plain copper sheet heat sink is also available commercially and may be less expensive than in-house manufacture. Two standard types are the Staver V7 and V8.

HEAT SINK FINISHES

The most common finish is probably black anodizing. It is economical and offers a good appearance. The black finish will also increase the performance of the heat sink, due to radiation, by as much as 25%. However, since anodizing is an electrical and thermal insulator, the heat sink should have an area free of anodize where the heat-generating device is attached.

Other popular finishes for heat sinks are irridite and chromic acid dips. They are economical and have negligible thermal and electrical resistances. These finishes, however, do not enjoy the 25% increase in performance that a dull black finish has.

FORCED AIR COOLING

The performance of many heat sinks can be increased by as much as 100% by forcing air over the fins. Where space is a problem, the cost of a small fan can often be justified. If a fan is required for other purposes, it is advantageous to place the semiconductor heat source in the air flow. A rule-of-thumb is that semiconductor failure rate is halved for each 10°C reduction in junction operating temperature.

CHIP DESIGN

Proper thermal design by the integrated circuit user can reduce the operating temperature of the semiconductor junction. However, the minimum chip temperature at any power level is determined solely by the device manufacturer. For this reason, care must be taken in choosing the manufacturer. "Exact equivalent" integrated circuits are not necessarily identical. Electrically and mechanically they may be the same, but thermal differences can mean that "identical" audio power amplifiers will not put out the same power without exceeding the rated junction temperature.

The circuit manufacturer must optimize his chip design so that component drift is minimized and/or equalized so that rated

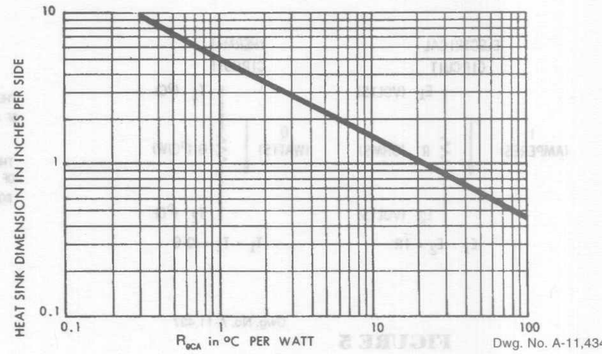


FIGURE 1

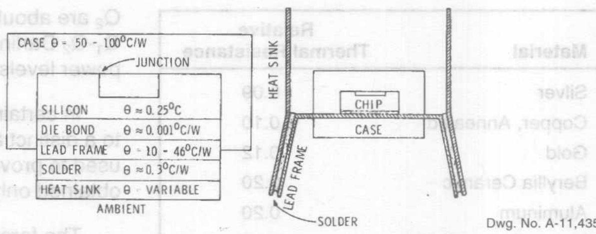


FIGURE 2

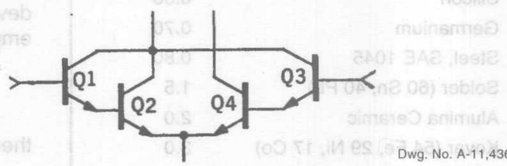


FIGURE 3

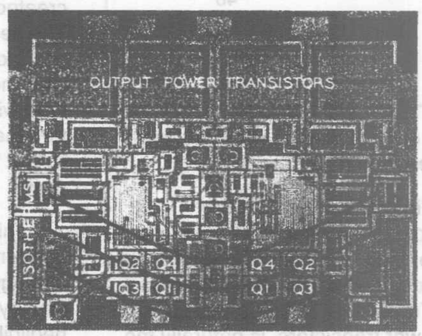


FIGURE 4

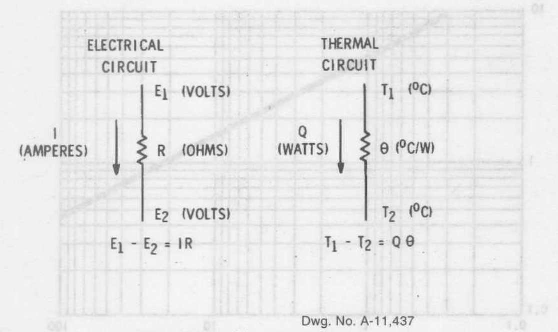


FIGURE 5

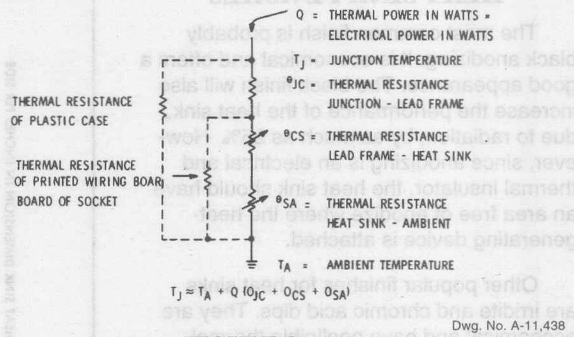


FIGURE 6

Material	Relative Thermal Resistance
Silver	0.09
Copper, Annealed	0.10
Gold	0.12
Beryllia Ceramic	0.20
Aluminum	0.20
Brass (66 Cu, 34 Zn)	0.40
Silicon	0.50
Germanium	0.70
Steel, SAE 1045	0.80
Solder (60 Sn, 40 Pb)	1.5
Alumina Ceramic	2.0
Kovar (54 Fe, 29 Ni, 17 Co)	3.0
Glass	40
Epoxy	40
Mica	50
Teflon PTFE	200
Air	2000

performance can actually be obtained under maximum thermal stress.

Note in Figures 3 and 4 that the Darlington input differential pairs are cross-connected so as to minimize differences in gain as a function of output transistor power dissipation. Transistor Q_4, being closest to the output power transistors, is naturally the hottest; Q_3 is a degree or two cooler; Q_1 and Q_2 are about equal and midway between Q_3 and Q_4. The gain of the Q_1-Q_2 Darlington pair is about equal to the gain of Q_3-Q_4 at all output power levels because of careful thermal design.

In certain specialized applications, thermal coupling can be used to a distinct advantage. Experimentally, thermal coupling has been used to provide a low-pass feedback network which otherwise could be obtained only with very large values of capacitance.

The foregoing discussion has covered the average thermal characteristics of dual in-line plastic integrated circuits. The specific devices will vary with the different packages and bonding techniques employed, but the concepts will remain the same.

APPENDIX

The following is intended to review terminology and compare thermal circuits with the more familiar electrical quantities.

The first law of thermodynamics states that energy cannot be created or destroyed but can be converted from one form to another. The second law of thermodynamics states that energy transfer will occur only in the direction of lower energy. In the semiconductor junction, the electrical energy is converted to thermal energy. Since no heat will be stored at the junction, the heat will flow to a lower temperature medium, air. The rate of heat flow is dependent on the resistance to that flow and the temperature difference between the source and the sink.

This thermal electrical analogy is convenient only for conduction problems where heat flow and temperature obey linear equations. The analogy becomes much more complex for situations involving heat flow by convection and radiation. Where these two modes are not negligible, they can be approximated by an equivalent thermal resistance. If ignored, the error introduced will only improve the device reliability.

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

ABSTRACT

A new, high-performance version of a Plastic Dual-In-Line package with improved reliability levels has been developed for high-power integrated circuit industrial and automotive applications. Superior thermal capability and reliability performances have been achieved with no increase in manufacturing cost or change in package outline.

The development of this package is based on a package optimization approach. Development methodology and package characterization results will be outlined. Data for production lots of the package show a thermal performance improvement of up to 35 percent compared with currently available packages, without the aid of an external heat sink. Furthermore, qualification test results indicate that this new package has an excellent reliability performance and its long-term survival exceeds the industry standard requirements. An improvement by a factor of 4 in the resistance to device metal deformation and a factor of 7 in wire-bond thermal fatigue has been achieved as a result of reducing the shear and normal stresses inside the package by proper selection of a state-of-the-art low modulus molding compound and optimizing the leadframe design. In addition, new design fundamentals will be briefly discussed.

This paper was presented at the 39th Electronic Components Conference, Houston, TX, May 22-24, 1989.

INTRODUCTION

As the maturation of power integrated circuit technologies continues to promise more miniaturization of power electronic systems, the role of package thermal management is becoming critical. Since the present power packaging technology lags sharply behind the chip technology, the device performance and its reliable operation can be described to a great extent as limited by the package thermal capability. This paper presents the results of a package design study, which employs a "package optimization approach." The package chosen for this study is the 16-lead web-DIP, class of Plastic Dual-In-Line-Package (PDIP), which was specifically developed for medium- to high-power applications. An important practical feature of the web-DIP is that it costs no more to produce than a conventional DIP.

The initial phase of this program is a comparative analysis, based on package thermal and physical evaluations. Five variations of power DIP packages from major power integrated circuit manufacturers were evaluated. The evaluation results indicate that packages presently available are still far from optimum, thus making further improvements a feasible goal. In parallel to the comparative analysis, three-dimensional finite-element models are constructed to simulate and analyze the expected thermal performance of the design under study. The projected configuration is also analyzed thermostructurally to examine the mechanical behavior of the new packaging system, prior to implementation. The reliability improvement of the new package is based on optimization of the leadframe design, and the proper selection of materials. The package reliability design is aimed at improving wire fatigue life and device metal deformation resistance during temperature cycling. In addition, the study provides a new insight into this type of package and new design principles that can be extended to packages of similar internal configuration, such as power surface-mount packages.

OPTIMIZATION STRATEGY

PDIP's are still the most common package option for high-volume IC production, due to their established manufacturing and handling, and their low cost. However, there are two different types of PDIP's. The first is the standard type in which the chip pad is not attached to any of the internal leads (Fig. 1(a)), and which is mainly used for low-power applications. The second is a modified form of the standard type in which the central leads are tied in pairs and connected with the paddle, forming one piece (Fig. 1(b)). This unconventional configuration has been employed to improve the package thermal performance, mainly by enhancing the conduction heat transfer mechanisms by

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

allowing the chip to be cooled directly by means of these four leads which are soldered to a board. This design format has made such a package suitable for medium-power applications up to 2.5 W in natural convection. Also, if the chip pad is extended to the outside of the package forming a web shape (Figure 1(c)), a miniature heat sink can be soldered to the web for even higher power dissipation.

WEB-DIP DESIGN

Although there are several extensive studies concerning thermal performance and reliability of standard PDIP's [1]-[4], there have been no similar efforts directed towards its web version. However, we felt that a new insight should be gained and established for the web-type package for the following reasons:

(1) The power dissipation capability of the package is greatly influenced by the web concept, which dramatically changes the temperature fields inside the package. Consequently, all of the previously identified thermal paths for standard packages are affected, and their relative thermal contributions are altered.

(2) It has been demonstrated that converting from the standard package to the web-type package has led to an improvement of the package power handling capability by 70 percent. For example, a 1-W standard package can dissipate 1.7 W instead by tying its four central leads to the chip pad. However, our observations, as will be described later, indicate that some package designers have conflicting views about the thermal merits of the concept compared with other paths. This limited understanding as to the precise relationship between the web and other leadframe parameters has cost some manufacturers a great thermal penalty, as will be explained in the next section.

(3) The mechanical configuration of the leadframe and its physical behavior within the package during assembly, testing, and operation has introduced a considerable amount of uncertainty involving the package component structural responses and long- term reliability.

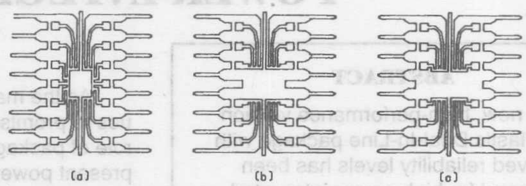


FIGURE 1

16-Lead PDIP leadframes (a) standard (b) unconventional (c) unconventional-web

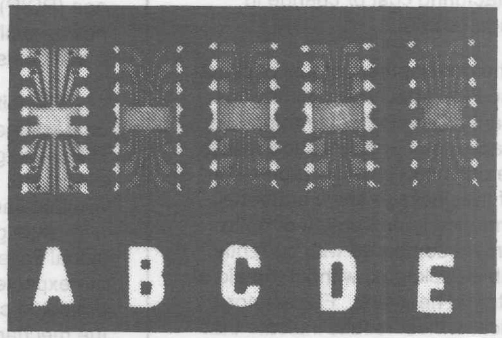


FIGURE 2

Leadframe designs for five different PDIP manufacturers

(4) Since this concept is being extended to new package families, notably PLCCs and SOICs, to improve their thermal performance, new safe design limits are required, particularly when these packages have not been completely perfected.

COMPARATIVE ANALYSIS

The primary purpose of this analysis was to assess the thermal performance of the industry state-of-the-art power DIP packages made by leading IC manufacturers. This performance evaluation enabled us to gain knowledge about the range of the thermal capabilities of existing packages and to establish an optimization target. Figure 2 shows the leadframe design of the examined packages.

Representative packages from five major companies including our targeted package were chosen for this study based on device perfor-

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

TABLE I

16-LEAD DIP THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)

Manufacturer	$R_{\theta JA}$ (°C/W) at 150°C T_J
A	47
B	51.5
C	52
D	55
E	59

mance equivalents and similarity of package outlines.

Steady-state thermal resistance of the packages was measured in still air under the same conditions at different power levels, using the Temperature Sensitive Parameters (TSP) method. During the measurements, packages were mounted individually by soldering to a printed circuit board that was oriented vertically and housed in a 1-ft.³ plexiglas sealed enclosure. Measurements were taken with the aid of a Sage model Theta 400A thermal resistance tester. Results of the measurements of the thermal resistance from junction to ambient, $R_{\theta JA}$ are presented in Table I. The manufacturers are listed in ascending rank, based on their package performances.

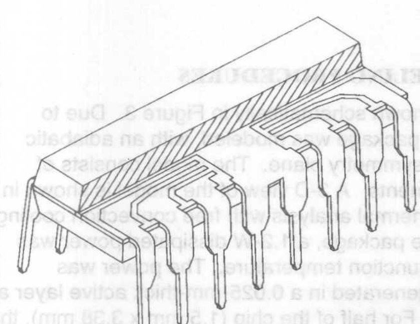


FIGURE 3

Web 16-lead PDIP

The next step of the analysis was to correlate these thermal resistances to their packaging systems. For this purpose, a construction analysis was performed. The results of the construction examination are summarized in Table II. The material analysis has been performed with the aid of a SEM equipped with an EDAX analyzer. Although it is not the intent of this study to critique these packages, the following discussion is in order.

WORST PERFORMANCE

Manufacturer E, whose package shows the highest thermal resistance, uses a very high thermal conductivity leadframe material which is identified as "silver-bearing copper." Its conductivity is 35 percent higher than that of Copper Alloy C194, used by other manufacturers. One might therefore expect that the package thermal resistance, $R_{\theta JA}$, would be lower than that of other packages employing C194 leadframes. However, as is indicated in Table I, this is not the case. The main reason is that the leadframe design has left out the tie bar. As a result, a dramatic increase in $R_{\theta JA}$ occurs, which is not compensated for by the higher conductivity leadframe. To verify this, an experiment was run with packages assembled using copper alloy C151 leadframes, whose conductivity is 25 percent higher than that of C194 leadframes. The tie bar was removed from some of these packages. Thermal resistance measurements showed that in natural convection cooling the leadframe material and the tie bar make separate contributions to $R_{\theta JA}$. First, despite the substitution of C194 material by C151, only about a 2.5°C/W improvement in $R_{\theta JA}$ is gained. The reason for this is that the package external resistance, $R_{\theta CA}$ (where C refers to both the package and lead surfaces) is the pre-dominant resistance, and is more than 75 percent of the package total resistance in still air. This $R_{\theta CA}$ has less dependency on the leadframe material [4], and is mainly a function of the motion and temperature of the boundary layers that exist on the package and the external lead surfaces. Second, packages with tie bar show a 6°C/W improvement in $R_{\theta JA}$ over packages assembled without a tie bar. Therefore, we conclude that the leadframe thermal conductivity has a minor effect on $R_{\theta JA}$, while the tie bar has a greater influence. This is due to its multiplying effect on heat distribution within the package to the adjacent leads as well as heat spreading to both the top and bottom surfaces of the packages, resulting in an additive thermal enhancement by conduction and convection. The same effect was also verified analytically, as will be discussed later.

BEST PERFORMANCE

Manufacturer A, whose package exhibits the lowest thermal resistance shown in Table I, employed the same high-conductivity leadframe material used by manufacturer E, but did not remove the tie bar. In addition, manufacturer A increased the leadframe thickness to 15 mils from the standard 10 mils. To evaluate the impact of the leadframe thickness on the package power handling capability, packages assembled with C194 and C151 leadframes with 10-, 12-, and 15-mil thickness were evaluated. Results of thermal resistance mea-

TABLE II

16-Lead DIP CONSTRUCTION ANALYSIS

Manufacturer	Leadframe Material	Leadframe Thickness (mm)	Chip Thickness (mm)	Die-Attach Material	Gold Wire Diameter (mm)	Leadframe Design (Refer to Fig. 1)
A	Silver-Bearing Copper	0.375	0.250	Solder	0.0375	(b)
B	Copper Alloy C-194	0.250	0.350	Silver Epoxy	0.0375	(c)
C	Copper Alloy C-194	0.250	0.450	Silver Epoxy	0.0375	(c)
D	Copper Alloy C-194	0.250	0.250	Silver Epoxy	0.375	(c)
E	Silver-Bearing Copper	0.250	0.350	Silver Epoxy	0.325	(b)

surements in still air are summarized as follows:

(1) $R_{\theta JA}$ for packages assembled with 10-mil C151 leadframes was 2.5°C/W lower than those assembled with 10-mil C194 leadframes.

(2) Packages assembled with 12- and 15-mil C151 leadframes showed an improvement in their $R_{\theta JA}$ by 3.5 and 7°C/W respectively over packages with 10-mil C151 leadframes.

Thus it is concluded that a thicker leadframe reduces the package heat spreading resistance and enhances the package surface thermal properties that result in improved thermal exchange between the package surfaces and their immediate surrounding air layers. As a result, $R_{\theta CA}$ is also reduced.

THERMAL MODELING

FINITE ELEMENT PROGRAM

In parallel to the comparative analysis, numerical solutions for a steady-state thermal model were obtained by using the finite element program, ANSYS. A three-dimensional (3-D) model for a typical web-16-lead package was first constructed as a reference model to simulate the thermal performance of a standard web-16-lead DIP for a typical package system. Parametric changes were then applied to the model to determine the best variable combinations which can be implemented to optimize the package power dissipation, while maintaining a constant junction temperature of 150°C. Major variables investigated in this study were:

1 - leadframe material
2 - leadframe thickness
3 - tie bar size and layout
4 - lead lock hole size
5 - leadframe design, (web design versus internal termination), see Figures 1(b) and (c)
6 - die attach material
7 - die pad area

MODELING PROCEDURES

A typical web-DIP is shown schematically in Figure 3. Due to symmetry, only half of the package was modeled, with an adiabatic boundary condition at the symmetry plane. The model consists of 3032 nodes and 2270 elements. A 3-D view of the model is shown in Figure 4. A steady-state thermal analysis with free convection cooling is assumed. For half of the package, a 1.2-W dissipated power was used to simulate a 150°C junction temperature. The power was assumed to be uniformly generated in a 0.025-mm-thick active layer at the top of the silicon chip. For half of the chip (1.5 mm x 3.38 mm), the power was specified as heat generation per unit volume (9.49 W/mm^3). The surfaces of the package and the external leads were assumed to have a convective heat transfer coefficient of 0.00001 W/mm^2°C. Table III shows the materials properties that were used in the analysis.

HIGH-PERFORMANCE POWER PACKAGE FOR POWER-INTEGRATED CIRCUIT DEVICES

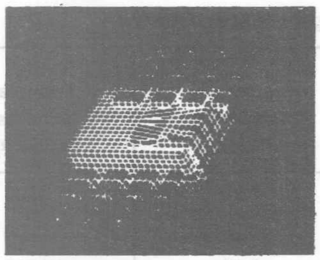


FIGURE 4

16-Lead DIP finite element model (3-D view)

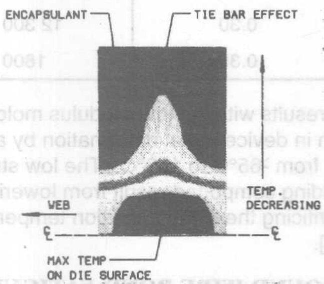


FIGURE 5

Temperature distribution on the die surface

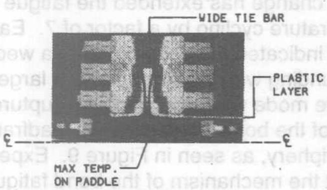


FIGURE 6

Temperature distribution across the leadframe surface

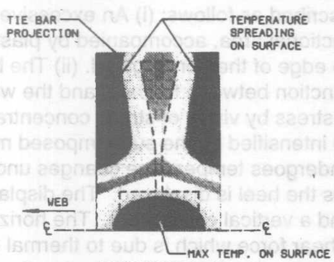


FIGURE 7

Temperature distribution on the package top surface

MODELING RESULTS AND DISCUSSION

Reference Model: The temperature distribution across the chip active layer is shown in Figure 5. The individual roles of the web and the tie bar in the package thermal performance are illustrated in Figure 6. It can be seen from Figure 6 that the web represents the primary thermal path in the transverse direction to the chip, where heat is directly conducted down through the chip pad out of the package to the connected protruding leads and dissipated into the board by conduction and to the air by convection and radiation. Also, it can be seen that the major remaining thermal barrier inside the package is the plastic layer between the chip edge and the lead tips, while the tie bar has a multiplying effect in dissipating and spreading heat to the adjacent leads and top and bottom surfaces of the package, as illustrated in Figures 6 and 7. Therefore, to achieve an effective thermal design, the plastic layer should be minimized and a massive tie bar utilized.

Parametric Study: For this analysis, the power generated in the active layer is held fixed and the junction temperature allowed to vary, while variables are applied. The results and conclusions of this parametric study are summarized as follows: (i) In natural convection cooling, for high-conductivity leadframe material, $R_{\theta JA}$ has a minor dependency on the material thermal conductivity. An increase in thermal conductivity of 25 percent yields an 8 percent decrease in $R_{\theta JA}$. The leadframe thickness is of somewhat greater influence, yielding a 10 percent decrease in $R_{\theta JA}$ for only a 20 percent increase in thickness. Both $R_{\theta JC}$ and $R_{\theta CA}$ are decreased, due to the massive size of the thicker frame and its effect of reducing the package internal resistance and improving the convection mechanism. (ii) The tie bar is critical to the package thermal performance even in the presence of the web feature because of its contribution in directing the heat flow throughout the package and disseminating heat to the package surfaces. Therefore, the package designer should not be tempted to remove it from the leadframe. (iii) Extending the chip pad outside the package has a thermal contribution. A 1.6°C/W increase in $R_{\theta JA}$ was found when the web had been removed and the paddle was terminated inside the package as in the case of package type in Figure 1 (b). (iv) Lead lock holes of 0.2 mm² each have no effect on the package thermal performance if they are placed on all the leads except the four central leads. (v) An improvement in $R_{\theta JA}$ of only 1.2°C/W was achieved by changing the die-attach material from epoxy to solder, despite the large difference in their conductivities. This is attributed to the very small thickness of this layer. (vi) For a given chip, $R_{\theta JA}$ is insensitive to the increase in the die pad area beyond a critical dimension, since any increase in the paddle area in the longitudinal direction is accompanied by moving the lead tips away from the chip edge which results in increasing the plastic thickness between the chip and the leads, thus, increasing lead resistance. Complete numerical data are summarized in Figure 8. The accuracy of these data is within 10 percent of the experimental results.

TABLE III

MATERIAL PROPERTIES OF 16 LEAD-PDIP PACKAGE COMPONENTS

Material	Thermal Conductivity (W/mm • °C)	Thermal Expansion Coefficient (10^{-6}/°C)	Poisson's Ratio	Young's Modulus (kg/mm^2)
Molding compound	0.75×10^{-3}	19	0.30	1500
Leadframe, C194	0.263	17	0.30	12 300
Silicon	0.140	2.4	0.28	17 000
Epoxy adhesive	0.004	20	0.30	6000
Leadframe, C151	0.331	17	0.30	12 300
Solder die attach	0.025	29	0.35	1800

Based on these data, we have predicted that a potential improvement in the package thermal performance of 25 percent could be achieved over our targeted package. It is also estimated that the proposed package could achieve a 40 percent increase in power dissipation capability over the worst case. Consequently, we decided to develop a new leadframe to meet the absolute targeted thermal improvement with the following characteristics: (i) optimum configuration, (ii) higher thermal conductivity copper C151, and (iii) increased thickness, 0.375 mm compared to the standard 0.25 mm thickness. The reliability aspects of the new package are detailed in the reliability improvement and in the thermostructural modeling sections.

RELIABILITY IMPROVEMENT

Although the package thermal enhancement seems to be the principal driving force for this program, package reliability improvement has been an intrinsic part of the package optimization strategy. For example, two separate studies recommended the use of (i) a new epoxy die-attach adhesive for its effectiveness in reducing the amount of voids and improving the die shear resistance, and (ii) a new state-of-the-art low modulus molding compound which has proven its contribution in reducing the shear force on the die surface. Experimental results with the low-modulus molding compound showed a reduction in device metal deformation by a factor of 4, after temperature cycling from -65°C to 150°C. The low stress characteristics of this new molding compound result from lowering its Young's modulus, without sacrificing the glass transition temperature for the finished product. [5], [6].

MECHANISM OF GROUND WIRE BOND FATIGUE AND RELIEF

A novel leadframe design change has extended the fatigue life of grounding wires during temperature cycling by a factor of 7. Earlier temperature cycling tests had indicated the occurrence of a wedge bond (heel), failure of the grounding wire that is used for a large number of devices. The failure mode was identified as a rupture or fracture occurring at the heel of the bond located on the leadframe, particularly on the die pad periphery, as seen in Figure 9. Experimental observations indicated that the mechanism of the bond fatigue failure is plastic flow and rupture in the heel area induced by cumulative cyclic strain during thermal fluctuations. The identified failure mechanism can briefly be described as follows: (i) An excessive reduction in the heel cross-sectional area, accompanied by plastic deformation, is caused by the edge of the bonding tool. (ii) The bond knee, which represents the junction between the heel and the wire span, sustains high localized stress by virtue of stress concentration effects. (iii) This stress will be intensified by the superimposed molding stress. (iv) As the package undergoes temperature changes under temperature cycling conditions the heel is displaced. The displacement has both a horizontal and a vertical component. The horizontal component results from the shear force which is due to thermal coefficient mismatch between the molding compound and the leadframe, while the vertical component results from the molding compound normal stress. (v) Due to very low yield strength and high ductility of

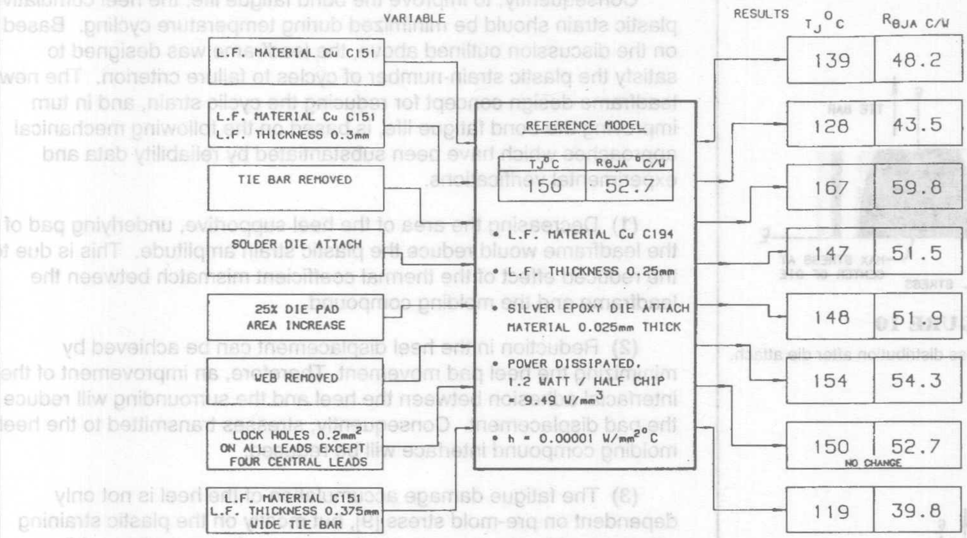


FIGURE 8

Numerical results of 3-D finite element analysis.

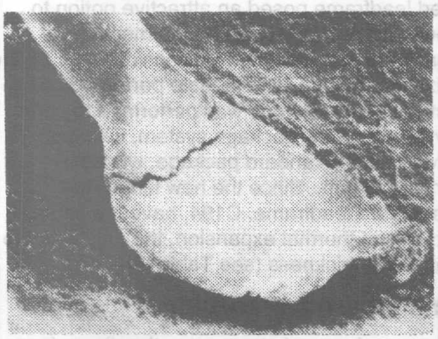


FIGURE 9

Wire heel damage after 1000 temperature cycles.

the gold wire, the displacement will produce a large amount of plastic strain, i.e. permanent deformation, at the knee for each temperature cycle. This plastic strain will accumulate during the course of the temperature cycling. (vi) In addition, during the high-temperature part of the cycle, a significant reduction in the gold yield strength could occur and the wire can behave as a perfectly plastic material [7] which will yield a very large cyclic strain at the knee and the molding compound interface. (vii) As the plastic straining continues and the cumulative magnitude of cyclic plastic strain reaches critical value (gold fracture strength), the heel will rupture at the knee and a fatigue crack can initiate, marking the beginning of the bond failure.

Analysis of experimental data suggested that the bond failure during temperature cycling is a function of heel strain. As a result, it was inferred that the bond fatigue life or number of cycles to failure can be expressed by the Coffin Law [8]

$$\Delta e_p = C/\sqrt{N}$$

where

Δe_p = cumulative plastic strain

N = number of cycles to failure

C = constant.

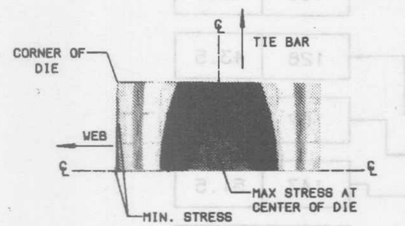


FIGURE 10

Die surface tensile stress distribution after die attach.

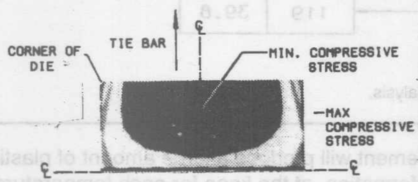


FIGURE 11

Die surface compressive stress distribution after die molding.

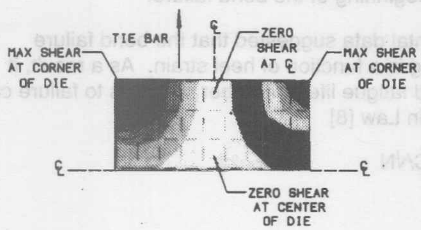


FIGURE 12

Die surface shear stress distribution after molding.

Consequently, to improve the bond fatigue life, the heel cumulative plastic strain should be minimized during temperature cycling. Based on the discussion outlined above, the leadframe was designed to satisfy the plastic strain-number of cycles to failure criterion. The new leadframe design concept for reducing the cyclic strain, and in turn improving the bond fatigue life, is based on the following mechanical approaches which have been substantiated by reliability data and experimental verifications.

(1) Decreasing the area of the heel supportive, underlying pad of the leadframe would reduce the plastic strain amplitude. This is due to the reduced effect of the thermal coefficient mismatch between the leadframe and the molding compound.

(2) Reduction in the heel displacement can be achieved by minimizing the heel pad movement. Therefore, an improvement of the interfacial adhesion between the heel and the surrounding will reduce the pad displacement. Consequently, stresses transmitted to the heel-molding compound interface will be reduced.

(3) The fatigue damage accumulation of the heel is not only dependent on pre-mold stress [9], but mostly on the plastic straining effects resulting from mechanical interaction between the molding compound and the configuration of the underlying pad.

THERMOSTRUCTURAL ANALYSIS

Although the proposed leadframe posed an attractive option to augment the package power dissipation capability, its mechanical compatibility with other package components was considered to be the key factor for its final utilization for long-term reliable performance. Therefore, a thermostructural analysis study was performed to compare the structural behavior of the new package system, with the thicker C151 leadframe, versus the standard package, whose leadframe thickness is only 0.25 mm. Since the new leadframe material, C151, and the standard leadframe, C194, have the same elastic moduli and coefficients of thermal expansion, the only variable considered in the analysis is the thickness (see Table III).

3-D FINITE ELEMENT MODELING

As the state of the shear and normal stresses on the die surface are of prime reliability concern, due to their role in device passivation cracking and metal deformation [10]-(12], they were analytically investigated after the die attach and molding processes. Only the web feature is considered, since the tie bar and other leads do not significantly affect the package system during these two processes. The following assumptions are made: (1) linear elastic analysis, (2) isotropic materials, (3) zero stress at or above the glass transition temperature of die attach adhesive and molding compound.

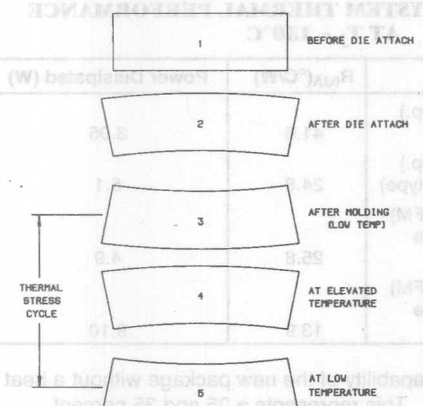


FIGURE 13
Die thermal stress fatigue model.

Die Attach Process: The modeling results show that for both assemblies, with two different leadframe thicknesses, the maximum normal stress on the die surface is tensile and occurs at the center of the chip. Figure 10 shows the tensile stress distribution on the die surface. It can be seen that the stresses gradually decrease towards the chip edges. Though the stress distributions on the die surface are identical in shape for both assemblies, they are different in magnitude. Assembly with the 0.25 mm thick leadframe produced 11.5 kg/mm^2 while assembly with the 0.375 mm thick leadframe produced 10.0 kg/mm^2. The model shows no shear stress on the die surface, which is expected since the surface is in pure bending. However, the chip maximum deflection at the center was 0.92 x 10^{-2} mm and 0.80 x 10^{-2}mm for thinner and thicker leadframes, respectively. This particular finding suggests that using a thicker leadframe in the assembly will produce lower die deflection which, in turn, can lead to a higher resistance to thermal cyclic fatigue during temperature changes that will be elaborated on later in reference to the thermal cyclic model.

Molding Process: Figure 11 shows the stress contours on the die surface at the end of the molding and cure process. Zero stress conditions were assumed at T_g = 155°C. The whole surface is seen to be under compressive stress, with maximum stress concentrated on the die edges parallel to the longitudinal axis and on the corners. The compressive stress distributions are similar for both assemblies but different in magnitude. Assembly with the 0.25 mm thick leadframe yielded 19.5 kg/mm^2 stress on the chip corners, while assembly with the 0.375 mm thick leadframe yielded only 16.5 kg/mm^2. A 15 percent reduction in stress on the chip corners is achieved by using a thicker leadframe in the package. In addition, the die surface shear stress is 12 percent lower for 0.375 mm thick leadframe. The shear stress distribution on the chip surface is the same for both assemblies. As shown in Figure 12, the maximum shear is concentrated on the chip corners and exponentially decreases to zero at the center of the die. [13]

In summary, these comparative results show that the 0.375 mm thick leadframe could be better than the 0.25 mm thick leadframe because (i) the permanent *in-situ* normal and shear stresses produced on the chip surface as a result of either the die attach or the molding processes are lower, (ii) the temperature dependence of the die surface stress is lower, and (iii) the maximum die deflection is also lower. These theoretical findings highlight the potential contribution that the leadframe thickness would have in reducing thermal-fatigue damage and vulnerability of the die to stress caused by temperature changes. To explain this, the following model is postulated.

DIE THERMAL FATIGUE MODEL

At the beginning of the molding process, the die surface is completely under tensile stress, as depicted in Figure 13. At the end of the molding process, at room temperature, the stress reverses to a com-

pressive stress If the package system is heated again to a higher temperature the compressive stress will reverse to a tensile stress. This reversible process is repeated whenever the package is exposed to temperature excursions, causing the die to deflect in a butterfly-like movement. [14] The reversible deflection is further aggravated by the effects of the superimposed shear force which eventually will lead to a combined vertical and horizontal thermal cyclic strain, particularly on the edges and corners of the die. Ultimately, microcracks will start to grow in the passivation layer. Subsequently, the device metal deformation will initiate.

Based on the analysis of the experimental and analytical results and the model proposed above, we inferred that a lower failure rate should be expected for package systems with thicker leadframes, since the cyclic die deflection and level of stresses will be lower during thermal stress transition. Therefore, less thermal fatigue effects will be induced on the surface of a die that is mounted on this thicker leadframe.

NEW PACKAGE EVOLUTION AND PERFORMANCE EVALUATION

Based upon the modeling predictions and the experimental evidence of thermal and reliability enhancement, the new package system was designed and placed into production. The features of the optimized package are described in Figure 14. Production lot samples of the newly developed package system were thermally characterized and exposed to an extensive reliability qualification study.

THERMAL CHARACTERIZATION

Production samples were thermally characterized under different ambient and cooling conditions. Results are summarized in Table IV. As shown in the table, two modes of cooling at room temperature were used during thermal characterization of the new package: natural convection, and moving air, both with and without a miniature heat sink. In still air at room temperature, the basic power dissipation capability of the new package without a heat sink is 3 W at $T_J = 150°C$. This represents a 25 and 35 percent improvement over the average and worst performances, respectively (see Table I). The comparison can be seen in Figure 15, which demonstrates the relationship between the thermal resistance and package power dissipation for the new package compared to packages discussed earlier. The boundary line in Figure 15 relates maximum power dissipation of the packages at $T_J = 150°C$, which is normally specified as the junction temperature safe limit for BiMOS silicon technology. The best absolute thermal improvement with the new package can be achieved in moving air with a heat sink mounted on its web. The maximum steady-state power capability then is 9.1 W.

TABLE IV

NEW PACKAGE SYSTEM THERMAL PERFORMANCE AT $T_J = 150°C$

No.	Test Conditions	$R_{\theta JA}$(°C/W)	Power Dissipated (W)
1	• Still air (room temp.) • No heat sink	41.6	3.05
2	• Still air (room temp.) • Heat sink (staver type)	24.8	5.1
3	• Moving air (200 LFM) • Room temperature • No heat sink	25.8	4.9
4	• Moving air (200 LFM) • Room temperature • Heat sink	13.9	9.10

QUALIFICATION TEST PROGRAM

The following were the qualification tests conducted:

1 - High-temperature reverse bias life test—150°C ambient at 50 V applied.

2 - Biased 85°C/85 percent RH test at 50 V applied.

3 - Pressure cooker—121°C, 100 percent RH.

4 - Extended temperature cycle, (-65°C + 150°C).

5 - Thermal resistance, $R_{\theta JA}$ after each interval of 500 temperature cycles.

No failures have been reported to date in any of the tests. Results are summarized in Table V.

SUMMARY AND CONCLUSIONS

A high-performance, unconventional 16-lead Plastic Dual-In-Line Package has been developed. The new package power dissipation capability is 25 percent higher than the average measured for available packages and 35 percent higher than the worst package. The long-term reliability performance of the new package exceeds present industry standard reliability requirements. Reliability data also show

TABLE V

RELIABILITY QUALIFICATION RESULTS FOR NEW 16-LEAD DIP

No.	Test	No. of Hours or Cycles Completed	Sample Size	Number of Failures
1	150°C HTRB	6000 h	100	0
2	85°C/85 percent RH/Bias	6000 h	50	0
3	Temp. cycle - 65°C + 150°C "Electrical"	10 000 C	50	0
4	Temperature cycling, "Thermal resistance"	9000 C	12	0
5	Temperature cycling (ground wire fatigue life)	9000 C	50	0

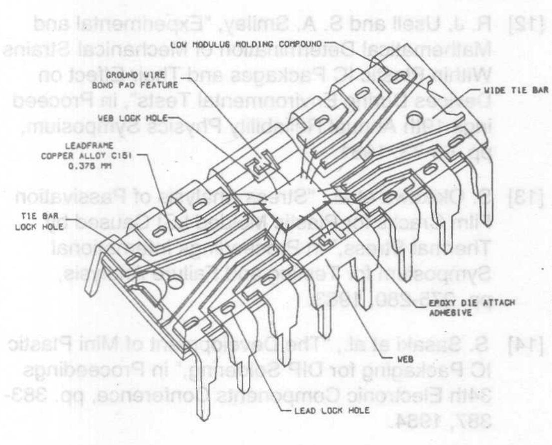


FIGURE 14

New web 16-lead PDIP.

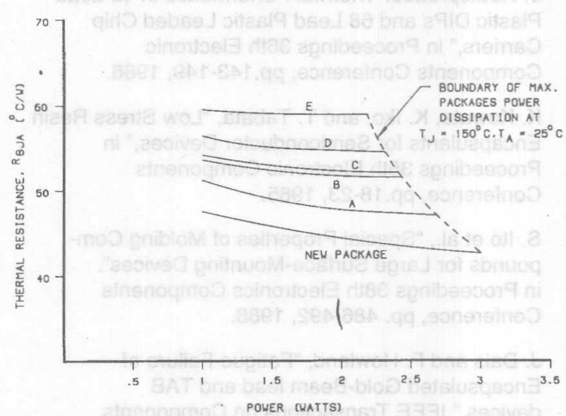


FIGURE 15

Thermal resistance versus power dissipation capability for various packages.

that the chip surface metal deformation resistance to temperature cycling is improved by a factor of 4, and the ground wire propensity for thermal cyclic fatigue damage has been reduced by a factor of 7.

The superiority of the package is due to a combination of an optimum leadframe design and proper choice of materials, such as a low-modulus molding compound. The development strategy was based on a package optimization approach, in which a comparative analysis indicated that existing packages are not fully optimized. Extensive thermal and thermostructural studies have been performed. The finite element results have provided an insight into both the thermal and structural performance of the package.

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APPLICATIONS INFORMATION

ELECTROSTATIC PROTECTION FOR SEMICONDUCTOR PRODUCTS

Users should be aware of certain problems not often associated with the use and handling of semiconductor devices. Common problems relative to ESD (electrostatic discharge) and the role it can play in the manufacturing of systems using microelectronic devices are described here.

A common misconception is that only metal-oxide semiconductors, such as used in CMOS technology, are susceptible to ESD damage. This has been shown, in numerous studies and testing, not to be the case. Bipolar products also can be susceptible and, in some cases, even have lower thresholds of failure or parametric degradation than MOS product. All semiconductor devices should be treated as though they are sensitive to static discharge. This approach will save the handler considerable costs both in manufacturing and field reliability.

Electrostatic potentials are pervasive in that they exist virtually everywhere that electrical insulators are present. The insulator does not necessarily have to be a solid since even liquids and gasses may possess insulating properties. High electric fields may be built up in these insulating materials and discharge themselves easily into a semiconductor device without the slightest indication that a field even existed. Everyone should be familiar with the effect of hair standing on end during the cold and dry winter months. This phenomenon is a result of static charge. It is important to note that the threshold at which a human can detect, by sense of feel, a static charge is roughly 4 kilovolts. This means an operator, assembler, technician, or engineer may be inducing static and never be aware that the event occurred.

There exists a group of materials known as the “Triboelectric Series”. Simply put, this is a group of materials that have a high propensity to generate static charge and thus create problems for semiconductor manufacturers as well as equipment manufacturers. Some of these materials are common in many workplaces and in manufacturing environments. The list includes such materials as acetate, glass, nylon, polyester, cotton, acrylics, polyurethane foam, Teflon (PTFE), PVC (vinyl), and numerous others. These materials should be kept from coming in direct contact with any semiconductor device no matter what its ESD sensitivity because they can generate static fields in the tens of kilovolts.

Static charge carries very limited energy, but damage to a semiconductor junction or gate dielectric in MOS devices does not require high energy to fail or be degraded. The simple discharge of static into a device is enough to rupture catastrophically an MOS gate oxide or create a damaged junction on a bipolar device. These effects can be subtle in that they are difficult to recognize visually on a device even

under extreme magnification (>500X). Often a SEM (scanning electron microscope) is required to identify the damage location and confirm that an ESD event in fact had occurred.

INPUT PROTECTION NETWORKS

Many semiconductor devices incorporate input protection networks directly onto the die to improve static sensitivity. Their purpose is to protect the device while in its application with ground and power applied and not meant to provide protection in any environment that does not have power and ground connections applied. Even in the case of a free-standing board populated with semiconductors, the input protection networks will be of little value since a PC board edge connector will simply act as an extension of the device's leads and any discharge into the card may ultimately wind up at a device terminal. For this reason, an assembly or PC board should be handled with the same care relative to ESD as a free-standing device. If a board is transported, it should be placed in a conductive container designed to protect static sensitive components. In addition, it always is prudent to use a shorting bar on any PC board edge connector to assure that static discharge does not reach any device through the edge connections.

STATIC PROTECTIVE MATERIALS

There are many brands of static protection materials that may be procured. The user should be aware that the efficacy of all these materials is not the same when it comes to static charge dissipation. Some materials, such as "static bags" and "static protective tubes", are coated simply with a conductive spray that will degrade over time and repetitive use. These systems are more appropriate for a one-time use and should not be considered for repeated use. The best ESD protection comes from materials that are "volumetrically" conductive. That is, their entire bulk is conductive and not just their surface. These materials can be used repetitively without the concern for degradation with time and use. Conductive sprays also are materials that one should be wary of since many degrade in their efficiency rapidly and their ability to reduce static levels varies greatly from vendor to vendor.

The best course of action for any user of semiconductor devices and systems that employ semiconductors is to assume that all product is susceptible and thus protect their devices as well as their systems throughout the entire manufacturing process.

APPLICATIONS INFORMATION

OPERATING AND HANDLING PRACTICES FOR MOS INTEGRATED CIRCUITS

MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute Force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

HANDLING PRACTICES—DIE

A conductive carrier should be used in order to avoid differences in voltage potential.

HANDLING PRACTICES— PACKAGED DEVICES

Input protection diodes are incorporated in all MOS/CMOS devices. However, because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS}, V_{DD}, or ground

AUTOMATIC HANDLING EQUIPMENT

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aid here and are available commercially. This method is very effective in eliminating static electricity problems.

AMBIENT CONDITIONS

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

ALERT FAILURE MODES

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

SURFACE-MOUNT IC PACKAGES

Significant benefits can be achieved through the use of surface-mounted devices (SMDs) and general surface-mount technology as it applies to all components, both active and passive. The major benefits are reduced size and weight, and improved system reliability through the reduction of printed wiring board holes. Improved quality and lower assembly cost are obtained through the adaptability of SMD to high-speed, pick-and-place assembly automation.

Prior dense circuit packing methods for active components used chip-and-wire hybrids or flatpacks. Hybrids have the disadvantages of yield limitations, specialized assembly requirements, and the difficulty of rework, burn-in, and testing at temperature or under operating conditions. The demand for flatpacks is decreasing with attendant increases in price. They are also prone to user damage in assembly.

Surface-mountable small-outline ICs and leaded or leadless chip carriers (SOIC, PLCC, and LCC, respectively) answer many of the limitations of flatpacks and chip-and-wire hybrids. In addition to the obvious benefits already described, due to the low mass of SMD, their ability to withstand shock and vibration is superior to conventional dual in-line packages (DIPs) and flatpack assemblies. SMD can also provide an improvement in electrical parameters (reduced wiring resistance, capacitance, and inductance) due to shorter signal paths and very dramatic improvements in the application of industry-standard DIPs.

Three types of surface-mount technology have been defined by the industry.

Type I: single- or double-sided board using only surface-mounted components. Space savings of 40% to 75% are achievable; lowest possible cost.

Type II or Mixed Technology: single- or double-sided board using a mixture of surface-mount and through-hole on the top side and possibly surface-mount on the bottom side. Space savings of 20% to 60% are typical; difficult to build with a single soldering process and typically requires two technologies; testing can be difficult and fixturing costly.

Type III: through-hole components on top side, surface-mount on bottom side. Space savings of 10% to 40% are typical; allows the use of existing equipment and technology for phasing in SMDs.

Another approach that facilitates phasing SMD into existing products is to design small Type I assemblies similar to ceramic

hybrids. With small boards and few components, testing is easily accomplished using the interconnect pins. This construction is especially effective in utilizing the usually wasted vertical space of most printed wiring board assemblies.

Most SOICs feature gull-wing leads on two sides of the package, similar to the DIP configuration. Lead row spacing is 0.150" (part number suffix "L") for 8, 14, and 16-lead packages; 0.300" row spacing (suffix "LW") for 16, 18, and 20-lead packages. Wide body SOICs with heat sink contact tabs (suffix "LB") are used for increased package power dissipation requirements.

PLCCs (part number suffix "EP") are currently supplied in 20, 24, 28, and 44-lead square packages with J-formed leads.

THERMAL CHARACTERISTICS

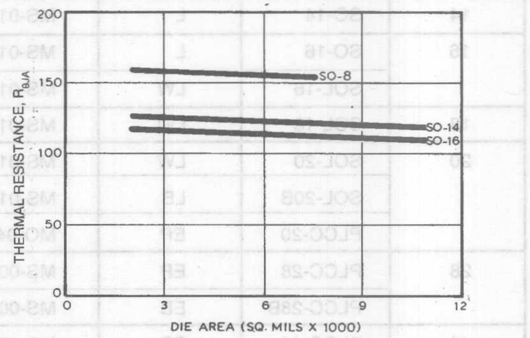
The thermal characteristics of power integrated circuit packages are often the limiting factor in circuit performance. IC packages for surface-mount application may be smaller, lighter, and more economical because of improved reliability and lower assembly cost, but they must still address the thermal problems in order to meet the circuit design requirements.

Regardless of package style (through-hole or surface-mount), the device junction temperature should be limited to +150°C.

The thermal resistance of surface-mounted ICs is increased due to the concentration of heat that results from the reduced package size. For packages with higher lead counts, this increase is minimized.

The printed wiring board on which SMDs are mounted is also very important in thermal management. Thermal resistance is affected less by convection or radiation and more by conduction into the mounting surface. Especially for LCCs, the application of a thermally conductive compound between the package bottom and the mounting surface will further reduce the thermal resistance.

For each surface-mount package type, worst-case thermal resistance is shown in the table on the next page. However, as shown in the curves here, thermal resistance is determined by both package style and chip dimensions. Differences in the data shown here and other industry data are due to the fact that the thermal resistance of these power packages is measured at worst-case junction temperatures at maximum power, making maximum use of convection, radiation, and conduction thermal paths.



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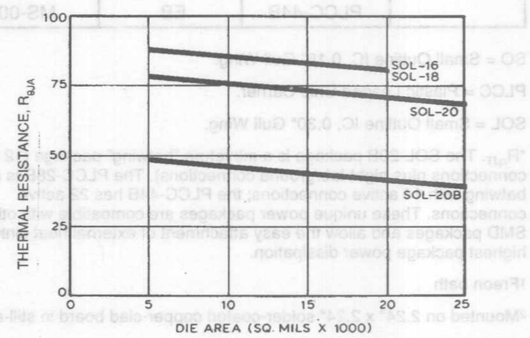

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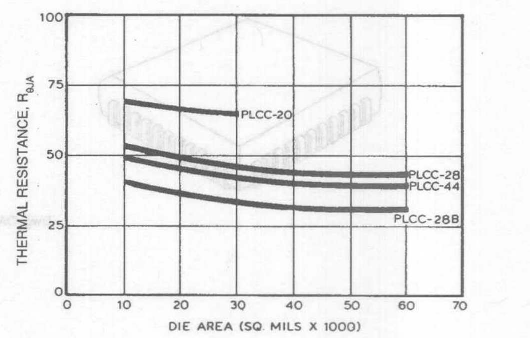

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Note: $R_{\theta JA}$ Measurements made with 2.24" x 2.24" solder-coated copper-clad board in still air.

SURFACE-MOUNT IC PACKAGES

Leads	Package Style	Package Suffix	Industry Package Outline	Thermal Resistance $R_{\theta JC}$[1]	$R_{\theta JA}$[2]	Tape and Reel Width x Pitch (mm)
8	SO-8	L	MS-012AA	45°C/W	108°C/W	12 x 8
14	SO-14	L	MS-012AB	33°C/W	95°C/W	16 x 8
16	SO-16	L	MS-012AC	32°C/W	90°C/W	16 x 8
	SOL-16	LW	MS-013AA	—	80°C/W	16 x 12
18	SOL-18	LW	MS-013AB	—	80°C/W	24 x 16
20	SOL-20	LW	MS-013AC	17°C/W	70°C/W	24 x 12
	SOL-20B	LB	MS-013AC	6°C/W*	60°C/W	24 x 12
	PLCC-20	EP	MO-047AA	35°C/W	59°C/W	16 x 12
28	PLCC-28	EP	MS-007AA	30°C/W	55°C/W	24 x 16
	PLCC-28B	EB	MS-007AA	6°C/W*	36°C/W	24 x 16
44	PLCC-44	EP	MS-007AB	25°C/W	46°C/W	32 x 44
	PLCC-44B	EB	MS-007AB	6°C/W*	30°C/W	32 x 44

SO = Small Outline IC, 0.15" Gull Wing.

PLCC = Plastic Leaded Chip Carrier.

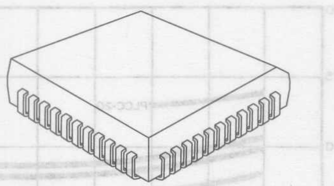
SOL = Small Outline IC, 0.30" Gull Wing.

*$R_{\theta JT}$. The SOL-20B package is a miniature "batwing" package (12 active connections plus eight tab/ground connections). The PLCC-28B is a batwing with 14 active connections; the PLCC-44B has 22 active connections. These unique power packages are compatible with other SMD packages and allow the easy attachment of external heat sinks for highest package power dissipation.

[1]Freon bath

[2]Mounted on 2.24" x 2.24" solder-coated copper-clad board in still-air.

PLCC-44



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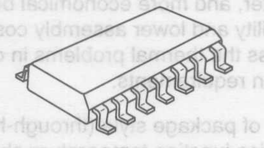
SO-14



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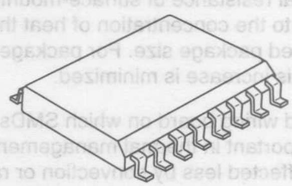
SOL-16



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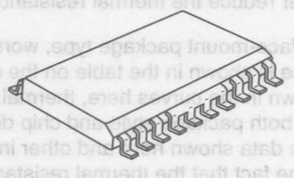
SOL-20B



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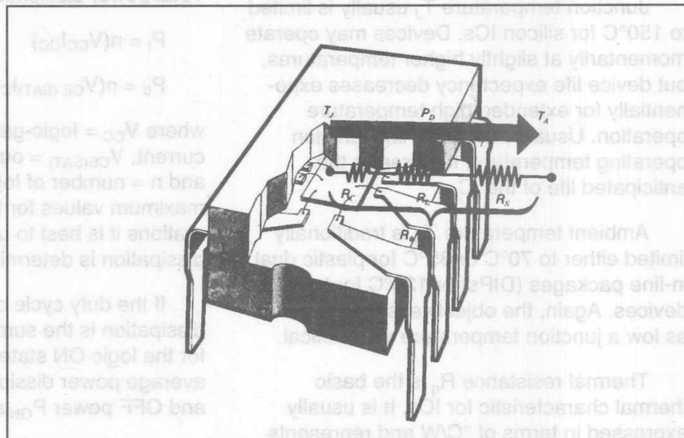
APPLICATIONS INFORMATION

COMPUTING IC TEMPERATURE RISE



IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.

WHY IC TEMPERATURES RISE

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

Excessive heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several amperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

THERMAL CHARACTERISTICS

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_q are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the

user. Equation 1 expresses the relation of these parameters.

$$T_J = T_A + P_D R_\theta \quad (1)$$

Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_q is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor, G_q expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flatpacks and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Total IC power to be dissipated depends on input current, output current, voltage drop, and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_I (typically less than 0.1 W) and output power P_0 must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_I and P_0.

$$P_I = n(V_{CC} I_{CC}) \quad (2)$$

$$P_0 = n(V_{CE\,(SAT)} I_C) \quad (3)$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate supply ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

If the duty cycle of the device is longer than 0.5 s, the peak power dissipation is the sum of the logic-gate power P_I and output power P_0 for the logic ON state alone. If the ON time is less than 0.5 s, however, average power dissipation must be calculated from instantaneous ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1-D)\, P_{OFF} \quad (4)$$

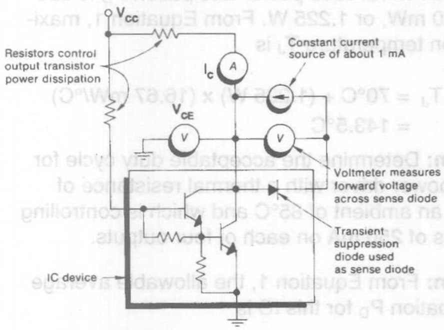
CORRECTIVE ACTIONS

If the junction temperature or the required power dissipation of the IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possibly will be reduced. Possible solutions are:

1. Modify or partition the circuit design so the IC is not required to dissipate as much power.
2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling.
3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC.
4. Specify a different IC with improved thermal or electrical characteristics (if available).

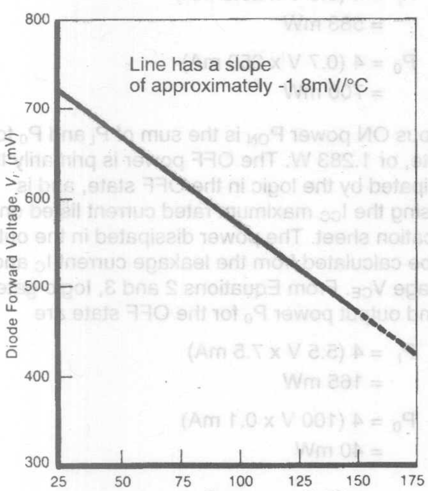
COMPUTING IC TEMPERATURE RISE

SETTING UP THE CIRCUIT



Input power is negligible compared to output power and is therefore not measured.

CALIBRATING THE SENSE DIODE



MEASURING IC TEMPERATURE

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique of measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature. Apply an accurately measured, low current of about 1 mA through the sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement with the internal power source against the voltage measurement with the temperature chamber.

FINDING SAFE OPERATING LIMITS

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$
$$= 0.64 \text{ W}$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ the maximum allowable power dissipation P_D, from Equation 1 is

$$P_D = (150°C - 70°C) \times (16.67 \text{ mW/°C})$$
$$= 1.33 \text{ W}$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an industrial power driver are V_{CC} = 5.25 V, I_{CC} = 25 mA, and $V_{CE(SAT)}$ = 0.7 V, and I_C = 250 mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_I = 4 \text{ (5.25 V x 25 mA)}$$
$$= 525 \text{ mW}$$

$$P_0 = 4 \text{ (0.7 V x 250 mA)}$$
$$= 700 \text{ mW}$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°C + (1.225 \text{ W}) \times (16.67 \text{ mW/°C})$$
$$= 143.5°C$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation P_D for this IC is

$$P_D = \frac{150°C - 85°C}{100°C/W}$$
$$= 0.65 \text{ W}$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 s, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_I and output power P_0 for the ON state are

$$P_I = 4 \text{ (5.5 V x 26.5 mA)}$$
$$= 583 \text{ mW}$$

$$P_0 = 4 \text{ (0.7 V x 250 mA)}$$
$$= 700 \text{ mW}$$

Instantaneous ON power P_{ON} is the sum of P_I and P_0 for the ON state, or 1.283 W. The OFF power is primarily the power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_C and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_I and output power P_0 for the OFF state are

$$P_I = 4 \text{ (5.5 V x 7.5 mA)}$$
$$= 165 \text{ mW}$$

$$P_0 = 4 \text{ (100 V x 0.1 mA)}$$
$$= 40 \text{ mW}$$

COMPUTING IC TEMPERATURE RISE

Instantaneous OFF power P_{OFF} is the sum of P_I and P_0 for the off state, or 205 mW. From equation 4, acceptable duty cycle D is

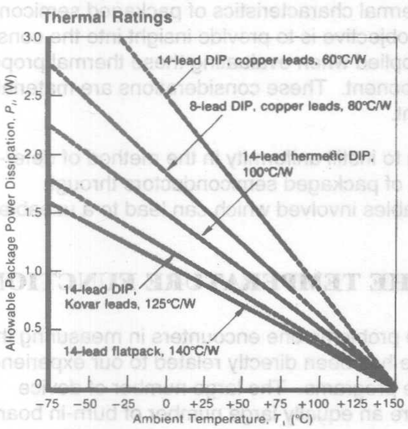
$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}}$$

$$= \frac{0.65\ \text{W} - 0.205\ \text{W}}{1.283\ \text{W} - 0.205\ \text{W}}$$

$$= 41\%$$

WHAT THE CURVES SHOW

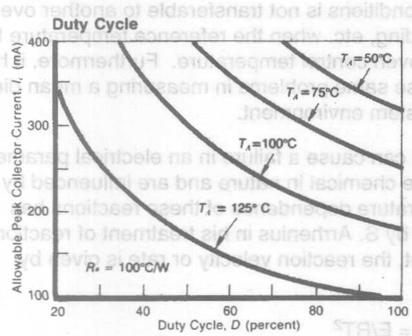
The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.



Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor G_q, which is the reciprocal of thermal resistance R_q. For an ambient temperature of 50°C, a typical 14-lead flatpack with an R_q of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C (R_q = 45°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.



Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 s.

APPLICATIONS INFORMATION

THERMAL RESISTANCE— A RELIABILITY CONSIDERATION

More and more the semiconductor component supplier and the ultimate system user are becoming aware of the need for reliable components. Most failure mechanisms responsible for reliability failures are temperature dependent and the kinetics of the failure reaction are normally described by an Arrhenius function. This dependence, therefore, demands the capability of measuring the mean temperature which an integrated circuit die will attain during operation to realistically assess the reliability of the part.

The problem addressed by this paper is the inconsistency of the measurement techniques and the results used by manufacturers and users to determine the thermal characteristics of packaged semiconductor components. Our objective is to provide insight into the considerations which must be applied when evaluating these thermal properties of the packaged component. These considerations are materials, geometry and environment.

Furthermore, we wish to instill uniformity in the method of determining thermal properties of packaged semiconductors through understanding of the variables involved which can lead to a useable industry standard.

RELIABILITY—THE TEMPERATURE FUNCTION

The recognition of the problems one encounters in measuring the mean temperature of a die has been directly related to our experiences in our reliability assurance programs. The large number of device types manufactured require an equally large number of burn-in boards having different functions and geometry for the individual reliability studies. The variations in board density and thermal environment for a device under test have provided considerable junction temperature data from which we conclude that a “thermal resistance” measured in one oven with its set of conditions is not transferable to another oven with different boards, loading, etc. when the reference temperature for the measurement is the oven control temperature. Furthermore, it has become obvious that these same problems in measuring a mean die temperature exist in a system environment.

Most reactions which can cause a failure in an electrical parameter of an integrated circuit are chemical in nature and are influenced by temperature. The temperature dependence of these reactions has been described very well by S. Arrhenius in his treatment of reaction kinetics.[1] In his treatment, the reaction velocity or rate is given by the equation

$$d\ln V_r/dT = E/RT^2$$

where V_r is the specific reaction rate, T is the absolute temperature, R is the Molar Gas Constant, and E is the energy difference between a mole of active molecules and a mole of normal molecules.

This equation integrates to

$$\ln V_r = E/RT + A$$

where A is a constant which is the value of $\ln V_r$ at $1/T = 0$, $(\ln V_r)$. A more familiar expression is

$$\ln V_r = \ln V_r^o - \epsilon/kT$$

or

$$V_r = V_r^o e - \epsilon/kT$$

where is the activation energy per molecule (= E/N), N = Avagado's number and k is the gas constant per molecule (= R/N), which is generally known as the Boltzmann constant. It has the value

$$8.6 \times 10^{-5}\ \mathrm{eV/^\circ K}.$$

V_E, the time rate of change of electrical parameters is proportional to V_r, i.e., $V_E = BV_r$. The amount of change in the electrical parameter necessary to cause a normal device to fail, ΔP_f, is $V_E t_f$ where t_f is the time of failure.

Recalling that $V_E = BV_r$, then

$$\Delta P_f = BV_r t_f$$

For a given device ΔP_f is a constant, therefore,

$$t_f = \Delta P_f B^{-1}/V_r$$

but

$$V_r = V_r^o e\ \epsilon/kT$$

therefore

$$t_f = (B^{-1}\,\Delta P_f / V_r^o\, e^{\epsilon/kT}) = 8e^{\epsilon/kT})$$

where

$$8 = B^{-1}\Delta P_f / V_r^o$$

The acceleration factor $(\overline{AF})$ between any two temperatures is derived from this equation, when the activation energy for the failure reaction is known:

$$\overline{AF} = t_{f_1}/t_{f_2} = e^{\epsilon/k(1T_1 - 1/T_2)}$$

Activation energies of most reactions responsible for random failures in a normal operating period (beyond infant mortality) are nominally

(0.4 - 1.0) eV.

The importance of accurately determining the die temperature is now clear if one considers a not unrealistic situation where a device is thought to be operating with a die temperature of 120° and the actual temperature is 150°C. If the failure reaction has an activation energy of 0.7 eV, then the acceleration factor is 4.3 which means the device would fail in less than one quarter of the time it would have taken if the device actually operated at 120°C.

THERMAL RESISTANCE — $R_{\theta JA}$

Quite frequently, applications engineers have made attempts to identify the temperature attained by a die when a steady state rate of heat is being generated by the die by applying the term called "Thermal Resistance." This "constant," designated $R_{\theta JA}$, or simply θ_{JA}, relates the temperature rise of a packaged integrated circuit die above an ambient temperature when a known constant power is generated in the die. This term is normally defined as

$$\theta_{JA} = (T_J - T_A)/P_D$$

where T_J is the mean junction or die temperature, T_A is an ambient temperature, and P_D is the power generated within the die which must be conducted from the die to the ambient. This is occasionally designated Q_T, the time rate of heat generation in the die. Thermal resistance data supplied by manufacturers may be referenced to a cubic foot of free or still air, flowing air at some velocity, or simply no reference. These are some of the definitions of "ambient" from which one must determine where to measure T_A.

Thermal resistance as defined by θ_{JA} is not constant. It is made up of a constant term (or terms) in series with a number of variable terms. The constant terms relate to the package materials and geometry, which we will designate θ_{JCi} and the variable terms relate to the heat paths from the package boundary to some isothermal envelope in the system which has the temperature T_A. Even if the system for measuring θ_{JA} is defined, it is virtually impossible to reproduce that system in an application since the external thermal paths are determined by the method of mounting, the printed wiring board if used, other heat generating components on the board or in the vicinity, air flow patterns, etc. These are all variables for each application. We have measured values of θ_{JA} for the same device which vary by a factor of two when the mounting and environmental conditions are changed. The values

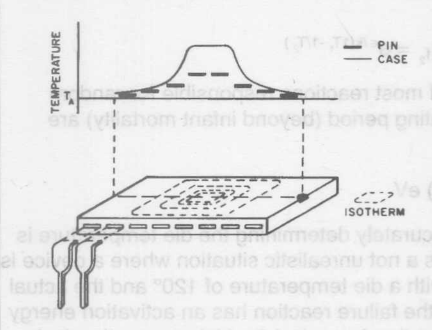


FIGURE 1

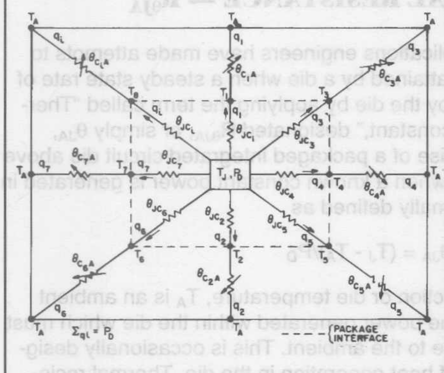


FIGURE 2

in the θ_{JA} column in Tables 2 and 3 are indicative of the variation.

One is tempted to partition θ_{JA} into two thermal terms.

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{JC} is defined as the thermal resistance from the source of power at T_J to the boundary of the package not including the external legs, and θ_{CA} is the thermal resistance from the package boundary to that isothermal envelope at T_A. However, when one examines the thermal profile along the surface of a plastic dual-in-line package such as shown in Figure 1, it is immediately obvious that a definition of θ_{JC}

$$\theta_{JC} = (T_J - T_C)/P_D$$

cannot be applied because T_C varies with position. Similarly, the term θ_{CA} defined by

$$\theta_{CA} = (T_C - T_A)/P_D$$

suffers from the same variablility in T_C. This being the case, it is invalid to partition θ_{JA} when operating on the *total* power to be dissipated, P_D.

THE THERMAL MODEL

When one examines a plastic package supplied by an individual manufacturer it is found that the geometry of the lead frame, its position within the package boundary, its composition, the composition of the plastic and its filler, the internal wire bonding are very carefully controlled and constant in time. This being the case one can readily build a model of the package which can be as invariant as the package material properties. If one considers all possible heat flows, a very complex model emerges. However, if the thermal conductivities of the package materials and the orders of magnitude difference in the values of these conductivities are considered, a simplified workable model can be generated by neglecting heat paths where heat flows are minimal. The simplified model shown in Figure 2 has ignored the heat flow between leads and assumes that the large difference between the thermal conductivity of the loaded plastic and the metals in the package define the specified heat paths. For example, the heat flow between leads would be a shunting resistor between heat paths in the model. The thermal conductivity of most plastics range between 1.5 and 3 x 10^{-3} calories/cm - °C while copper based materials range between 0.5 and 0.82 calories/cm - °C and nickel based alloys are about 0.03 calories/cm - °C.

The heat paths defined by θ_{JCi}, where i refers to a particular path, radiate from the chip to an area on the package periphery defined by the projected chip or pad area as well as the mean cross-sectional area of each of the leads within the plastic package boundary (see Figure 1). Because of package symmetry, a 16-lead isolated-pad

package may have seven different heat paths which can be characterized. The thermal resistance, θ_{JCi}, can be calculated for each path from the geometry and material properties. For example θ_{JC1} is the resistance from the top of the chip to the projected area on the package surface. The value of θ_{JC1}, is given by

$$\theta_{JC_1} = (T_J - T_{C_i})/q_1 = L/K_pA$$

where L is the length of the heat path (thickness of the plastic above the die), A is the cross-sectional area of the heat path (area of the die or the pad), K_P is the thermal conductivity of the loaded plastic and q_1 is the heat/second flowing in the path defined by A and L.

θ_{JC2} is the thermal resistance from the top of the die through the silicon, through the pad and through the plastic to the bottom surface. The value of θ_{JC2} is given by

$$\theta_{JC_2} = (T_J - T_C)/q_2 = [1/A] \sum L_n/K_n \quad n = \text{Si, Metal, Plastic}$$

Similar expressions can be derived for each of the leads and they have the form

$$\theta_{JC_i} = (T_J - T_{C_i})/q_i = [1/t] [(L/K_PW_P) + (1/K_M) \sum L_n/W_n] \quad n = 1, 2.......$$

where t is the thickness of the lead frame, K_p is the thermal conductivity of the loaded plastic, K_M is the thermal conductivity of the frame metal, L_n is the mean length of each connected portion of a leg segment having a mean width, W_n. In accord with the model, each internal path characterized by a thermal resistance, θ_{JCi}, is in series with an external thermal resistance, θ_{CiA}, which completes the path to T_A. The value of θ_{CiA} can be calculated from the amount of heat, q_i, flowing through the internal package path and the temperature difference, $(T_{Ci} - T_A)$, with the equation

$$\theta_{CiA} = (T_{C_i} - T_A)/q_i.$$

TABLE 1

COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES OF $[\theta_{JC}]\ T_{C_i} = T_A$ (All measurements in °C/W)

PackageFrame Type	Material	$[\theta_{JC}]\ T_{C_i} = T_A$ Experimental	Calculated
16-Pin, Isolated Pad, Epoxy I	Copper	41 ± 3	43
16-Pin, Isolated Pad, Epoxy I	Kovar	100 ± 4	93
16-Pin Tab	Copper	8.6 ± .7	8.5

Values of θ_{CiA} are variable and depend upon the specific environment.

We identify the heat paths in our calculations and data as follows: a) when i = 1, the path is from die to case surface directly above, b) when i = 2, the path is from die to the case surface directly below and c) when i = 3, 4, 5 . . . the path is from die through an identified metal lead to the intersection with the plastic surface.

VERIFICATION OF MODEL

From the model one can derive the minimum thermal resistance which is characteristic of the package. This can be calculated for the condition when all case temperatures are equal and at T_A. This is equivalent to shorting all external thermal resistances so that $T_{C_i} = T_A$. When all T_{C_i} are equal, the reciprocal of the sum of the reciprocals of all θ_{JCi} is the minimum thermal resistance for the package. This is realized experimentally by placing the unit in an infinite heat sink such as a rapidly stirred, low-viscosity controlled temperature bath. The case temperature is now forced to be the same over all surfaces and by definition it is T_A. θ_{JC} is the minimum limit of θ_{JA}. Table 1 shows the agreement between the values of θ_{JC} calculated from the model when the case temperatures are shorted together and the values experimentally measured in a controlled temperature liquid bath. The agreement between calculated and experimental values for packages constructed from different materials enhance the validity of the model.

APPLYING THE MODEL TO MEASURE T_J

Having verified the model, any one of the identified heat paths, which has a constant thermal resistance, θ_{JC_i}, can now be used to determine quite accurately the die temperature, T_J. If one chooses to measure the case temperature directly above the die, the difference between die temperature and case temperature is related to the heat

flow, q_i, through that path by the thermal conductivity equation:

$$q_i = K_pA\ (T_J - T_{C1})/L_1.$$

Rearranging this equation to

$$(T_J - T_{C1})/q_1 = L_1/k_pA_1 = \theta_{JC1}$$

Then

$$T_J = T_{C1} + q_1 q_{JC_1}$$

If the fraction of total heat, P_D, generated by the die which passes through path 1 is defined as k, then

$$q_1 = k_1\ P_D$$

Substituting into the previous equation T_J is now referenced to T_{C_1} by

$$T_J = T_{C_1} + k_i\ \theta_{JC_1}\ P_D$$

where T_J, T_{C1}, and P_D are experimentally measurable quantities. Values of $k_i\theta_{JC1}$ can be determined. This term can be used to determine T_J in any environment by measuring T_{C1} and the total heat generated by the die. This equation applies for any path, i, i.e.

$$T_J = T_{C_i} + k\ \theta_{JC_i}\ P_D$$

Experimental results are presented in Table 2 which establish that $k_i\theta_{JC_i}$ is a constant, the magnitude of which is determined by the heat path chosen.

TABLE 2
THERMAL RESISTANCE VALUES—ISOLATED PAD—EPOXY PACKAGE (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_4A}$	$k_4\theta_{C_1A}$	$k_4\theta_{JC_1}$	$k_4\theta_{JC_4}$
ULN2003A 16-Pin Copper Frame	1 ft.³ Still Air, Socket Mount	84.7	39.1	48.1	36.6	45.6
ULN2003A 16-Pin Copper Frame	Oven #1, 60 CFM, Pin Connectors	60.0	17.0	25.2	34.8	42.3
ULN2003A 16-Pin Copper Frame	AAVID E type 5010 Heat Sink Oven #1, 60 CFM	50.4	11.4	15.2	35.2	39
ULN2003A 16-Pin Copper Frame	Fluorocarbon Bath, Pin Connectors	41.3	3.3	2.9	38.4	38

TABLE 3
THERMAL RESISTANCE VALUES—TAB PAD—EPOXY (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_5}A$	$K_5J_{C_5}$
Test Chip "B" Package	Oven #1, T_A = 50°, 60 CFM	32.8	25.0	7.8
ULN2068B	Oven #1, T_A = 50°, 60 CFM	34.9	26.4	8.5
ULN2068B	Socket Mount, FC-40 Bath	23.2	13.5	9.7
ULN2068B	Socket Mounted on Board, FC-40 Bath	26.8	17.4	9.4
Test Die "B" Package	Oven #1, Soldered on Test Board, 60 CFM	31.2	22.8	8.4
Test Die "B" Package	Oven #1, Soldered in Test Board w/Staver Heat Sink	22.3	14.2	8.1

In our notation, $k_4\theta_{JC_4}$ is the thermal resistance of the path determined by measuring the temperature of pin 4 at the point of intersection with the case body. Further data are presented in Table 3 for a copper tab package where the pad on which the die is mounted extends to the outside of the package. The values of $k_5\theta_{JC_5}$ remain constant over a large change in environment. When i = 5, the heat path is from the die through the heat tab to the intersection with the case surface.

Figure 3 shows the outline of the frame in the 16-pin isolated-pad package which is designated the "A" package. The "B" package or tab package frame outline is also shown.

MEASUREMENT OF $k_i\theta_{JC_i}$

Although the derived equations indicate that $k_5\theta_{JC_i}$ are determined by two temperature measurements at one power level, the values are more accurately determined from temperature versus power plots.

If one considers any one path, i, in the model, that path is described by:

$$T_J - T_A = q_i\,(\theta_{JC_i} + 0_{C_iA})$$

Here again, if k_i is the fraction of the total heat (P_D) which traverses path i, then the previous equation can be written

$$T_J - T_A = k_iP_D\,(\theta_{JC_i} + \theta_{C_iA})$$

or rearranging terms

$$(T_J - T_A)/P_D = k_i\theta_{JC_i} + k_i\theta_{C_iA}$$

By definition $(T_J - T_A)/P_D = \theta_{JA}$, therefore by subtitution and rearrangement

$$k_i\theta_{JC_i} = \theta_{JA} - k_i\theta_{C_iA}$$

where experimentally θ_{JA} is the slope of a plot of T_J versus P_D and $K_i\theta_{CA_i}$ is the slope of the plot of T_{C_i} versus P_D. Figures 4, 5, and 6 are representative of the experimental plots for evaluation of $k_i\theta_{JC_i}$.

T_{Ci} MEASUREMENT

The numerical values of $k_i\theta_{JC_i}$, which we have shown experimentally to be constant over a large variation in environmental conditions,

are functions of the measuring system for determining the case or leg temperature, T_C. This can be shown by considering heat path 1 in the Model shown in Figure 2. In this case, $q_1 = (T_J - T_A)/(\theta_{JC_1} + \theta_{C_1A})$. θ_{JC_1} is defined as L_1/k_pA_1, where A_1 is determined by the die area. When a thermocouple is attached to the surface directly over the die, it also functions as a heat sink. This changes the effective area A of the internal heat path and also changes the external thermal resistance, θ_{C_1A}. The changes are functions of the thermocouple composition and size. The value of θ_{JC_1} is now determined by the effective area of contact of the thermocouple and its value remains constant when the attached thermocouple's size is held constant. k_1, ($= q_1/Q_t$), also changes because q_1 is determined by the sum of θ_{JC_1} and θ_{C_1A}. The term $(T_J - T_A)$ is essentially constant within experimental error because q_1 is small compared to Q_t and the variations in q_1 do not measureably change the die temperature.

θ_{C_1A} decreases as the wire size of a copper-constantan thermocouple increases and it increases as the composition is changed from copper-constantan to iron constantan. The thermal conductivities of copper, iron, and constantan are respectively 0.9, 0.16, and 0.054 cal/°C-cm.

Data in Table 4 confirm the direction and change in $k_1\theta_{JC_1}$, with change in measuring system. Data were taken in the same oven ambient.

PLASTIC PACKAGE FRAME GEOMETRY

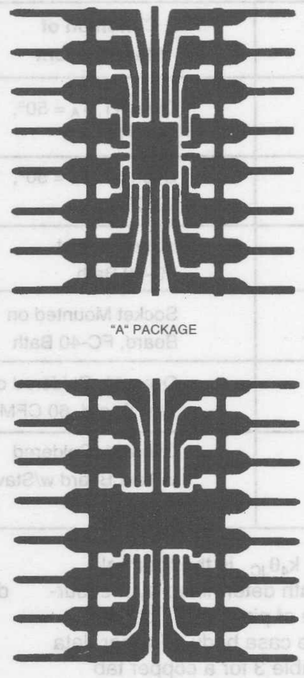


FIGURE 3

When the physical system for T_C measurement and the conditions for measurement are specified and held constant, values for $k_1\theta_{JC_1}$ are constants.

TABLE 4
VARIATIONS IN $k_i\theta_{JCi}$ WITH MEASUREMENT SYSTEM (All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_1\theta_{C_1A}$	$k_1\theta_{JC_1}$
Test Device	0.005" Type "J" Thermocouple	127.6	52.2	75.4
Test Device	0.012" Type "J" Thermocouple	123.5	31.5	92.0
Linear Circuit	0.005" Type "T" Thermocouple	123.3	75.0	48.3

THERMAL RESISTANCE—
A RELIABILITY CONSIDERATION

T_J MEASUREMENT FOR $k_i\theta_{JC_i}$ DETERMINATION

An accurate measurement of the value of $k_i\theta_{JC_i}$ requires a method of measuring the mean temperature of the die, T_J. Techniques to make this measurement have been discussed elsewhere. (See Ref. 2, 3, 4) They involve measurement of a temperature sensitive parameter of an element on the die. The forward voltage drop across a diode measured at constant current is a commonly used parameter. One must observe caution when applying the calibration data for an element in an unpowered die to the measured values of that element when the die is powered. It is rather unique if a parasitic voltage or current from the powered portion of the die does not interact with the temperature measuring element. This interaction leads to an inaccurate indication of the true temperature.

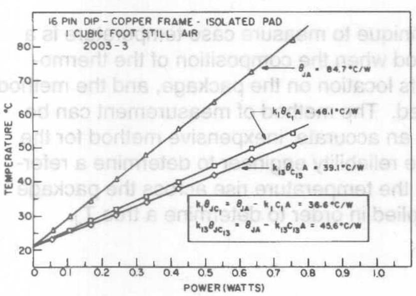


FIGURE 4

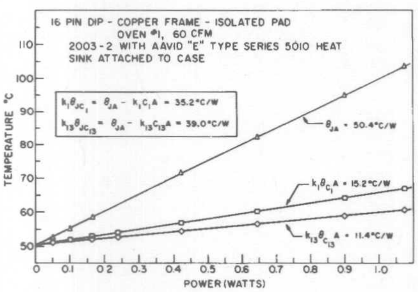


FIGURE 5

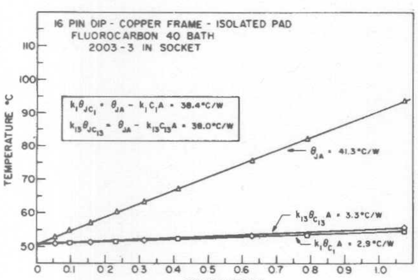


FIGURE 6

A test chip with a number of temperature sensitive elements is valuable. Figure 7 is a photo micrograph of a test chip designed to evaluate thermal resistance values for various packages as well as package surface interactions. The die contains 3 heat generators, and 6 primary temperature sensors, which are either diodes or special resistors. Parasitics normally interact differently with different elements because of location or structure variations. Agreement in the value of temperatures measured simultaneously for different elements on the chip normally indicates a correct measurement.

Figure 8 illustrates errors which can be introduced when making static steady state measurements of temperature during power application. Observe the plots of T_J (from V_{eb} calibration) versus P_D for three different diodes on the chip. Although the slopes of the plots after initial power agree within 10%, the initial portion of the curve indicates a negative thermal resistance and the offsets of the curves indicate a varying interaction at different power levels. Although calculation of thermal resistance by the slope method would introduce a similar error for all three diodes, the single power point method for calculating $k_i\theta_{JC_i}$, where $k_i\theta_{JC_i} = (T_J - T_{C_i})/P_D$, would introduce considerable and different levels of error in the calculated values for each diode measurement.

For example, if temperature measurements were made at a power level of 0.22 W, one would calculate a value of 44.6°C/W for $k_i\theta_{JC_i}$ using T_J from diode 7-15. 57.1°C/W using T_J from diode 7-5, and 63.8°C/W using T_J from diode 7-6. The true value which was verified by pulse measurements was 97°C/W.

To eliminate interactions between the powered portion of a circuit and the temperature sensing element during measurement, the circuit shown in Figure 9 was developed. This circuit was designed for thermal evaluaton of packages in which the function could be a linear circuit, a digital circuit, or the standard test chip which has a number of different power sources and temperature sensing elements.

In operation, the circuit applies power at a measured level to the device under test for approximately one second, interrupts power for 40 microseconds, and continues this cycle throughout the test period. At the beginning of the 40-microsecond power off interval, a 10-microsecond delay allows circuit transients to decay before the

diode current is activated. A 6-microsecond delay allows the current to settle before a sample and hold circuit samples the diode voltage to determine the chip temperature. This sequence allows the package under test to come to thermal equalibrium with the environment which approaches that for continuous power input. The power down sequence and temperature measurement interval are short enough to ensure that the actual temperature drop when power is removed is less than the sensitivity of the temperature sensitive element.

The case temperature measurements, T_{Ci}, can be made by thermocouple or by infra-red measurements.[4] In theory, the infra-red measurements would be preferred since a conductive contact is not made to the surface which is to be measured. In practice, a number of difficulties with I.R. measurements are encountered. The emissivity of the surface to be measured must be controlled to give accurate measurements. This normally requires painting the surface with a "proprietary" film. When the emissivity is mastered, two larger difficulties must be overcome; a) physically placing the infra-red measuring instrument into the system to view a package surface when the unit may be buried in a maze of printed wiring boards and circuitry and b) the cost of available instrumentation.

The thermocouple technique to measure case temperature is a practical and reliable method when the composition of the thermocouples, its physical size, its location on the package, and the method of its attachment are defined. The method of measurement can be standardized and provides an accurate, inexpensive method for the applications engineer or the reliability engineer to determine a reference temperature to which the temperature rise across the package path, $(k_i\theta_{JC_i})P_D$, can be applied in order to determine a true T_J.

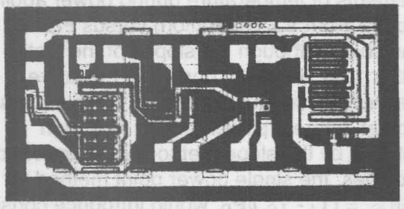


FIGURE 7

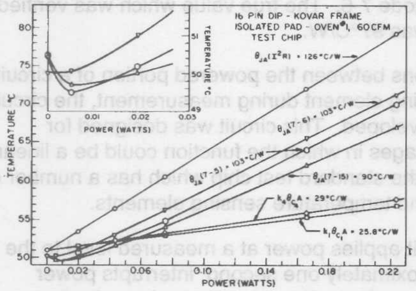


FIGURE 8

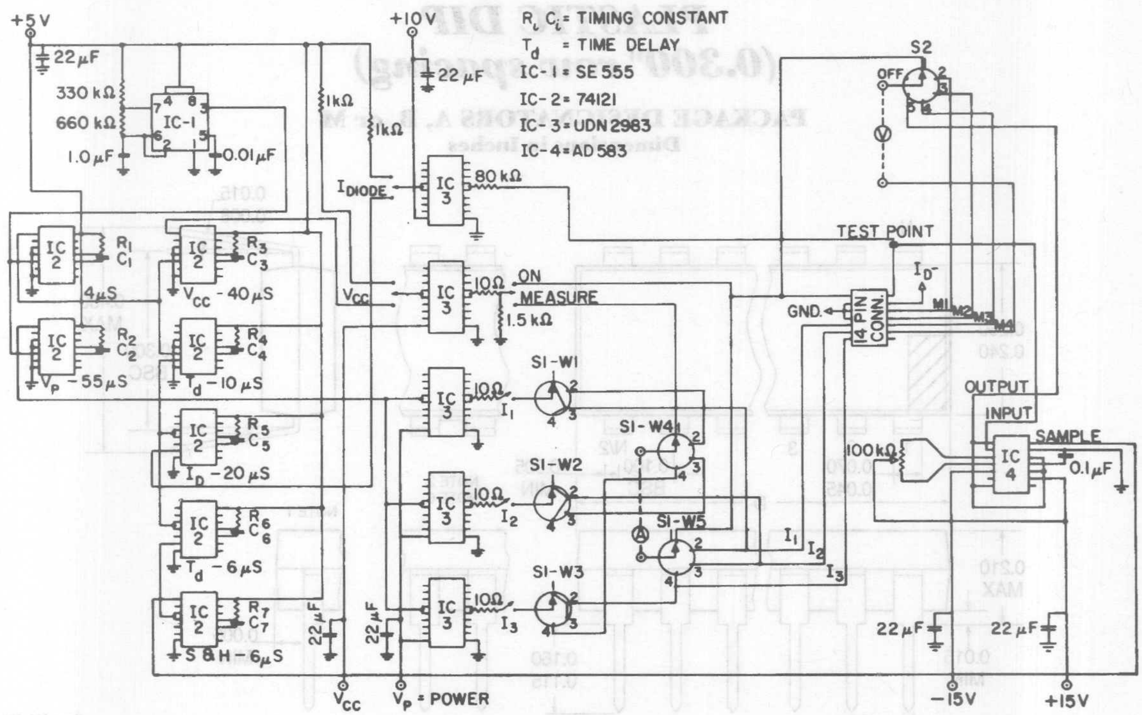


FIGURE 9

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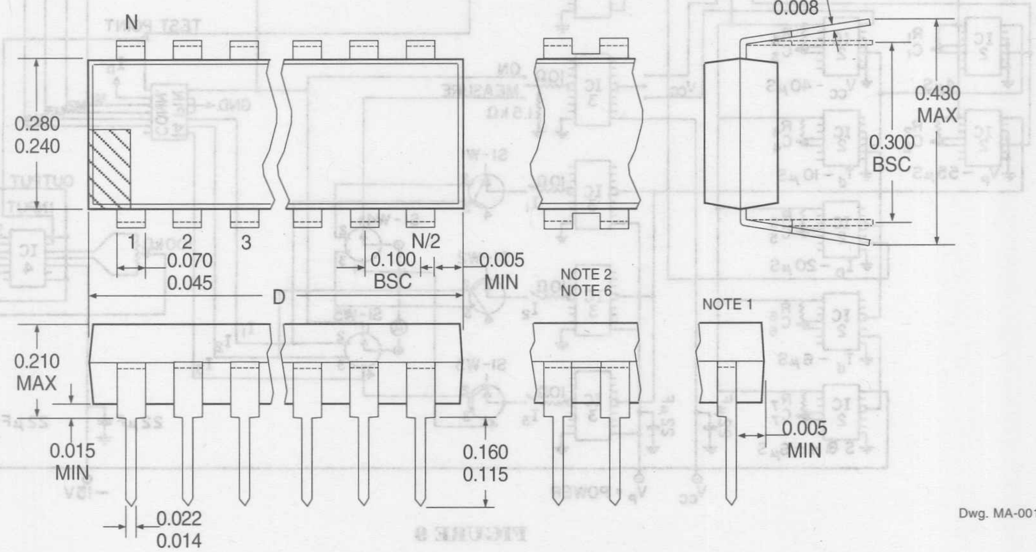
PACKAGE OUTLINES

PLASTIC DIP (0.300" row spacing)

PACKAGE DESIGNATORS A, B, or M
Dimensions in Inches



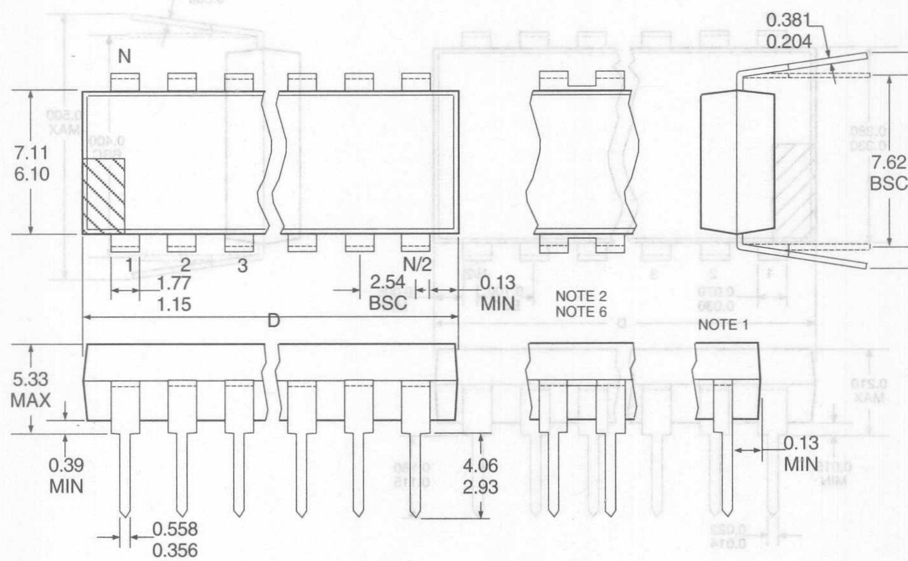
N	Number of Leads Pkg. Designator	8 M	14 A	16 A	16 B	18 A	20 A	24 B
D	Body Length	0.355/0.400	0.735/0.775	0.735/0.775	0.735/0.775	0.880/0.920	0.980/1.060	1.230/1.280
Notes	(Leads Affected)	1 (1, 4, 5, 8)	—	1 (1, 8, 9, 16)	1 (1, 8, 9, 16) 2 (4, 5, 12, 13) 3	—	—	2 (5-7, 18-20) or 2 (6, 7, 18, 19)
JEDEC Outline Designation		MS-001BA	MS-001AA	MS-001BB	—	MS-001AC	MS-001AD	MS-001AF

NOTES:
1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Maximum lead thickness is 0.020".
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP (7.62 mm row spacing)

PACKAGE DESIGNATORS A, B, or M
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-001A mm

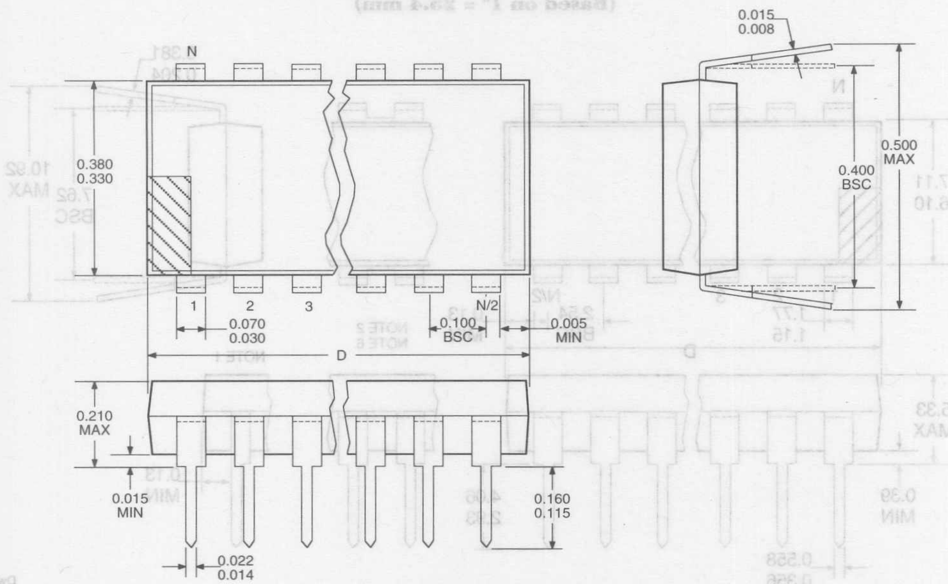
N	Number of Leads Pkg. Designator	8 M	14 A	16 A	16 B	18 A	20 A	24 B
D	Body Length	9.02/10.16	18.67/19.68	18.67/19.68	18.67/19.68	22.35/23.67	24.89/26.92	31.24/32.51
Notes	(Leads Affected)	1 (1, 4, 5, 8)	—	1 (1, 8, 9, 16)	1 (1, 8, 9, 16) 2 (4, 5, 12, 13) 3	—	—	2 (5-7, 18-20) or 2 (6, 7, 18, 19)
JEDEC Outline Designation		MS-001BA	MS-001AA	MS-001BB	—	MS-001AC	MS-001AD	MS-001AF

NOTES: 1. Leads 1, N/2, (N/2) + 1, and N may be half leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Maximum lead thickness is 0.508 mm.
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP
(0.400" row spacing)

PACKAGE DESIGNATOR A
Dimensions in Inches



Dwg. MA-002A in

N	Number of Leads Pkg. Designator	22 A						
D	Body Length	1.050/1.120						
Notes	(Leads Affected)	—						
JEDEC Outline Designation		MS-010AA						

NOTES: 2. Webbed lead frame. Leads indicated are internally one piece.

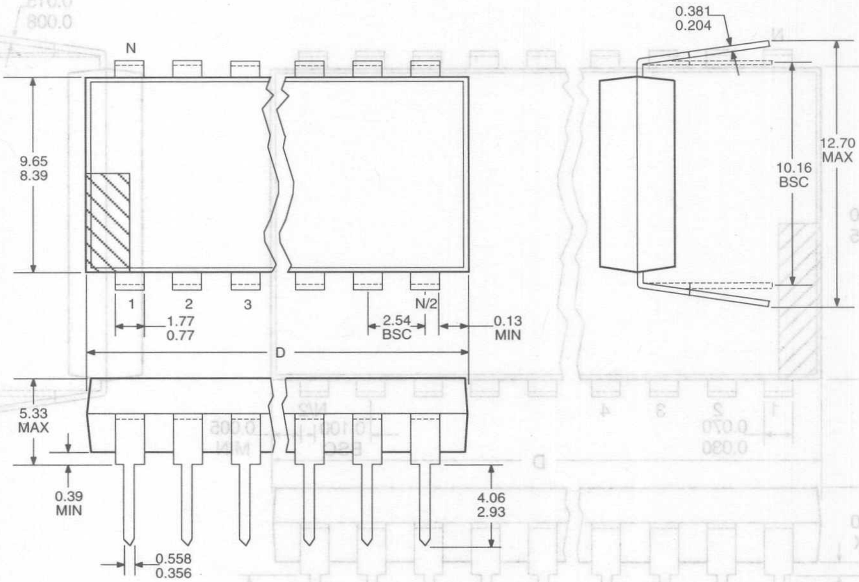
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP (10.16 mm row spacing)

PACKAGE DESIGNATOR A

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-002A mm

N	Number of Leads	22							
	Pkg. Designator	A							
D	Body Length	26.67/28.44							
Notes	(Leads Affected)	—							
JEDEC Outline Designation		MS-010AA							

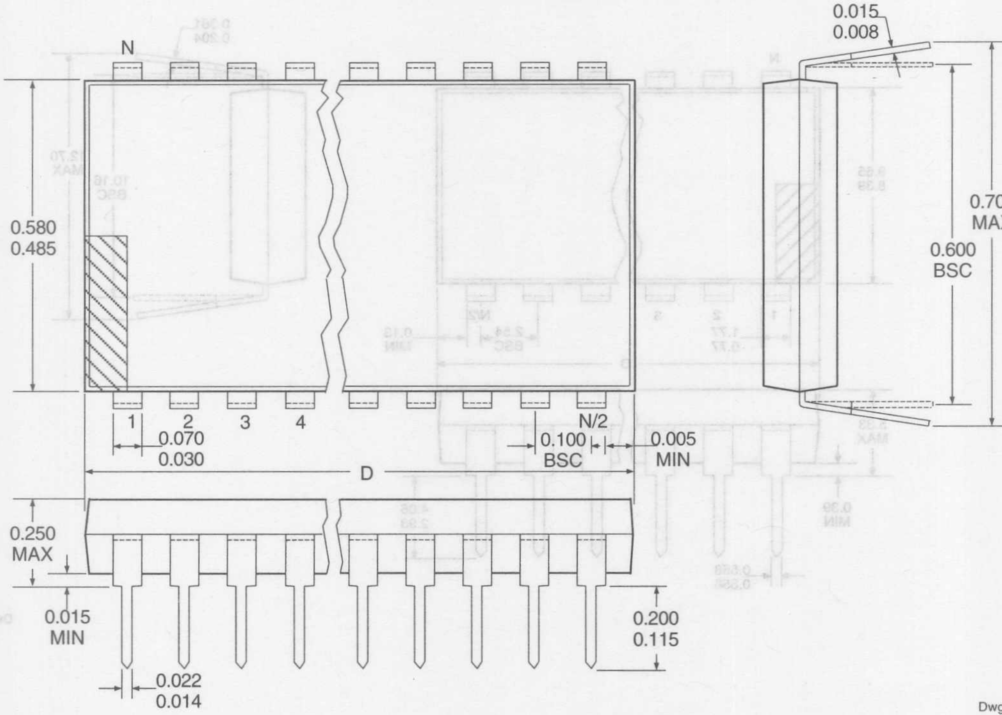
NOTES: 2. Webbed lead frame. Leads indicated are internally one piece.
4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

PLASTIC DIP (0.600" row spacing)

PACKAGE DESIGNATOR A

Dimensions in Inches



Dwg. MA-003A in

N	Number of Leads	28	40					
	Pkg. Designator	A	A					
D	Body Length	1.380/1.565	1.980/2.095					
Notes		—	—					
JEDEC Outline Designation		MS-011AB	MS-011AC					

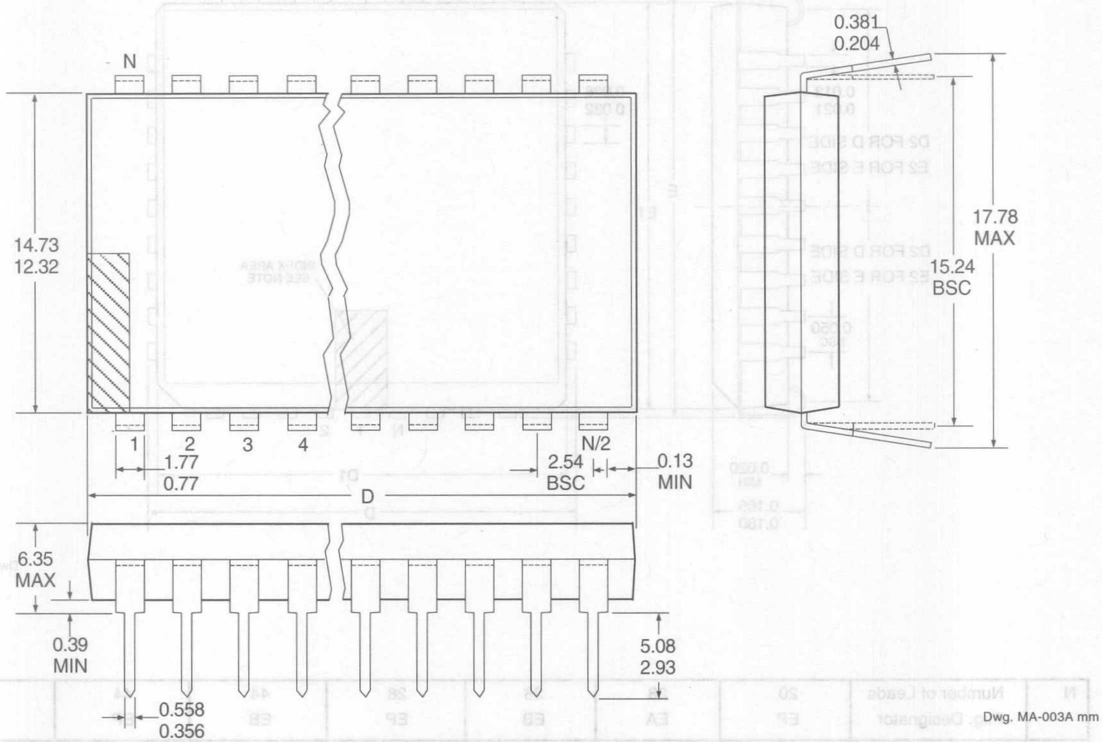
NOTES: 4. Lead thickness is measured at seating plane or below.

5. Lead spacing tolerance is non-cumulative.

6. Exact body and lead configuration at vendor's option within limits shown.

PLASTIC DIP
(15.24 mm row spacing)

PACKAGE DESIGNATOR A
Dimensions in Millimeters
(Based on 1" = 25.4 mm)



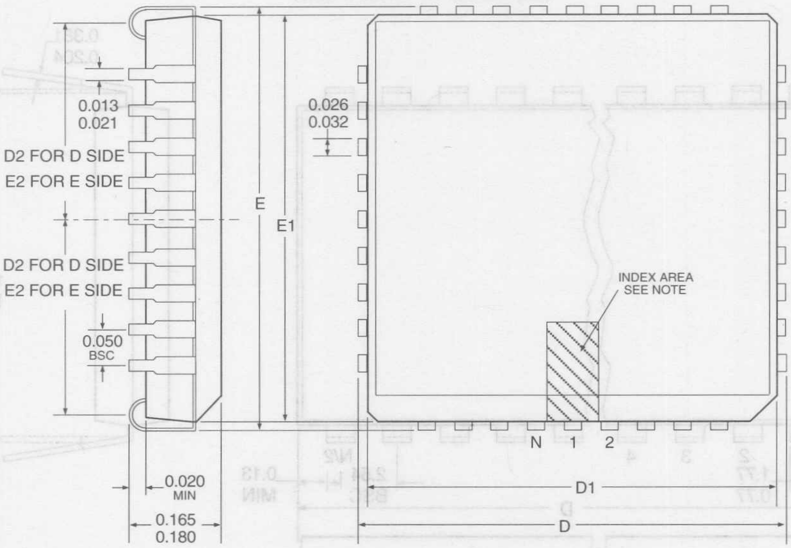
N	Number of Leads Pkg. Designator	28 A	40 A
D	Body Length	35.1/39.7	50.3/53.2
Notes		—	—
JEDEC Outline Designation		MS-011AB	MS-011AC

NOTES: 4. Lead thickness is measured at seating plane or below.
5. Lead spacing tolerance is non-cumulative.
6. Exact body and lead configuration at vendor's option within limits shown.

SQUARE PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATORS EA, EB, or EP

Dimensions in Inches



Dwg. MA-005A in

N	Number of Leads Pkg. Designator	20 EP	28 EA	28 EB	28 EP	44 EB	44 EP
D	Overall Length	0.385/0.395	0.485/0.495	0.485/0.495	0.485/0.495	0.685/0.695	0.685/0.695
D1	Body Length	0.350/0.356	0.450/0.456	0.450/0.456	0.450/0.456	0.650/0.656	0.650/0.656
D2	Row Spacing	0.141/0.169	0.191/0.219	0.191/0.219	0.191/0.219	0.291/0.319	0.291/0.319
E	Overall Width	0.385/0.395	0.485/0.495	0.485/0.495	0.485/0.495	0.685/0.695	0.685/0.695
E1	Body Width	0.350/0.356	0.450/0.456	0.450/0.456	0.450/0.456	0.650/0.656	0.650/0.656
E2	Row Spacing	0.141/0.169	0.191/0.219	0.191/0.219	0.191/0.219	0.291/0.319	0.291/0.319
Notes	(Leads Affected)	—	2 (12-18)	2 (5-11, 19-25)	—	2 (7-17, 29-39)	—
JEDEC Outline Designation		MS-018AA	MS-018AB	MS-018AB	MS-018AB	MS-018AC	MS-018AC

NOTES: 1. Index is centered on "D" side.

2. Webbed lead frame. Leads indicated are internally one piece.

3. Lead spacing tolerance is non-cumulative.

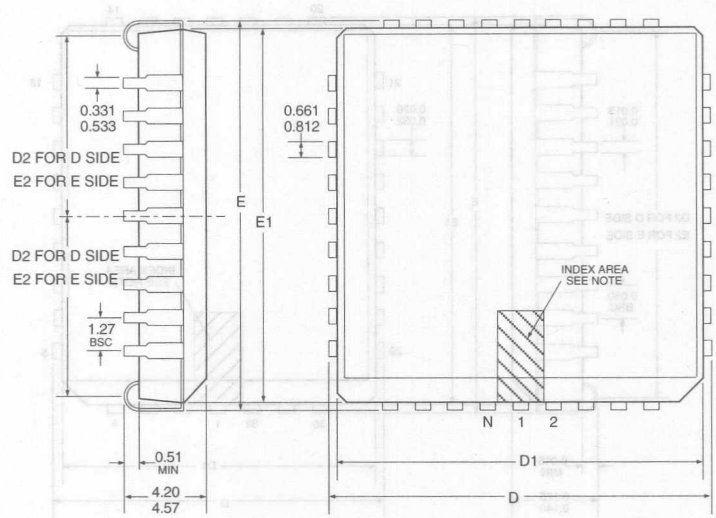
4. Exact body and lead configuration at vendor's option within limits shown.

PACKAGE OUTLINES

SQUARE PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATORS EA, EB, or EP

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-005A mm

N	Number of Leads	20	28	28	28	44	44
	Pkg. Designator	EP	EA	EB	EP	EB	EP
D	Overall Length	9.78/10.03	12.32/12.57	12.32/12.57	12.32/12.57	17.40/17.65	17.40/17.65
D1	Body Length	8.890/9.042	11.430/11.582	11.430/11.582	11.430/11.582	16.510/16.662	16.510/16.662
D2	Row Spacing	3.58/4.29	4.85/5.56	4.85/5.56	4.85/5.56	7.39/8.10	7.39/8.10
E	Overall Width	9.78/10.03	12.32/12.57	12.32/12.57	12.32/12.57	17.40/17.65	17.40/17.65
E1	Body Width	8.890/9.042	11.430/11.582	11.430/11.582	11.430/11.582	16.510/16.662	16.510/16.662
E2	Row Spacing	3.58/4.29	4.85/5.56	4.85/5.56	4.85/5.56	7.39/8.10	7.39/8.10
Notes	(Leads Affected)	—	2 (12-18)	2 (5-11, 19-25)	—	2 (7-17, 29-39)	—
JEDEC Outline Designation		MS-018AA	MS-018AB	MS-018AB	MS-018AB	MS-018AC	MS-018AC

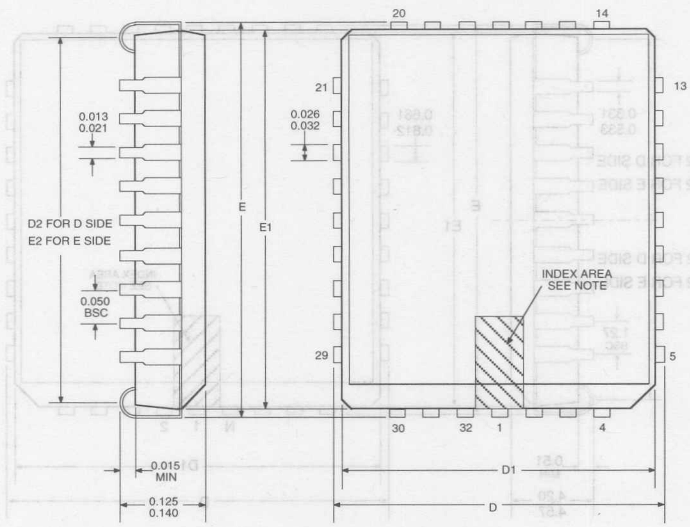
NOTES: 1. Index is centered on "D" side.
2. Webbed lead frame. Leads indicated are internally one piece.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown

PACKAGE OUTLINES

RECT. PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATOR EQ

Dimensions in Inches



Dwg. MA-006 in

N	Number of Leads	32 (7 x 9)
	Pkg. Designator	EQ
D	Overall Length	0.485/0.495
D1	Body Length	0.447/0.453
D2	Row Spacing	0.376/0.446
E	Overall Width	0.585/0.595
E1	Body Width	0.547/0.553
E2	Row Spacing	0.476/0.546
Notes	(Leads Affected)	—
JEDEC Outline Designation		MS-016AE

NOTES: 1. Index is centered on (short) “D” side.

3. Lead spacing tolerance is non-cumulative.

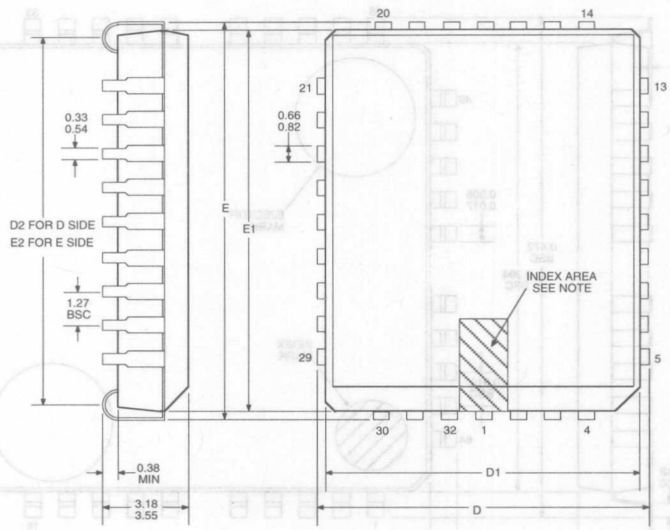
4. Exact body and lead configuration at vendor’s option within limits shown

PACKAGE OUTLINES

RECT. PLASTIC LEADED CHIP CARRIER (PQCC)

PACKAGE DESIGNATOR EQ

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MA-006 mm

N	Number of Leads Pkg. Designator	32 (7 x 9) EQ						
D	Overall Length	12.32/12.57						
D1	Body Length	11.36/11.50						
D2	Row Spacing	9.56/11.32						
E	Overall Width	14.86/15.11						
E1	Body Width	13.90/14.04						
E2	Row Spacing	12.10/13.86						
Notes	(Leads Affected)	—						
JEDEC Outline Designation		MS-016AE						

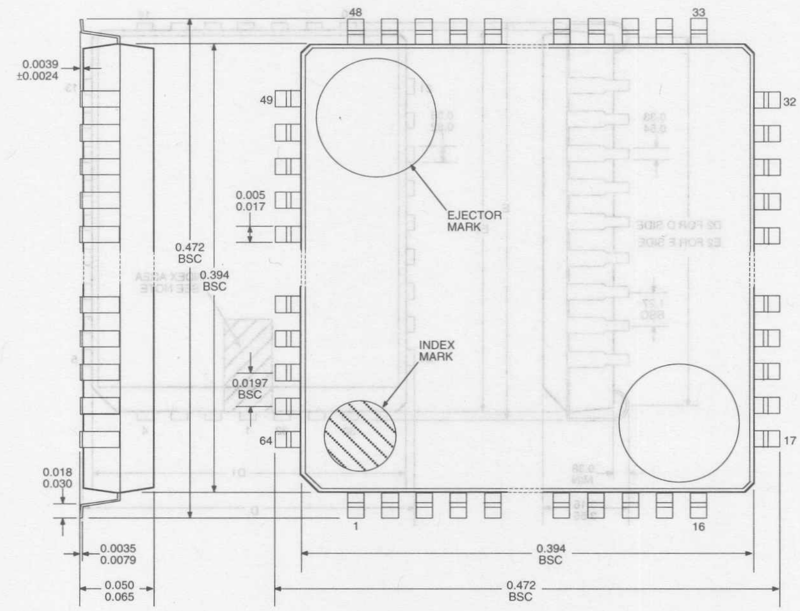
NOTES: 1. Index is centered on (short) "D" side.
3. Lead spacing tolerance is non-cumulative.
4. Exact body and lead configuration at vendor's option within limits shown

PACKAGE OUTLINES

LOW-PROFILE QUAD FLATPACK

PACKAGE DESIGNATOR JT

Dimensions in Inches
(Based on 1 mm = 0.03937")



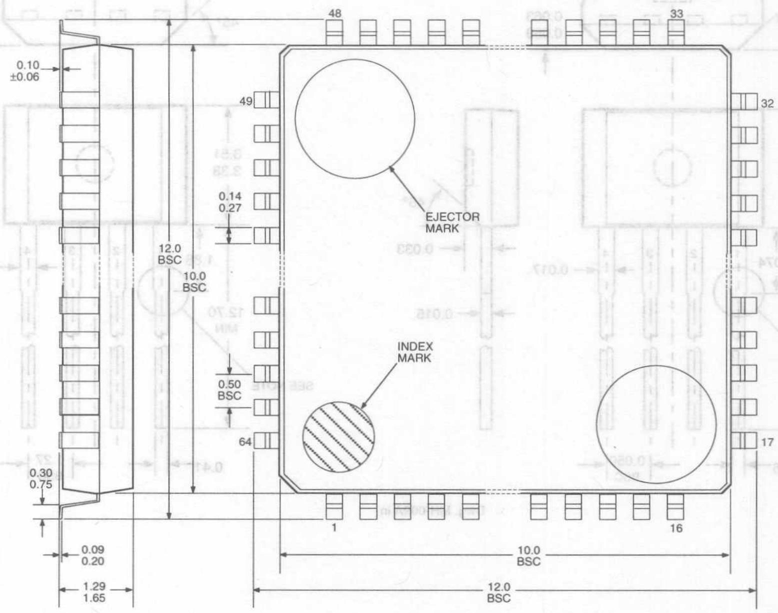
Dwg. MA-004 in

NOTES: 1. This device is similar to JEDEC registration MO-136BJ except for certain tolerances. Contact factory for detailed information.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. The top package body size may be smaller than the bottom package body size by as much as 0.006". Body dimensions include mold mismatch but do not include mold protrusion.

PACKAGE OUTLINES

LOW-PROFILE QUAD FLATPACK

PACKAGE DESIGNATOR JT
Dimensions in Millimeters



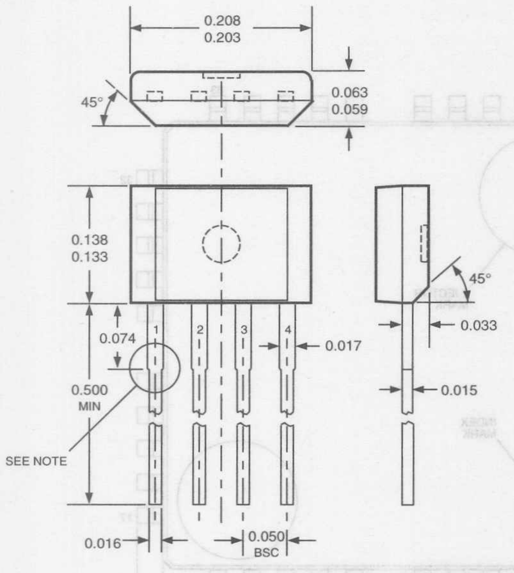
Dwg. MA-004 mm

NOTES: 1. This device is similar to JEDEC registration MO-136BJ except for certain tolerances. Contact factory for detailed information.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm. Body dimensions include mold mismatch but do not include mold protrusion.

PLASTIC SIP

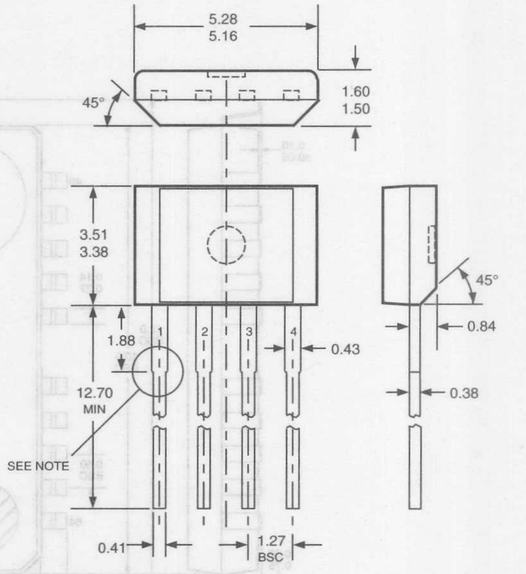
PACKAGE DESIGNATOR K

Dimensions in Inches



Dwg. MH-009A in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



Dwg. MH-009A mm

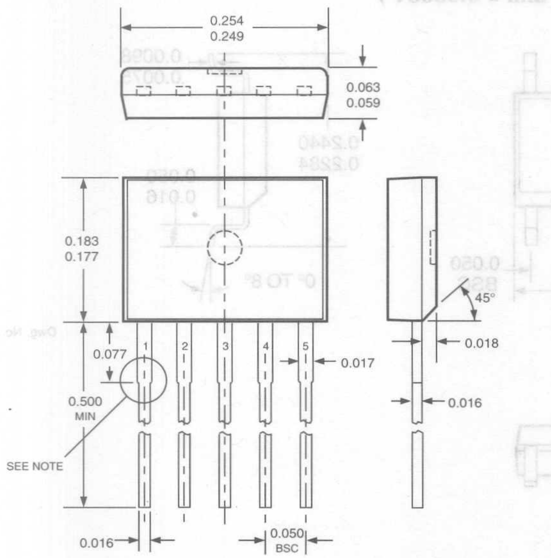
NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

PACKAGE OUTLINES

PLASTIC SIP

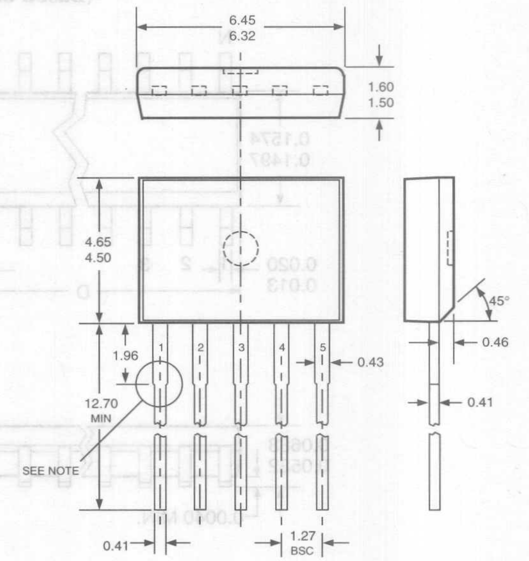
PACKAGE DESIGNATOR KA

Dimensions in Inches



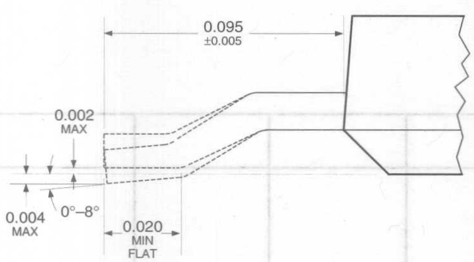
Dwg. MH-010A in

Dimensions in Millimeters (Based on 1" = 25.4 mm)

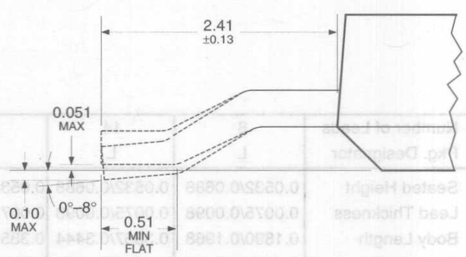


Dwg. MH-010A mm

SURFACE-MOUNT LEAD FORM TL



Dwg. MH-015 in



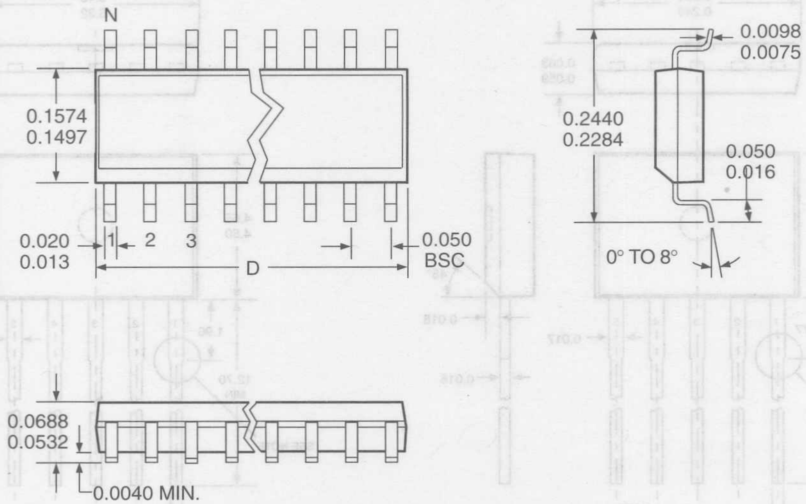
Dwg. MH-015 mm

NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

PLASTIC SOIC
(0.150" body width)

PACKAGE DESIGNATOR L

Dimensions in Inches
(Based on 1 mm = 0.03937")



Dwg. No. MA-007 in

N	Number of Leads Pkg. Designator	8 L	14 L	16 L				
A	Seated Height	0.0532/0.0688	0.0532/0.0688	0.0532/0.0688				
C	Lead Thickness	0.0075/0.0098	0.0075/0.0098	0.0075/0.0098				
D	Body Length	0.1890/0.1968	0.3367/0.3444	0.3859/0.3937				
E	Body Width	0.1497/0.1574	0.1497/0.1574	0.1497/0.1574				
H	Overall Width	0.2284/0.2440	0.2284/0.2440	0.2284/0.2440				
Notes	(Leads Affected)	—	—					
JEDEC Outline Designation		MS-012AA	MS-012AB	MS-012AC				

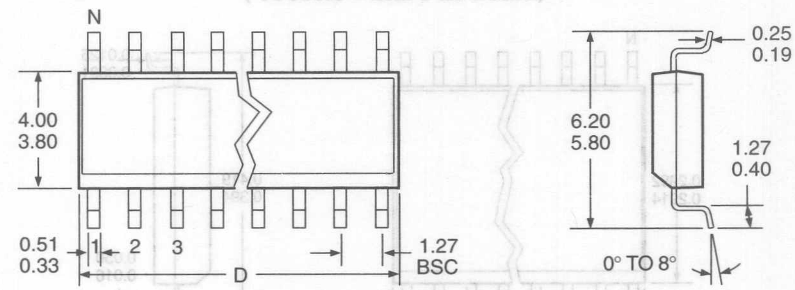
NOTES: 2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. For package designator 'LR', see plastic small-outline transistor (SOT-23/TO-236AB).

PACKAGE OUTLINES

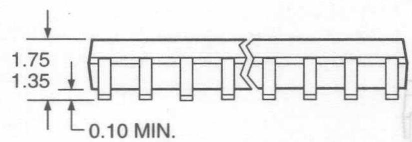
PLASTIC SOIC (3.75 mm body width)

PACKAGE DESIGNATOR L

Dimensions in Millimeters



Dwg. No. MA-007 mm



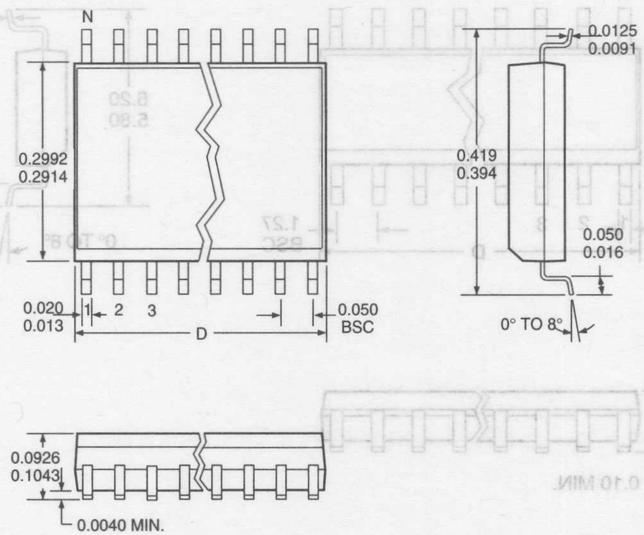
N	Number of Leads	8	14	16			
	Pkg. Designator	L	L	L			
A	Seated Height	1.35/1.75	1.35/1.75	1.35/1.75			
C	Lead Thickness	0.19/0.25	0.19/0.25	0.19/0.25			
D	Body Length	4.80/5.00	8.55/8.75	9.80/10.0			
E	Body Width	3.80/4.00	3.80/4.00	3.80/4.00			
H	Overall Width	5.80/6.20	5.80/6.20	5.80/6.20			
Notes	(Leads Affected)	—	—	—			
JEDEC Outline Designation		MS-012AA	MS-012AB	MS-012AC			

NOTES: 2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. For package designator 'LR', see plastic small-outline transistor (SOT-23/TO-236AB).

PACKAGE OUTLINES

WIDE-BODY PLASTIC SOIC (0.300" body width)

PACKAGE DESIGNATORS LB or LW
Dimensions in Inches
(Based on 1 mm = 0.03937")



Dwg. No. MA-008 in

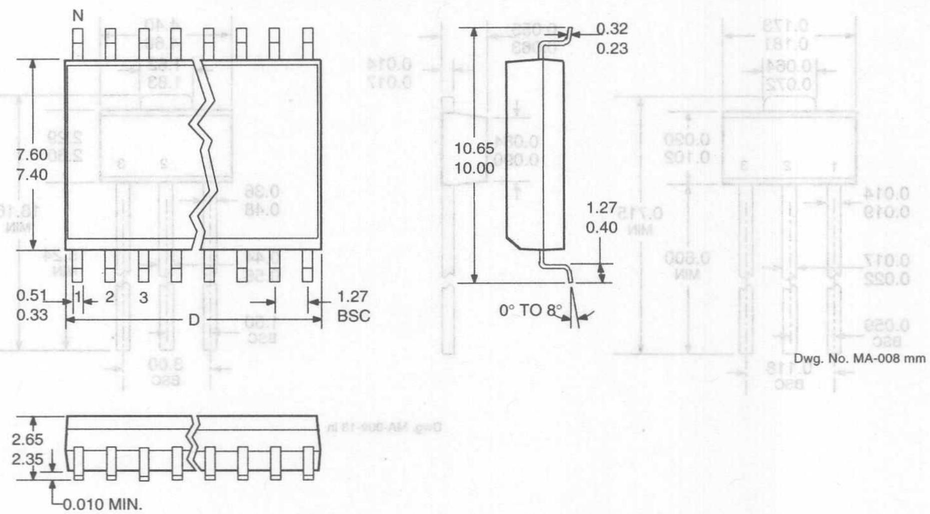
N	Number of Leads	16	16		18	20	24	28
	Pkg. Designator	LB	LW		LW	LB	LB	LW
A	Seated Height	0.0926/0.1043	0.0926/0.2043		0.0926/0.1043	0.0926/0.1043	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0091/0.0125	0.0091/0.0125		0.0091/0.0125	0.0091/0.0125	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.3977/0.4133	0.3977/0.4133		0.4469/0.4625	0.4961/0.5118	0.5985/0.6141	0.6969/0.7125
E	Body Width	0.2914/0.2992	0.2914/0.2992		0.2914/0.2992	0.2914/0.2992	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.394/0.419	0.394/0.419		0.394/0.419	0.394/0.419	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	1 (4, 5, 12, 13)	—		—	1 (4-7, 14-17)	1 (6, 7, 18, 19)	—
JEDEC Outline Designation		MS-013AA	MS-013AA		MS-013AB	MS-013AC	MS-013AD	MS-013AE

NOTES: 1. Webbed lead frame. Leads indicated are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. For package designator 'LR', see plastic small-outline transistor (SOT-23/TO-236AB).

WIDE-BODY PLASTIC SOIC (7.50 mm body width)

PACKAGE DESIGNATORS LB or LW

Dimensions in Millimeters



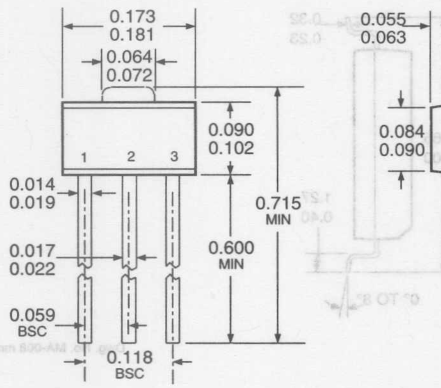
N	Number of Leads Pkg. Designator	16 LB	16 LW		18 LW	20 LB	24 LB	28 LW
A	Seated Height	2.35/2.65	2.35/2.65		2.35/2.65	2.35/2.65	2.35/2.65	2.35/2.65
C	Lead Thickness	0.23/0.32	0.23/0.32		0.23/0.32	0.23/0.32	0.23/0.32	0.23/0.32
D	Body Length	10.10/10.50	10.10/10.50		11.35/11.75	12.60/13.00	15.20/15.60	17.70/18.10
E	Body Width	7.40/7.60	7.40/7.60		7.40/7.60	7.40/7.60	7.40/7.60	7.40/7.60
H	Overall Width	10.00/10.65	10.00/10.65		10.00/10.65	10.00/10.65	10.00/10.65	10.00/10.65
Notes	(Leads Affected)	1 (4, 5, 12, 13)	—		—	1 (4-7, 14-17)	1 (6, 7, 18, 19)	—
JEDEC Outline Designation		MS-013AA	MS-013AA		MS-013AB	MS-013AC	MS-013AD	MS-013AE

NOTES: 1. Webbed lead frame. Leads indicated are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. For package designator 'LR', see plastic small-outline transistor (SOT-23/TO-236AB).

LONG-LEADED PLASTIC SOT

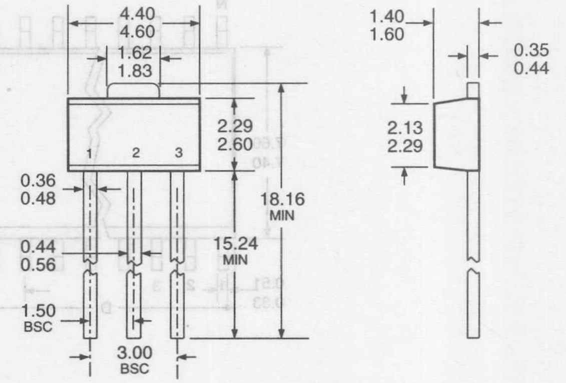
PACKAGE DESIGNATOR LL

Dimensions in Inches (Based on 1 mm = 0.0394")



Dwg. MA-009-13 in

Dimensions in Millimeters



Dwg. MA-009-13 mm

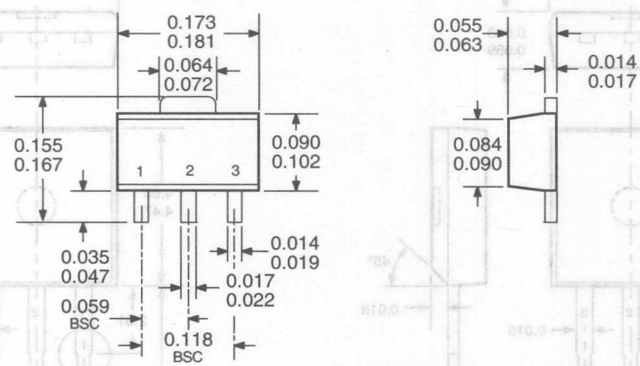
For package designator 'LR', see plastic small-outline transistor (SOT-23/TO-236AB).

PACKAGE OUTLINES

PLASTIC SOT (SOT-89/TO-243AA)

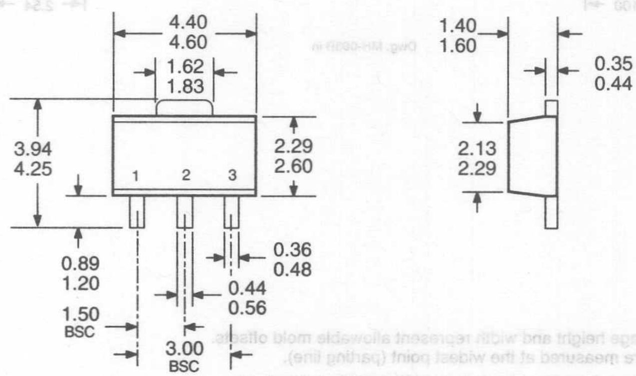
PACKAGE DESIGNATOR LT

Dimensions in Inches (Based on 1 mm = 0.0394")



Dwg. No. MA-009-3 in

Dimensions in Millimeters



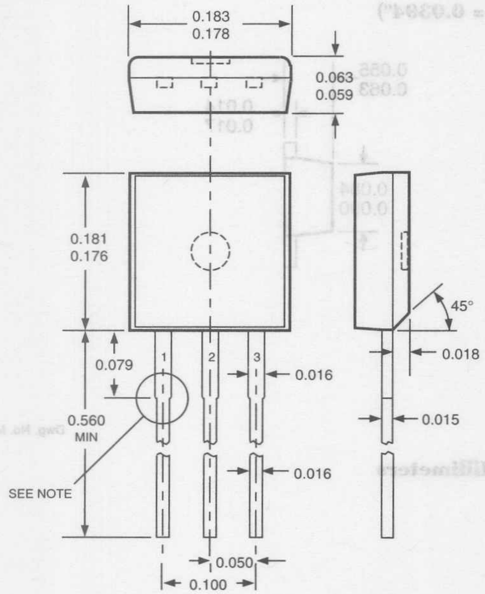
Dwg. No. MA-009-3 mm

PACKAGE OUTLINES

PLASTIC SIP

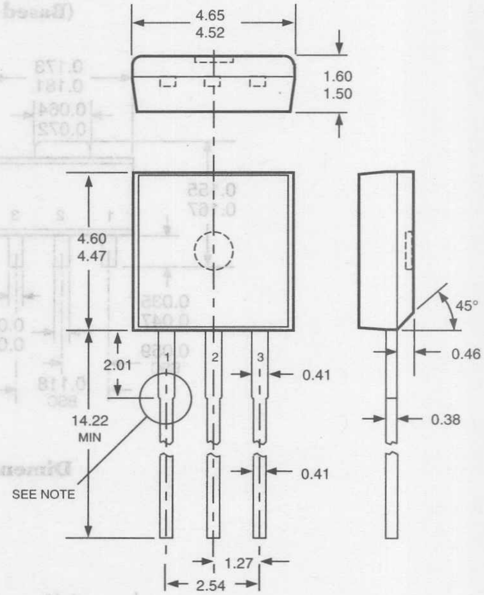
PACKAGE DESIGNATOR U

Dimensions in Inches



Dwg. MH-003B in

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



Dwg. MH-003B mm

NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clean transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.
6. Minimum lead length was 0.500" (12.70 mm). If existing product to the original specifications is not acceptable, contact sales office before ordering.

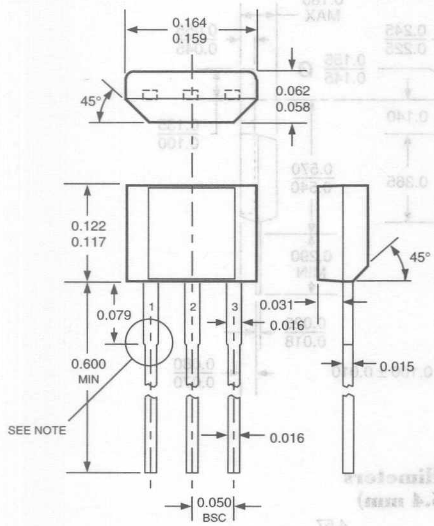
PACKAGE OUTLINES

PLASTIC SIP

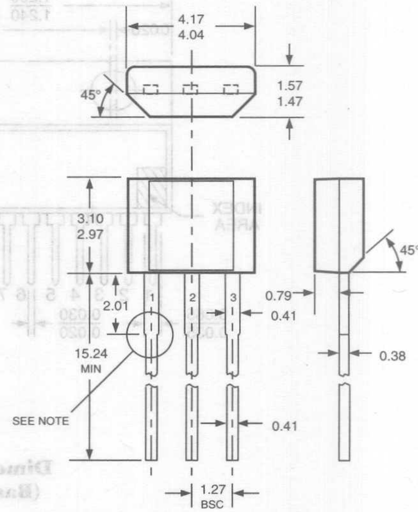
PACKAGE DESIGNATOR UA

Dimensions in Inches

Dimensions in Millimeters (Based on 1" = 25.4 mm)

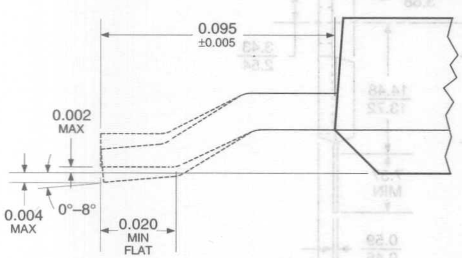


Dwg. MH-014B in

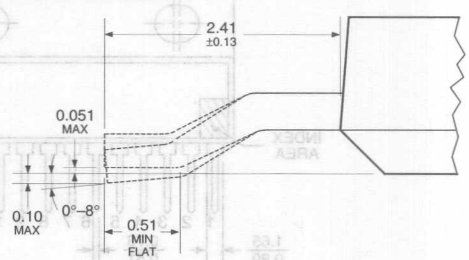


Dwg. MH-014B mm

SURFACE-MOUNT LEAD FORM TL



Dwg. MH-015 in



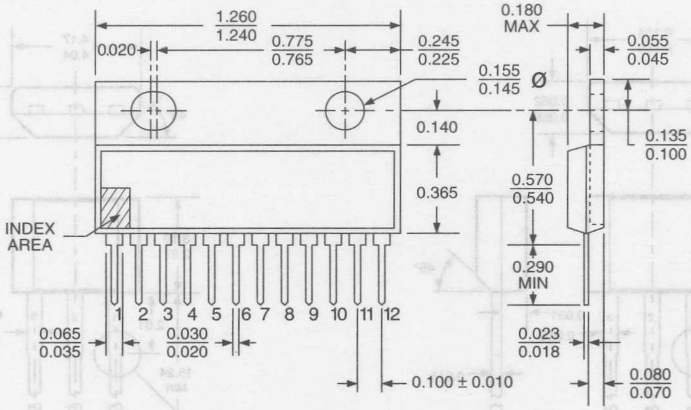
Dwg. MH-015 mm

NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clean transition area is 0.035" (0.89 mm).
4. Where no tolerance is specified, dimension is nominal.
6. Minimum lead length was 0.500" (12.70 mm). If existing product to the original specification is not acceptable, contact sales office before ordering.

PLASTIC POWER-TAB SIP

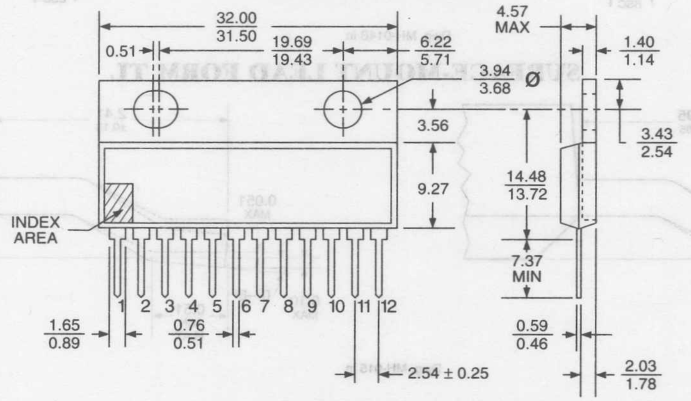
PACKAGE DESIGNATOR W

Dimensions in Inches



Dwg. MP-007 in

Dimensions in Millimeters (Based on 1" = 25.4 mm)



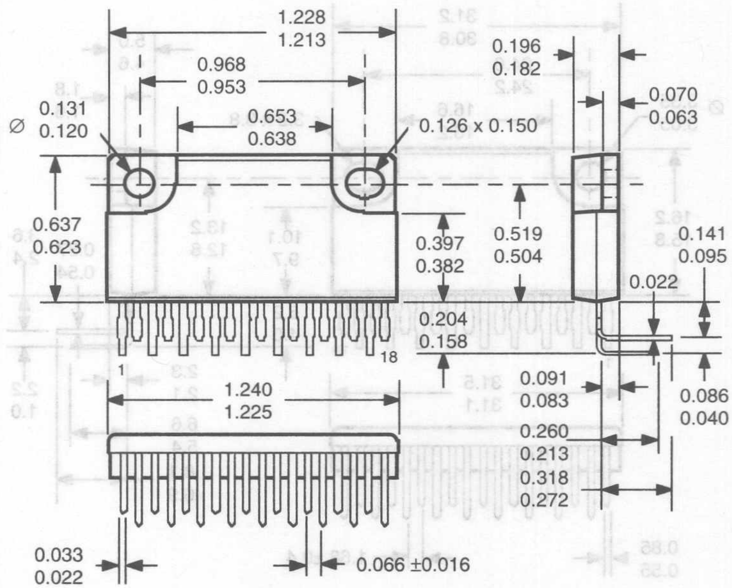
Dwg. No. MP-007 mm

NOTES:
1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. Lead gauge plane is 0.030" (0.762 mm) below seating plane.

PACKAGE OUTLINES

PLASTIC POWER-TAB SIP (with lead forming for horizontal mounting)

PACKAGE DESIGNATOR WH
Dimensions in Inches
(Based on 1 mm = 0.03937")

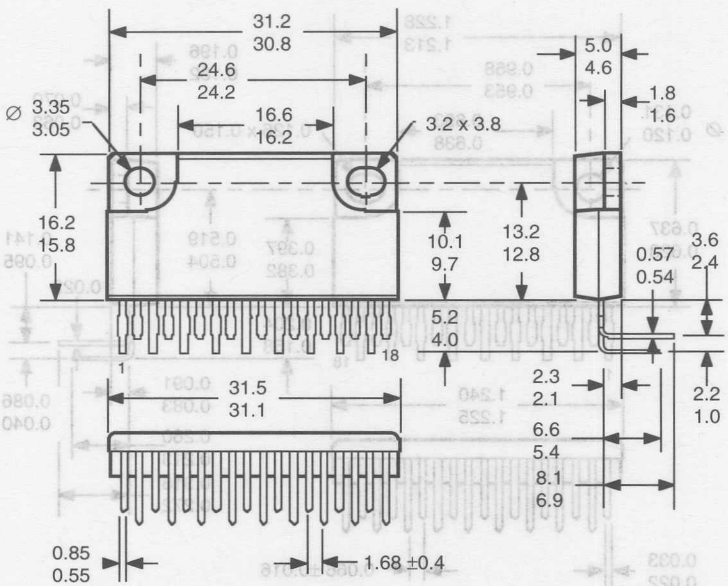


Dwg. MP-006 in

PACKAGE OUTLINES

PLASTIC POWER-TAB SIP (with lead forming for horizontal mounting)

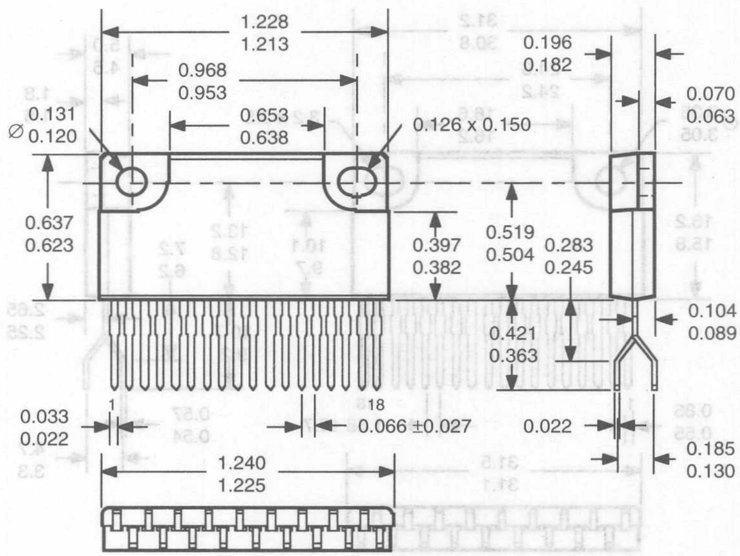
PACKAGE DESIGNATOR WH
Dimensions in Millimeters



Dwg. MP-006 mm

PLASTIC POWER-TAB SIP (with lead forming for vertical mounting)

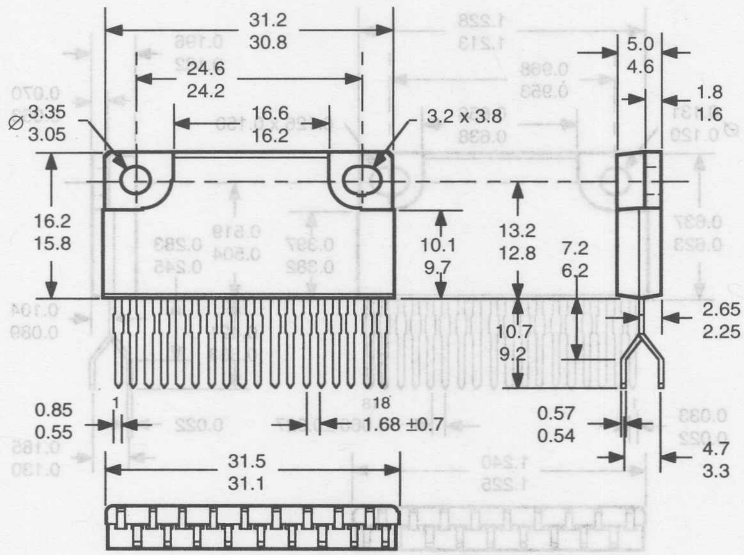
PACKAGE DESIGNATOR WV
Dimensions in Inches
(Based on 1 mm = 0.03937")



Dwg. MP-004 in

PLASTIC POWER-TAB SIP
(with lead forming for vertical mounting)

PACKAGE DESIGNATOR WV
Dimensions in Millimeters



Dwg. MP-004 mm

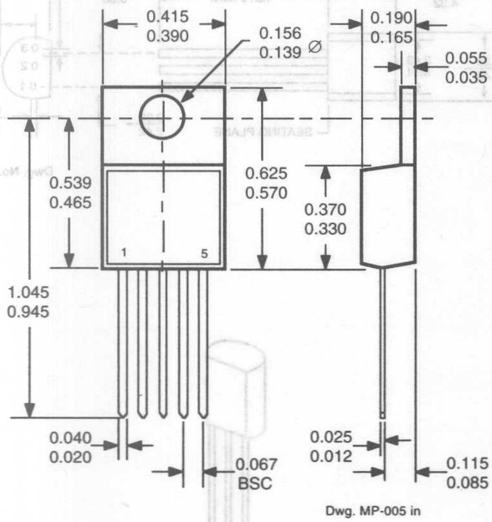
PACKAGE OUTLINES

PLASTIC POWER-TAB SIP

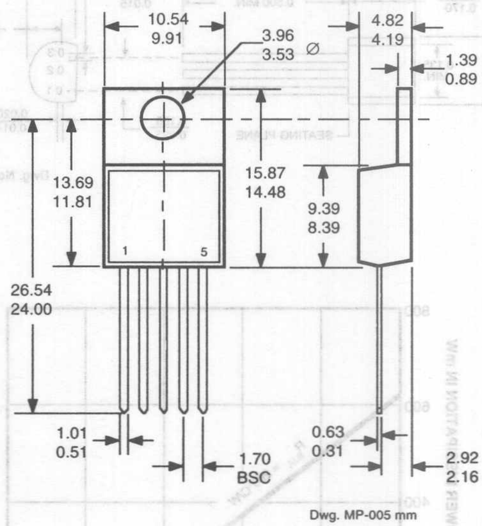
PACKAGE DESIGNATOR Z

(JEDEC outline TS-001)

Dimensions in Inches

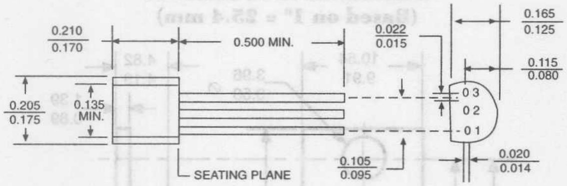


Dimensions in Millimeters
(Based on 1" = 25.4 mm)



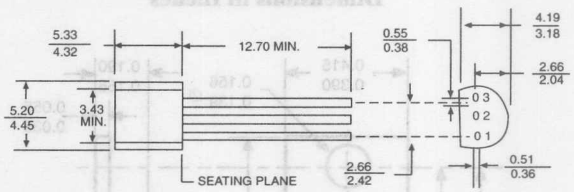
PLASTIC TRANSISTOR
(TO-92/TO-226AA)

Dimensions in Inches

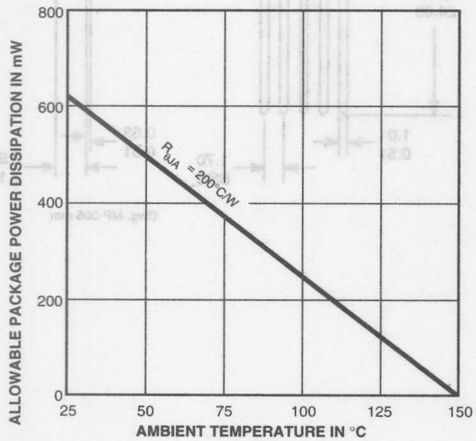


Dwg. No. A-13,610

Dimensions in Millimeters
(Based on 1" = 25.4 mm)



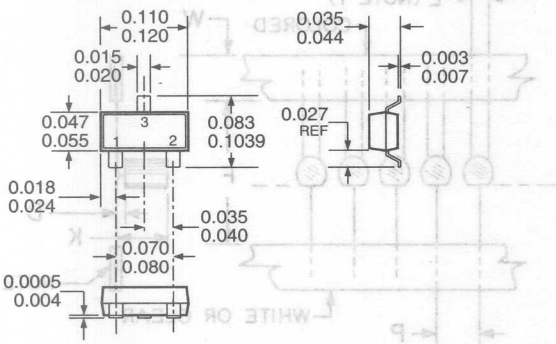
Dwg. No. A-13,611



Dwg. GD-001

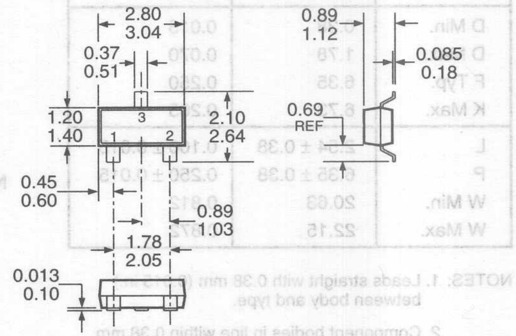
PLASTIC SMALL-OUTLINE TRANSISTOR (SOT-23/TO-236AB)

Dimensions in Inches (Based on 1 mm = 0.03937")

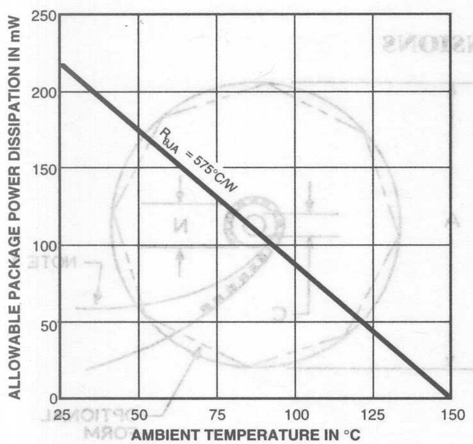


Dwg. MA-010 in

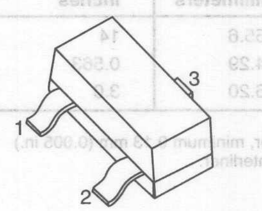
Dimensions in Millimeters



Dwg. MA-010 mm



Dwg. GD-002



Die size = 0.025" by 0.025" (0.635 mm by 0.635 mm). Other factors that determine allowable package power dissipation include circuit board material, pad size, and proximity of other heat-producing circuit elements.

TAPE AND REEL INFORMATION FOR DISCRETE DEVICES

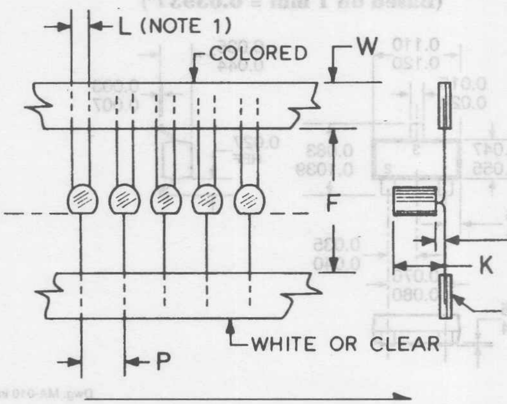
AXIAL-TAPED TO-226AA TAPE DIMENSIONS

Dimension	Millimeters	Inches
D Min.	0.38	0.015
D Max.	1.78	0.070
F Typ.	6.35	0.250
K Max.	6.73	0.265
L	2.54 ± 0.38	0.100 ± 0.015
P	6.35 ± 0.38	0.250 ± 0.015
W Min.	20.63	0.812
W Max.	22.15	0.872

NOTES: 1. Leads straight with 0.38 mm (0.015 in.) between body and type.

2. Component bodies in line within 0.38 mm (0.015 in.).

3. Lead length in contact with tape, each side, 1.78 mm (0.070 in.), minimum.

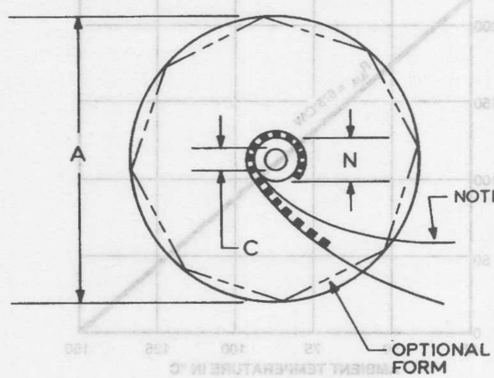


Dwg. No. A-13,626

REEL DIMENSIONS

Dimension	Millimeters	Inches
A Max.	355.6	14
C	14.29	0.563
N Min.	76.20	3.0

NOTES: 1. Kraft paper, minimum 0.13 mm (0.005 in.) thick, as interliner.

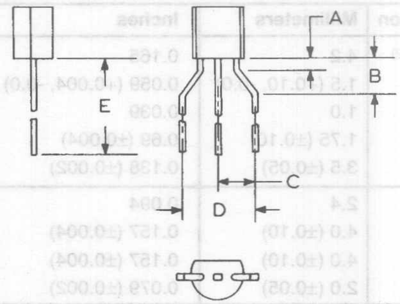


Dwg. No. A-13,627

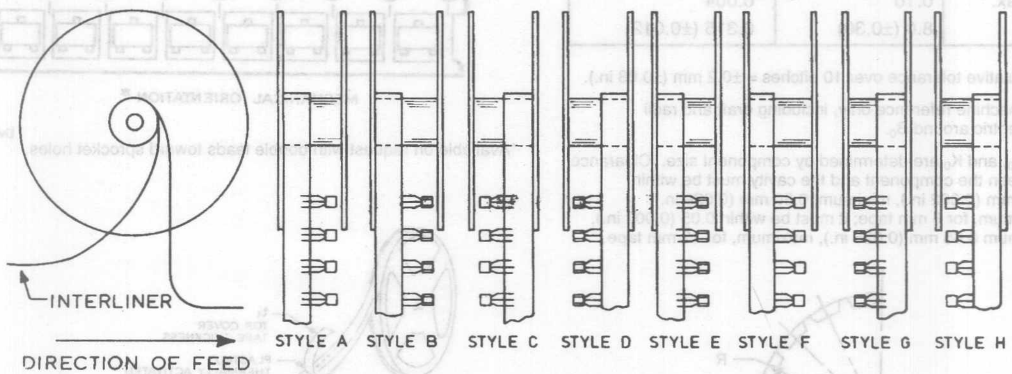
RADIAL-TAPED TO-226AA LEAD DIMENSIONS

Dimension	Millimeters	Inches
A	1.52 ± 0.38	0.060 ± 0.015
B	3.18 ± 0.38	0.125 ± 0.015
C	2.54 ± 0.30	0.100 ± 0.012
D	5.08 ± 0.76, -0.20	0.200 + 0.030, -0.008
E Min.	12.70	0.500
E Max.	15.70	0.620

Styles A and F—Flat side down, carrier tape to left.
Styles B and E—Flat side up, carrier tape to left.
Styles C and H—Flat side sown, carrier tape to right.
Styles D and G—Flat side up, carrier tape to right.



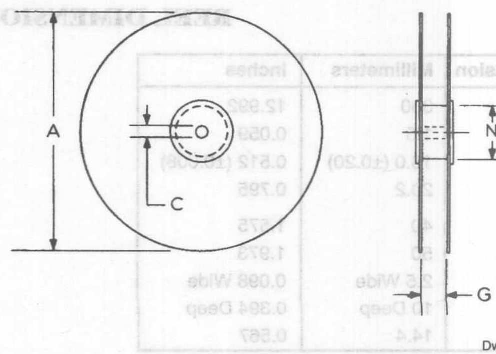
Dwg. No. A-13,628



Dwg. No. A-13,629

REEL DIMENSIONS

Dimension	Millimeters	Inches
A	355.6 ± 6.35	14 ± 0.250
C	21.59 ± 6.35	0.850 ± 0.250
G	45.72 ± 7.62	1.800 ± 0.300
N Min.	76.20 ± 6.35	3.0 ± 0.250



Dwg. No. A-13,630

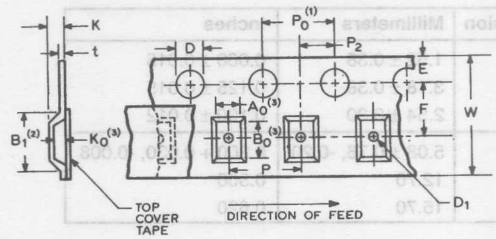
TAPE DIMENSIONS FOR TO-236AB

Dimension	Millimeters	Inches
B_1 Max.[2]	4.2	0.165
D	1.5 (+0.10, -0.0)	0.059 (+0.004, -0.0)
D_1 Min.	1.0	0.039
E	1.75 (±0.10)	0.69 (±0.004)
F	3.5 (±0.05)	0.138 (±0.002)
K Max.	2.4	0.094
P	4.0 (±0.10)	0.157 (±0.004)
P_0[1]	4.0 (±0.10)	0.157 (±0.004)
P_2	2.0 (±0.05)	0.079 (±0.002)
R Min.	25	0.984
t Max.	0.400	0.016
t_1 Max.	0.10	0.004
W	8.0 (±0.30)	0.315 (±0.012)

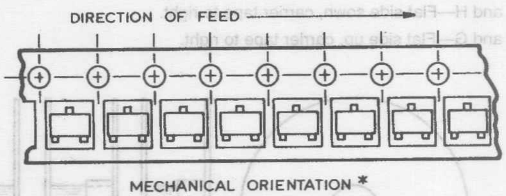
(1) Cumulative tolerance over 10 pitches = ±0.2 mm (±0.08 in.).

(2) For machine reference only, including draft and radii concentric around B_0.

(3) A_0, B_0, and K_0 are determined by component size. Clearance between the component and the cavity must be within 0.05 mm (0.002 in.), minimum, 0.50 mm (0.020 in.), maximum, for 8 mm tape; it must be within 0.05 (0.002 in.), minimum 0.65 mm (0.026 in.), maximum, for 12 mm tape.

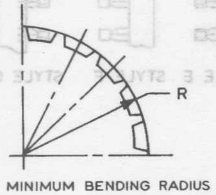


Dwg. No. A-13,310

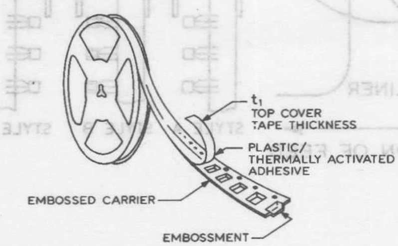


Dwg. No. A-13,313

*Available on request with double leads toward sprocket holes.



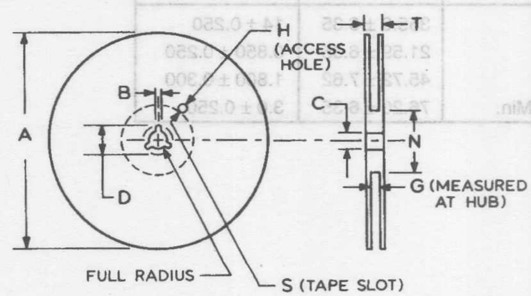
Dwg. No. A-13,312



Dwg. No. A-13,312

REEL DIMENSIONS FOR TO-236AB

Dimension	Millimeters	Inches
A Max.	330	12.992
B Min.	1.5	0.059
C	13.0 (±0.20)	0.512 (±0.008)
D Min.	20.2	0.795
H Min.	40	1.575
N Min.	50	1.973
S Min.	2.5 Wide	0.098 Wide
	10 Deep	0.394 Deep
T Max.	14.4	0.567



Dwg. No. A-13,314

TO-236AB

SHIPPING

Shipping options for small-outline transistors and diodes include vial pack and 8 mm tape and reel for use with automated insertion equipment.

The 8 mm tape pack puts 3000 devices on a 7-inch (178 mm) reel. Components can be placed in the tape cavity with the single lead toward the sprocket hole or with the double leads toward the sprocket hole. Tape and reel dimensions conform to EIA Standard 481 Rev. A.

MOUNTING

Surface-mount semiconductors can be attached to substrates by conventional techniques such as vapor-phase or wave soldering and hot-plate methods.

Recommended maximum time/temperature soldering conditions are shown in the graph. In general, attachment with a soldering iron is not recommended due to the difficulty of consistently controlling temperature and time temperature.

CLEANING

Small-outline semiconductors are compatible with most commonly used defluxing solvents. Freon-based alcohol compounds such as Du Pont TMS or TES (or equivalents) are recommended. Solutions containing methylene chloride or other known epoxy solvent should not be used.